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(54) **SPUR REDUCTION TECHNIQUE FOR SAMPLING PLL'S**

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See application file for complete search history.

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(57) **ABSTRACT**

Control circuitry and method of controlling for a sampling phase lock loop (PLL). By controlling the duty cycle of a sampling control signal, in accordance with the PLL reference and output signals, spurious output signals from the sampling PLL being controlled can be reduced.

20 Claims, 6 Drawing Sheets