A combined receiver front-end for Bluetooth and HiperLAN/2

Vincent Arkesteijn[1], Roel Schiphorst[2], Fokke Hoeksema[2],
Eric Klumperink[1], Bram Nauta[1] and Kees Slump[2]
[1]Integrated Circuit Design Group, MESA$^+$ Institute
[2]Laboratory of Signals and Systems, CTIT Institute
Department of Electrical Engineering, Mathematics and Computer Science
University of Twente, P.O. box 217 - 7500 AE Enschede - The Netherlands
http://www.sas.el.utwente.nl/home/SDR/

Abstract— **A Software Defined Radio is a radio receiver that is reconfigurable by software. This reconfigurability leads to flexibility that can be used to offer more functionality to the user. Also, because common reconfigurable hardware can be used for very diverse radio interfaces, production and logistics can be faster and cheaper.**

In our Software Defined Radio project we aim at a receiver that is able to receive signals of any contemporary or future radio standard. However, because we need tangible specifications in order to design, we have chosen to implement a combination of two rather different standards: Bluetooth and HiperLAN/2.

Both the analogue and the digital/software parts are included in the design. A CMOS integrated wideband analogue front-end containing a low noise amplifier, downconversion mixers and filters has been designed. This front-end is connected to a PCB that contains two analogue-to-digital convertors and a sample rate convertor (SRC). The output of this board is connected to a standard PC through a digital I/O board with PCI bus. Software on this PC performs the demodulation.

We conclude that an analog wide-band front-end with a flexible SRC combined with appropriate software on an inherently flexible PC forms a promising architecture for Software Defined Radio.

keywords: Software Defined Radio, HiperLAN/2, Bluetooth, Radio Frequency, Wide-band front-end, MAP receiver, Demonstrator.

I. Introduction

In our SDR project we aim at combining two different types of standards –Bluetooth and HiperLAN/2– on one common hardware platform. HiperLAN/2 is a high-speed Wireless LAN (WLAN) standard [1], whereas Bluetooth is a low-cost and low-speed Personal Area Network (PAN) standard [2]. As is illustrated in table I the standards differ in several aspects and pose an interesting challenge for an SDR platform.

We focus on the radio front-end of a receiver, so from antenna (Radio Frequency (RF) signal) till and including demodulator (raw bits).

TABLE I
Bluetooth & HiperLAN/2 Parameters.

	Bluetooth	HiperLAN/2
System	PAN	WLAN
Frequency Band	2.4-2.4835 GHz	5.150-5.300 GHz, 5.470-5.725 GHz
Access Method	CDMA	TDMA
Duplex Method	TDD	TDD
Modulation Type	GFSK	OFDM
Max. Data Rate	1 Mbps	54 Mbps
Channel Spacing	1 MHz	20 MHz
Max Power Peak	100 mW	200 mW - 1 W

Our vehicle is a notebook to which we add SDR functionality. The analog front-end is made to be flexible and reconfigurable, see section II, in which we present the wide band integrated front-end. The digital baseband part consists of a channel selection and sample-rate conversion part in flexible and reconfigurable hardware and a demodulator part with algorithms using GPP hardware, see section III. We think the latter is feasible as current processors, such as the Pentium IV have huge processing capabilities. This capability is even increased due to special (signal processing) instructions such as SSE.

Most of the system-level design decisions were presented last year [3]. In this paper we present the actually designed demonstrator and discuss implementation choices. The combination of wide-band analog front-end and GPP hardware is capable of receiving Bluetooth and HiperLAN/2 signals.

II. Analogue front-end

This section discusses the analogue part of our SDR front-end. A block schematic can be seen in figure 1.

As discussed in [3], the front-end uses separate antennas and RF filters for the various bands. The rest of the

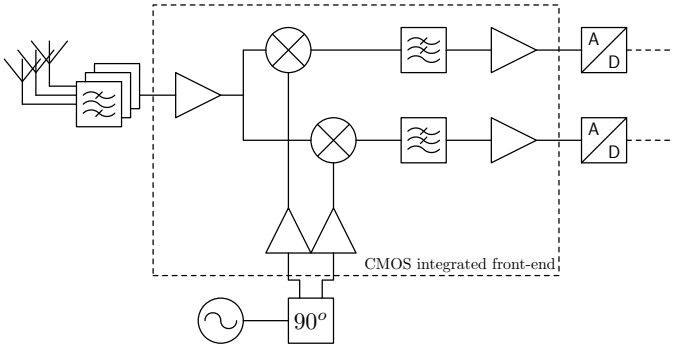

Fig. 1
ANALOGUE FRONT-END.

receiver however, which should have a large bandwidth, is integrated. This way, the integrated circuit can still be used for a large number of applications, and only a new PCB with filters and possibly the antenna has to be designed when a receiver for a new frequency band is required.

The rest of the discussion in this section will focus on the part in figure 1 inside the dashed rectangle. For this part, an integrated circuit has been designed using a standard 0.18μm CMOS process. This front-end poses a strong technical challenge, as it has to work over a wide bandwidth of a few GHz, while satisfying high linearity and noise demands. We aim to show that this is feasible in CMOS IC-processes available in the near future.

The circuit starts with a wideband low noise amplifier (LNA). This LNA employs noise cancelling, a recently published technique which is useful for obtaining a low noise figure over a wide bandwidth [4].

The LNA is followed by two mixers. Two local oscillator (LO) signals with a phase difference of 90 degrees are present. These implement quadrature down-conversion, enabling both zero-IF and low-IF architectures.

The two mixers are both followed by a low-pass filter with a cut-off frequency of around 10 MHz. This is more than enough for a single channel Bluetooth signal and sufficient for HiperLAN/2 signals.

Finally, the circuit contains two baseband amplifiers.

The circuit is currently being fabricated, and measurements will begin shortly.

III. DIGITAL PART

This section first presents the functional architecture of a Bluetooth-enabled HiperLAN/2 receiver. Subsequently the real-time demonstrator for the digital part of the project is described.

A. Functional architecture

The Bluetooth standard is designed for low power and low cost receivers. Therefore a large part of the receiver is implemented in the analogue domain which does not map on a digital OFDM receiver. In our project we used a Maximum A posteriori Probability (MAP) receiver for Bluetooth. This receiver has better and even optimal performance compared with commonly used Bluetooth receivers [5]. Moreover this receiver can be mapped on the HiperLAN/2 receiver.

In our proposed SDR receiver (see figure 2), channel selection of the Bluetooth receiver has been integrated with the frequency offset correction and FFT of the HiperLAN/2 receiver. Also, the HiperLAN/2 QAM demodulator (and FEC decoder) can be combined with the Bluetooth MAP receiver. More information can be found in [5] and [6].

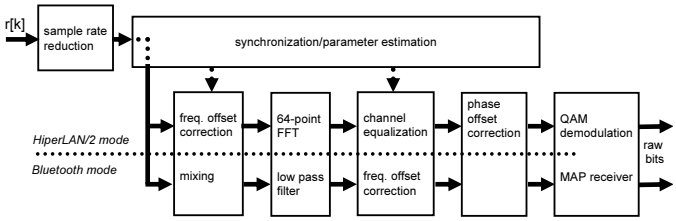

Fig. 2
DIGITAL PART OF A BLUETOOTH-ENABLED HIPERLAN/2 RECEIVER.

B. Real-time demonstrator

The real-time demonstrator consists of two computers (transmitter PC and receiver PC) and two PC boards. This setup is depicted in figure 3. These two PC boards communicate with the computer through a digital I/O $\leftrightarrow$ PCI interface (NuDAQ cPCI-7300A).

All baseband processing in the transmitter is performed by the computer and the baseband output is connected to the DAC PC board. This board contains an FPGA for communication with the computer, two DACs (20 MSPS) and analogue reconstruction filters.

The output of this board can be connected to a signal generator and our analogue front-end for bandpass-signal experiments, see figure 4.

In baseband experiments however, the output of the DAC PC board board is connected to the ADC/SRC PC board. This PC board contains two ADCs (80 MSPS), a Sample Rate Converter (Intersil ISL5416) that decimates the incoming (complex) 80 MSPS to a 20 MSPS signal and an FPGA for communication with the computer. Further

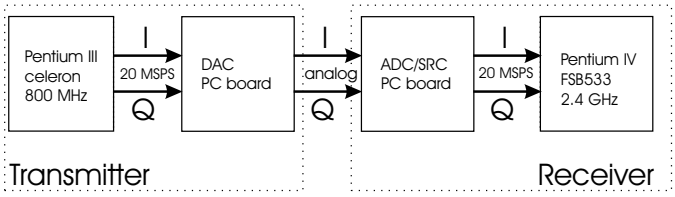

Fig. 3
SETUP OF THE REAL-TIME DEMONSTRATOR (SCENARIO FOR BASEBAND EXPERIMENTS).

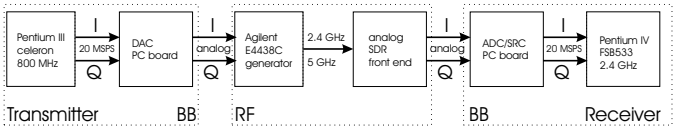

Fig. 4
SETUP OF THE REAL-TIME DEMONSTRATOR (SCENARIO FOR BANDPASS EXPERIMENTS).

signal processing is performed by the CPU of the computer.

We expect that all parts of this demonstrator (hardware and software) will be ready before the end of 2003.

IV. CONCLUSIONS

In this paper we outlined our SDR demonstrator. For this demonstrator we design and implement a wide-band analog front-end, a PCB with SRC/ADC and GPP software.

The combination of wide-band analog front-end and GPP hardware is capable of receiving Bluetooth and HiperLAN/2 signals.

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