# Band Offset Measurements on Ultra-Thin (100) SOI MOSFETs

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***Abstract*— This work shows experimental evidence of structural quantum confinement showing up in the electrical device characteristics through a widening of the band gap. In this work, subthreshold currents in long channel ultra-thin SOI MOSFETs with (100) crystal orientation have been analyzed for various temperatures and different silicon body thicknesses in order to extract shifts in the band edges. Although the offsets in both the valence band and conduction band contribute to the total band gap, this work concentrates on the valence band offset, as the investigated devices are $p$-MOSFETs. Likewise, changes in the conduction band can be measured on $n$-type devices. The valence band edge was found to move downward for decreasing silicon body thickness, corresponding to a widening of the band gap. This implies that devices with an extremely thin semiconductor body exhibit a stronger temperature dependence. Good agreement with theory was observed.**

## I. Introduction

The double-gate (DG) MOSFET [1] and similar devices such as FinFETs [2]–[4] and Gate–All–Around structures are widely recognized as promising candidates for replacing the conventional bulk MOSFETs. In fact, the combination of multiple gates and an extremely thin semiconductor body (i.e., the actual channel) reinforces the gate-induced field effect, thereby improving important device parameters such as suppression of short-channel effects and subthreshold slope. However, when the device dimensions enter the (deca-)nanometer range, quantum effects can no longer be neglected: energy quantization will occur due to carrier confinement in the semiconductor body enclosed between the gate dielectrics [5], referred to as structural confinement. This significantly alters the band structure and, hence, the device characteristics. To be more specific, subbands emerge in the conduction and valence band, thereby effectively increasing the band gap.

From an experimental point of view, we expect that changes in $E_{\mathrm{g}}$ can be observed particularly in the subthreshold current, which can be explained as follows: when flowing from source to drain, charge carriers have to traverse an energy barrier, shown schematically in Fig. 1(a) and (b). This barrier is almost exclusively determined by $E_{\mathrm{g}}$ under low gate bias, hence subthreshold, operation. In effect, changes in the band gap will directly enforce a change in subthreshold current and its temperature dependence.

In this work, we present a procedure to extract shifts in the conduction and valence band edge from temperature dependent subthreshold current measurements on ultra-thin body (UTB) DG MOSFETs. The core of this work has recently been published elsewhere [6]. The present paper shows additional simulation data supporting our earlier findings. Although only results for $p$-type devices are shown, we would like to stress that the presented procedure can as well be applied to $n$-type devices in order to extract shifts in the conduction band edge. In fact, the procedure is similar to the commonly used method for determining the energy barrier in e.g. Schottky diodes and SiGe bipolar transistors [7], [8].

## II. Theory

The subthreshold (diffusion) current $I_{\mathrm{DS}}$ in a long channel device can be expressed as

$$I_{\mathrm{DS}} = \frac{\mu u_{\mathrm{T}}}{L} Q_{\mathrm{i}}(V_{\mathrm{GS}}) \left[1 - \exp\left(-\frac{|V_{\mathrm{DS}}|}{u_{\mathrm{T}}}\right)\right] \qquad (1)$$

with $\mu$ the carrier mobility, $u_{\mathrm{T}}$ the thermal voltage ($kT/q$), $k$ Boltzmann's constant, $T$ the absolute temperature, $q$ the elementary charge, $L$ the channel length, $V_{\mathrm{DS}}$ the drain–source voltage and $Q_{\mathrm{i}}$ the inversion charge density per unit area in the source side of the channel. In relatively thick silicon layers, quantum confinement is negligible while the concept of *volume inversion* [1] still holds. Then, $Q_{\mathrm{i}}$ is essentially uniformly distributed throughout the silicon body and proportional to $t_{\mathrm{Si}}$, for a $p$-type MOSFET given by

$$Q_{\mathrm{i}} = q t_{\mathrm{Si}} N_{\mathrm{V}} \exp\left(\frac{E_{\mathrm{V}} - E_{\mathrm{F}}}{kT}\right) \qquad (2)$$

with $N_{\mathrm{V}}$ the effective density of states (DOS) in the bulk valence band, $E_{\mathrm{F}}$ the Fermi level and $E_{\mathrm{V}}$ the valence band edge. The above expressions employ Boltzmann's approximation which is justified by the low injection condition in subthreshold. In fact, $E_{\mathrm{V}} - E_{\mathrm{F}}$ in Eq. (2) can be expressed in terms of gate bias and material parameters as $\phi_{\mathrm{m}} - (\chi_{\mathrm{s}} + E_{\mathrm{g}}/q) - V_{\mathrm{GS}}$, with $\phi_{\mathrm{m}}$ the gate work function, $\chi_{\mathrm{s}}$ the electron affinity, $E_{\mathrm{g}}$ the band gap and $V_{\mathrm{GS}}$ the gate bias [see also Fig. 1(c)]. This suggests that, for a given gate and drain bias, the difference in gate work function and valence band edge can be extracted from the slope of the drain current versus the inverse temperature, which represents an 'activation energy'.

When $t_{\mathrm{Si}}$ is scaled down, the conduction and valence band will gradually split into subbands due to quantum confinement. However, Eq. (2) shows that in $p$-MOSFETs only the position of the valence band with respect to the vacuum level (i.e., $E_{\mathrm{V}}$) is important. Hence, when measuring $p$-type devices, only changes in the valence band edge can be observed.

Quantization in the valence band is accounted for by replacing '$t_{\mathrm{Si}}N_{\mathrm{V}}$' in Eq. (2) by its quantum mechanical equivalent [9]. Employing the effective mass approximation, this reads

$$\frac{kT}{\pi\hbar^2}\sum_{\mathrm{k,n}} m^*_{\mathrm{d,k}} \exp\left(-\frac{E_{\mathrm{k,n}}}{kT}\right) \tag{3}$$

with

$$E_{\mathrm{k,n}} = \frac{\hbar^2}{2m^*_{\mathrm{z,k}}}\left(\frac{n\pi}{t_{\mathrm{Si}}}\right)^2$$

$m^*_{\mathrm{d,k}}$ and $m^*_{\mathrm{z,k}}$ are the density–of–states and quantization effective masses respectively of valley $k$; $E_{\mathrm{k,n}}$ is the minimum of subband $n$. In effect, occurrence of quantum confinement implies a lower DOS compared to the bulk DOS due to the energy gaps separating the subbands. More important in this case, however, is that the valence band edge moves down in energy, thus effectively widening the band gap. The strong $t_{\mathrm{Si}}$ dependence of the subband minima $E_{\mathrm{k,n}}$ can be exploited to extract the valence band offset by comparing the subthreshold currents of two devices with different $t_{\mathrm{Si}}$, given by

$$\eta_{\mathrm{rat}} = \frac{I_{\mathrm{ref}}}{I_{\mathrm{thin}}} \propto \frac{\mu_{\mathrm{ref}} g(t_{\mathrm{Si,ref}})}{\mu_{\mathrm{thin}} g(t_{\mathrm{Si,thin}})} \cdot \exp\left(\frac{\Delta E_{\mathrm{V}}}{kT}\right) \tag{4}$$

in which $g(\cdot)$ represents the product '$t_{\mathrm{Si}}N_{\mathrm{V}}$', either classically or quantum mechanically depending on $t_{\mathrm{Si}}$; the subscripts 'ref' and 'thin' refer to the quantities corresponding to the reference and thin device respectively. In the following experiments, the reference device has a sufficiently thick layer for quantum confinement to be negligible, thus having the bulk silicon band gap. Then, $\Delta E_{\mathrm{V}}$ is equal to $E_{\mathrm{V,ref}} - E_{\mathrm{V,thin}}$, i.e., the band offset in the thinnest layer referenced to the bulk silicon band edge. Note that Eq. (4) is valid for any combination of $t_{\mathrm{Si}}$'s, provided that the volume inversion condition holds. In the following, we assume that the temperature dependence of $\mu$ and the DOS is approximately equal for both devices. This is, however, is not very critical as the exponential temperature dependence is much stronger than the temperature dependence of the prefactor. Consequently, $\Delta E_{\mathrm{V}}$ is equal to the slope of $\ln(\eta_{\mathrm{rat}})$ versus the inverse temperature.

## III. Results and Discussion

Before proceeding to the actual measurements, some simulation results will be shown to demonstrate that, in general, temperature dependent subthreshold current measurements can be used to extract the energy difference between gate workfunction and valence band edge. The simulations have been done with Atlas from Silvaco [10], in which Poisson's equation, the drift-diffusion and continuity equations were solved with Boltzmann's approximation, employing the classical description of the charge carrier distribution. Fig. 2(a) depicts the simulated subthreshold current in a $p$-type 23 nm device for several temperatures along with the measured curves, showing very good agreement with the experimental data. Furthermore, the weaker slope at elevated temperatures and low gate bias originates from thermal rather than gate induced generation of carriers. Fig. 2(b) shows $\ln(I_{\mathrm{DS}})$ versus the inverse temperature, at a fixed gate bias. The slope of the curve represents the aforementioned 'activation energy' and equals the energy difference between gate work function and valence band edge. For a device with $n^+$-polysilicon gate, hence $\phi_{\mathrm{m}} \approx \chi_{\mathrm{s}}$, this value is close to the band gap energy, as confirmed by the simulations. Repeating this procedure for an $n$-type device results in a value of 30 meV [not shown] which corresponds to the energy difference of the $n^+$-polysilicon gate and the *conduction* band edge.

A TEM image of a typical device is shown in Fig. 3. The devices are long-channel (25 $\mu$m) (100) SOI MOSFETs, on a 400 nm BOX layer, with the back of the wafer serving as back-gate contact. All devices have an $n^+$-poly gate and a front oxide thickness of 25 nm; $t_{\mathrm{Si}}$ ranges from 27 nm down to 5 nm. The device fabrication is documented in [11]. The inset shows a close-up of the channel region for the thinnest available device, revealing that the thickness uniformity of the channel is very high ($\pm 0.5$ nm).

Fig. 4 depicts the temperature dependence of the subthreshold current for two devices with different $t_{\mathrm{Si}}$. The subthreshold swing is -65 mV/dec at 25 °C and increases linearly with temperature in accordance with Eq. (2). This means that no significant side effects occur which affect the device behavior in subthreshold, implying that shifts of the band edges can be reliably extracted from the temperature dependent $IV$ measurements. Furthermore, the ratio of the currents was found to scale more than proportionally with $t_{\mathrm{Si}}$, in contrast to the classical prediction that the subthreshold current scales linearly with $t_{\mathrm{Si}}$ as given by Eq. (2). Besides widening of the band gap, this observation is attributed to a reduced DOS and mobility (shown for strong inversion in [12], [13]).

As given by Eq. (4), $\Delta E_{\mathrm{V}}$ can be extracted from $\eta_{\mathrm{rat}}$ ($= I_{\mathrm{ref}}/I_{\mathrm{thin}}$) versus the inverse temperature for a given gate bias. Hereto, $\eta_{\mathrm{rat}}$ is depicted in Fig. 5(a) for three values of $t_{\mathrm{Si}}$, with a 27 nm device as reference (having the bulk silicon band gap). It clearly demonstrates that $\eta_{\mathrm{rat}}$ of the 19 nm device is essentially constant, whereas the 9 nm and 5 nm device exhibit a nonzero slope, hence a stronger temperature dependence. The slope, or difference in activation energy, is more positive for the thinnest layer and corresponds to a shift of the valence band edge downward in energy. Furthermore, the offset in the current ratio increases for decreasing $t_{\mathrm{Si}}$, pointing to a reduction in DOS and mobility.

The procedure was repeated for all devices and the resulting band edge shifts are depicted in Fig. 5(b), along with the theoretical prediction from Eq. (3) and [9]. The dotted line represents the valence band edge in absence of quantum confinement. The figure shows that $\Delta E_{\mathrm{V}}$ increases for decreasing $t_{\mathrm{Si}}$, in agreement with theory. The scattering is attributed to thickness variation across the wafer, which is estimated to be $\pm 2$ nm. Since the strength of quantum confinement is governed by $t_{\mathrm{Si}}$, the accuracy of the results depends strongly on the determination of $t_{\mathrm{Si}}$, particularly for $t_{\mathrm{Si}}$ around 5 nm and smaller. However, despite the scattering,

the trend is clearly visible. The method described in this work is, in itself, very reliable as shifts of the band edges can be measured separately from transport parameters such as mobility and DOS.

## IV. Conclusion

In this work, shifts in the valence band edge were observed when scaling down the silicon body thickness of thin (100) SOI $p$-type MOSFETs. In effect, an offset of the valence band edge results in a wider band gap, making the subthreshold current stronger dependent on the temperature. The band offsets were extracted from temperature dependent subthreshold current measurements and were found to increase for decreasing silicon body thickness, showing good agreement with theory. Furthermore, the experimental procedure allows for extracting shifts in the conduction and valence band edges, separately from other $t_{\mathrm{Si}}$ dependent transport parameters such as the mobility and density of states.

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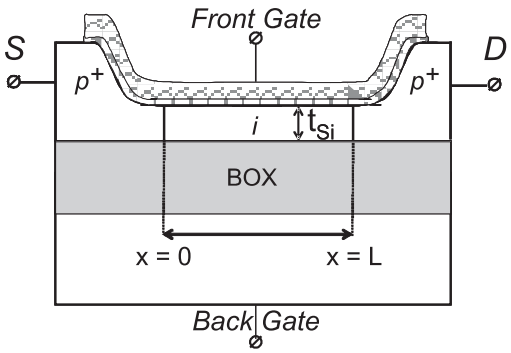
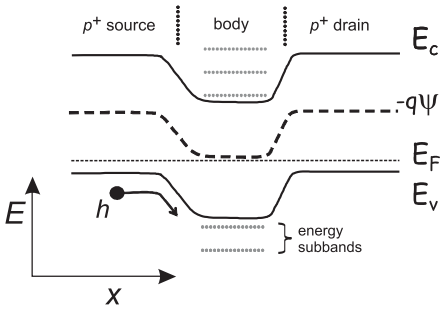



(a)

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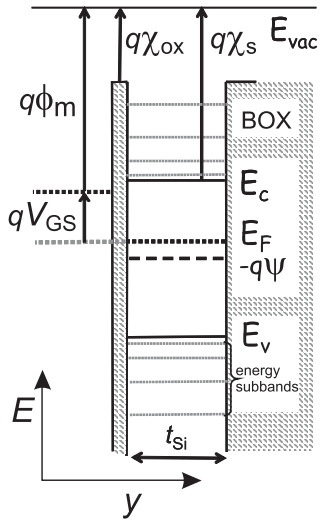
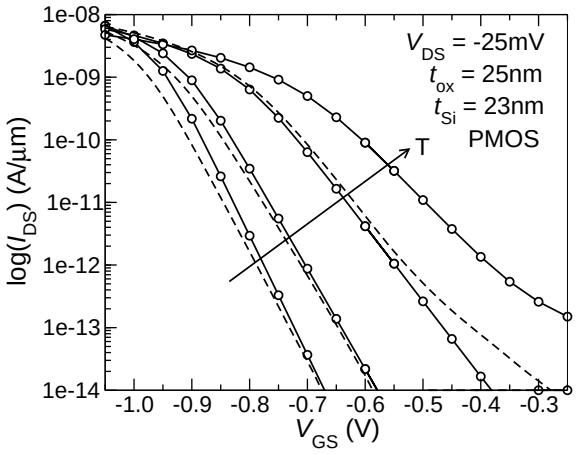
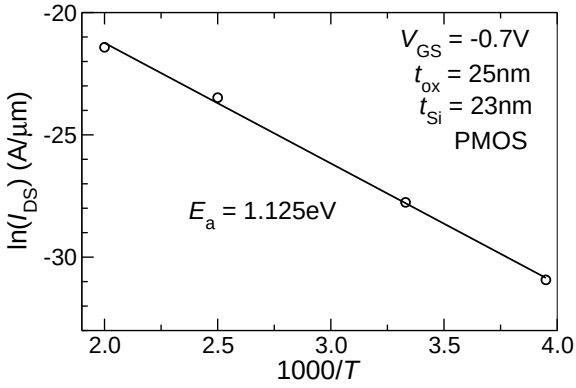



(c)

Fig. 1. (a) Schematic cross-section of the investigated long-channel $p$-type (100) SOI DG MOSFET; $t_{\mathrm{Si}}$ denotes the silicon body thickness. (b) Schematic band diagram lateral to the gate, showing the discrete energy levels originating from carrier confinement in the thin silicon body; $E_{\mathrm{F}}$ is the Fermi level, $E_{\mathrm{C}}$ and $E_{\mathrm{V}}$ are the bulk conduction and valence band edge respectively and $\psi$ is the potential. (c) Band diagram perpendicular to the gate; $V_{\mathrm{GS}}$ is the gate–source voltage, $E_{\mathrm{vac}}$ is the vacuum level; $\chi_{\mathrm{ox}}$ and $\chi_{\mathrm{s}}$ are the electron affinity of $SiO_2$ and Si resp.; $\phi_{\mathrm{m}}$ is the gate work function.




(a)




(b)

Fig. 2. (a) Simulated (solid lines) and measured (dashed lines) subthreshold current at T = 253 K, 300 K, 400 K and 500 K for a device with $t_{\mathrm{Si}}$ 23 nm, showing good agreement. The subthreshold swing increases linearly with temperature. (b) $\ln(I_{\mathrm{DS}})$ versus the inverse temperature at $V_{\mathrm{GS}} = -0.7$ V, with corresponding activation energy of 1.125 eV.

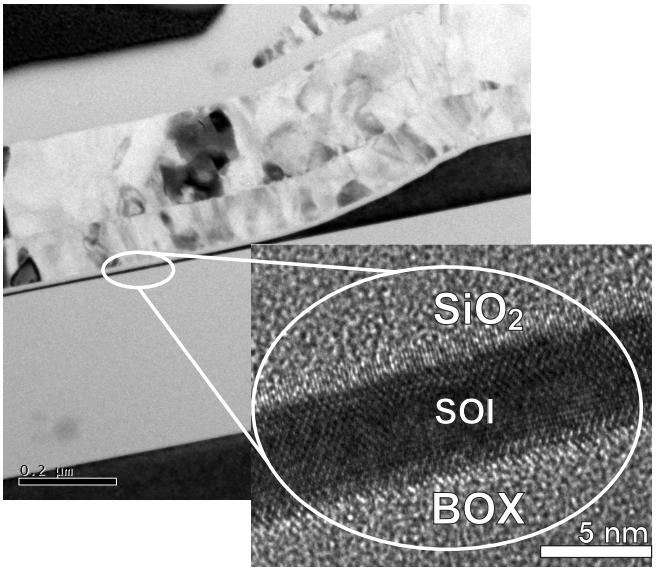



Fig. 3. TEM image of the investigated PMOS on a 400 nm BOX layer. The inset shows a detailed image of the 5 nm thick channel region; the typical channel uniformity is approximately $\pm 0.5$ nm. The device fabrication is described in [11].

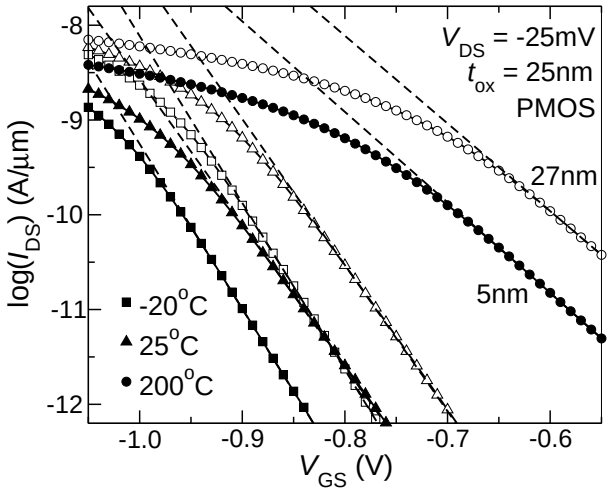



Fig. 4. Subthreshold characteristics of the thickest (27 nm, open symbols) and thinnest (5 nm, filled symbols) available PMOS devices, shown for various temperatures. The devices were operated in double gate mode by sweeping the front and back gate simultaneously at equal voltage. All devices have sufficiently thin channels to ensure volume inversion, given subthreshold operation [1], [14]. The ratio of the currents in the thickest and thinnest devices ($\eta_{\rm rat}$) decreases with temperature (-20 °C: 12.3; 25 °C: 11.5; 200 °C: 6.6). The dashed lines have been used to extract the subthreshold slope from the measured data.

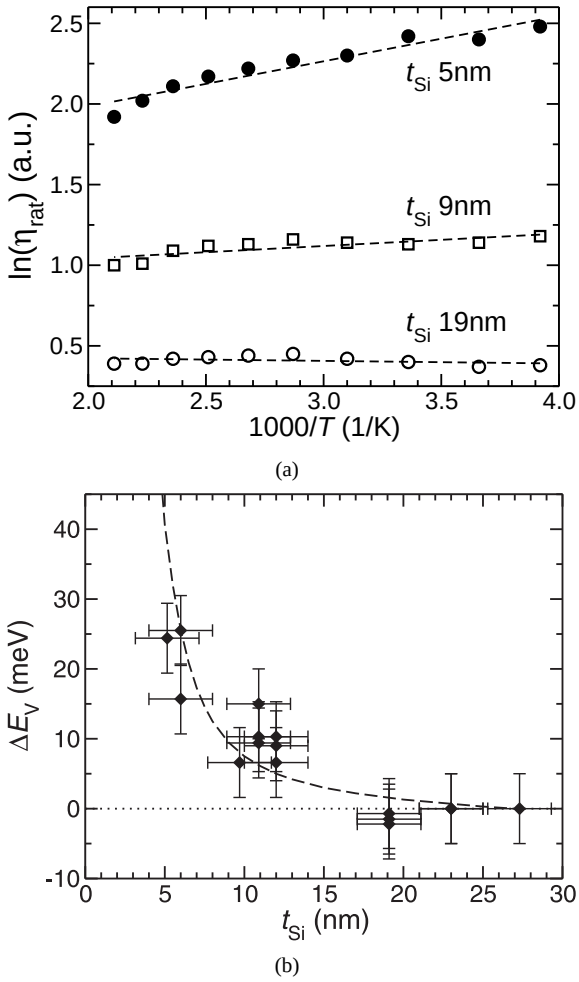



Fig. 5. (a) $\eta_{\rm rat}$ ($= I_{\rm ref}/I_{\rm thin}$) for three values of $t_{\rm Si}$, with the 27 nm device as reference; the slope clearly increases for decreasing $t_{\rm Si}$, corresponding to $\Delta E_{\rm V} > 0$. (b) Valence band offset vs. $t_{\rm Si}$ extracted from the slope of $\eta_{\rm rat}$. The observed scattering can be attributed to the limited thickness uniformity across the wafer, which shows a larger variation ($\pm 2$ nm) than the channel uniformity within one device ($\pm 0.5$ nm). Most $t_{\rm Si}$ values have been determined with TEM analysis, whereas the error bars have been determined with ellipsometry measurements on several reference layers to account for the uncertainty in $t_{\rm Si}$ across the wafer. The error in $\Delta E_{\rm V}$ is estimated to be $\pm 5$ meV, obtained from the observed spread in the measurements on devices with equal specified channel thickness. The dashed line is the theoretical $\Delta E_{\rm V}$, obtained from Eq. (3) and [9].