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FREQUENCY DIVIDER

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Abstract of WO2006016312 (A1)

A frequency divider comprising, a first latch circuit (10) and a second latch circuit (10'), the second latch circuit (10') being crossed-coupled to the first latch circuit (10). Each latch (10; 10') comprises a respective sense amplifier coupled to a respective latch (11). The sense amplifiers comprise a first clock input for receiving a first clock signal (f, f) and 5 respective complementary first clock signal having a first frequency. The latches (11) comprise a second clock input (2f; 2f) for receiving a second clock signal and respective complementary second clock signal having a second frequency, the second frequency being substantially double the first frequency.