2016 International

Integrated Reliability Workshop

Handout: Welcome ◇ Schedule ◇ Maps ◇ Attendees

Stanford Sierra Conference Center
S. Lake Tahoe, California
October 9-13, 2016

Sponsored by
the IEEE Electron Devices Society and
the IEEE Reliability Society

Advancing Technology
For Humanity

2016 IEEE INTERNATIONAL INTEGRATRED RELIABILITY WORKSHOP

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welcome

As the General Chair of the 2016 International Integrated Reliability Workshop, it is my pleasure to welcome you to this year's meeting.

After a long journey to the conference, we will be please to continue the Sunday night tradition with a “techlite” lecture. Tom Malzbender a 31-year veteran of Hewlett Packard Labratories will present on “Imaging the Antikythera Mechanism,” an ancient analog computer used to predict astronomical positions. We look forward to Tom sharing his imaging expertise.

Monday, after the superb breakfast provided by the staff of the Stanford Sierra Camp, the technical program of the workshop begins starting the keynote speaker. This year we have the privilege to listen to Bruce Doris from IBM. Bruce has work extensively in the area of exploratory devices and he will speak to the title “Opportunities for 5nm Node CMOS Technology and Beyond.”

This year's technical program committee, led by Dr. Tom Kopley from ON Semiconductor, has put together a wonderful program. With invited and contributed speakers that cover a wide range of reliability related topics like advanced physical characterization techniques, BEOL and FEOL reliability, memory, and much more.

The tutorial program has been organized by Dr. Suresh Uppal and Dr. Steve Ramey and includes 7 tutorial lectures from world renowned experts. The tutorials are spread throughout the duration of the conference and provide a great introduction to the more specialized talks.

Monday and Wednesday evenings include poster sessions, organized by Dr. Dave Estrada and Dr. Pat Lenahan. The poster sessions are a great way to interact with the authors and discuss their research and findings. The Hors d’oeuvres and drinks make these intellectual conversations very enjoyable and a favorite of many attendees.

Both Tuesday and Wednesday evenings are spent in discussion groups, another great tradition of IIRW, organized by Dr. Stanislav Tyaginov and Dr. Jim Lloyd. These sessions are centered on hot reliability topics and all attendees are welcome and encouraged to actively participate. These discussion groups provide a forum where ideas and problems are explored openly by the group and moderated by the discussion group leaders. Please sign up for the respective DG’s as early as possible to allow for good preparation.

Wednesday afternoon provides an open schedule for everyone and is a highlight for many attendees. The area around the Stanford Sierra Camp is amazing and offers many adventures so grab another attendee or join a group to explore the area. A hike through Desolation Wilderness is wonderful and the view from Mt Tallac is breath taking. Before your hike make sure you fill out a permit at the front desk. There are many return attendees that know the area and will be hiking so feel free to join them. You can also relax at the camp, go for a boat ride or brave the cold water with a swim in the lake. There is no shortage of activities at this wonderful area.

I would like to take this time to thank all the members of the IIRW management and technical program committee. IIRW is a volunteer run workshop and without the many hours spent by these people IIRW would not be possible. I have enjoyed working with them and I am proud of the work they have done to make IIRW a success. I am also grateful to our Major Patron, Mentor Graphics and our Supporting Patron IBM as well as the sponsorships of the IEEE Electron

Devices Society and Reliability Society. The contributions of these organization is very much appreciated and helps make IIRW possible.

Finally, I would like to thank the 2016 IIRW attendees for their contribution and attendance. Without your often yearlong support of IIRW the workshop would not be possible. I attended IIRW for the first time in 2004 as a grad student and have attended every year since then except one due to the birth of my son. IIRW has shaped my career and I can say without it I would not be where I am today. I have met what I consider dear friends at IIRW have started collaborations with many of them and it has opened many doors for me. I sincerely hope that you will profit from your attendance as much as I have.

Enjoy the workshop,

Richard Southwick
2016 IIRW General Chair

2016 IIRW Technical Program Committee

Chair: Tom Kopley, ON Semiconductor
Vice-Chair: Luca Larcher, University of Modena

Name	Affiliation
Andreas Aal	Volkswagen
Brad Bittel	Intel
Christian Schlünder	Infineon
Dave Estrada	Boise State U.
Ennis Ogawa	Broadcom
Gabriel Lansbergen	TSMC
Jacopo Franco	IMEC
Jason Campbell	NIST
Jason Ryan	NIST
Jean Yang-Scharlotta	NASA JPL
Jeff Gambino	ON Semiconductor
Jim Lloyd	SUNY Poly Albany, CNSE
Koji Eriguchi	Kyoto University
Matt Ring	ON Semiconductor
Matthew Hogan	Mentor Graphics
Michael Dammann	Fraunhofer Institute
Nagarajan Raghavan	SUTD
Partha Chakraborty	Freescale
Patrick Lenahan	Penn State Univ.
Peter Moens	ON Semiconductor
Pragya Shrestha	NIST
Stanislav Tyaginov	TU of Vienna
Steve Ramey	Intel
Suresh Uppal	GlobalFoundries
Susanna Reggiani	University of Bologna
Yuuichiro Mitani	Toshiba
Zakariae Chbili	Globalfoundries
Ziyuan Liu	Riken

2016 IEEE International Integrated Reliability Workshop

PROGRAM SCHEDULE

SUNDAY, October 9 Please have lunch before arriving at the camp; no lunch will be served at the camp.

3:00-6:00 p.m.	Registration: Pick up badges, electronic handout, and attendee gift; Discussion Group and SIG Signup (*Lodge Lounge*)
3:00-10:00 p.m.	Lodge check-in: Get room assignment (prearranged) & room key. (If physically challenged please notify desk of special needs.)
6:00-7:30 p.m.	DINNER (*Dining Room*)
7:30-8:30 p.m.	**Sunday Night Tutorial** (*Angora Room*) Imaging the Antikythera Mechanism—Tom Malzbender, Malzbender Consulting
8:30-10:00 p.m.	Social (*Old Lodge*)

MONDAY, October 10

7:00-8:00 a.m.	BREAKFAST (*Dining Room*)
	Plenary Session (*Angora Room*)
8:00-8:10 a.m.	Welcome & Introduction—General Chair: Richard Southwick, IBM
8:10-8:20 a.m.	Technical Program Overview—Tom Kopley, ON Semiconductor
8:20-9:20 a.m.	**Keynote:** Opportunities for 5 nm Node CMOS Technology and Beyond—Bruce Doris, IBM
	Session #1 (*Angora Room*) — **Advanced Characterization 1,** Chair: Pat Lenahan, Penn State
9:20-9:50 a.m.	1.1 **(INVITED)** Advances in imaging and quantification of electrical properties at the nanoscale using Scanning Microwave Impedance Microscopy (sMIM)—Stuart Friedman, Prime Nano Inc.
9:50-10:20 a.m.	Coffee and Snack Break
10:20-11:25 a.m.	**Tutorial # 1:** Oxide Defects in Emerging Technologies: Characterization and Mitigation—Dmitry Veksler, NIST
	Session #2 (*Angora Room*) **—Memory and Circuit Reliability,** Chair: Luca Larcher, Univ. of Modena and Reggio Emilia
11:25-11:50 a.m.	2.1 BTI variability of SRAM cells under periodically changing stress profiles—Kay-Uwe Giering, Fraunhofer IIS/EAS
12:00-1:00 p.m.	LUNCH (*Dining Room*)
1:00-1:05 p.m.	Announcements (*Angora Room*)
1:05-1:35 p.m.	2.2 **(INVITED)** AC Stress and STD cell aging characterization to enhance reliability coverage of logic circuits—Kevin Huang, TSMC
1:35-2:05 p.m.	2.3 **(INVITED)** Novel characterization techniques providing reliable and low-power Flash NOR memory operations—Jean Coignus, CEA-LETI
2:05-2:30 p.m.	2.4 The Sources of Erase Voltage Variability n Split-Gate Flash Memory Cell Arrays—Yuri Tkachev, Silicon Storage Technology
2:30-3:10 p.m.	Coffee and Snack Break
	Session #3 (*Angora Room*) **— MEMS,** Chair: Tom Kopley, ON Semiconductor
3:10-4:45 p.m.	**Tutorial #2:** MEMS Reliability—Allyson Hartzell, Veryst Engineering
4:50-5:10 p.m.	Discussion Group Overview (*Angora Room*)
5:10-6:00 p.m.	Poster Setup (*Cathedral Room*), Chair: Dave Estrada, Boise State; Vice-Chair: Pat Lenahan, Penn State
6:00-7:30 p.m.	DINNER (*Dining Room*)
7:30-9:00 p.m.	**Poster Session** (*Cathedral Room*), Chair: Dave Estrada, Boise State; Vice-Chair: Pat Lenahan, Penn State
9:00-10:00 p.m.	Social (*Old Lodge*)

TUESDAY, October 11

7:00-8:00 a.m.	BREAKFAST (*Dining Room*)
8:00-8:05 a.m.	Announcements (*Angora Room*)

Session #4 (*Angora Room*) — **Defects,** Chair: Stanislav Tyaginov, TU Vienna

8:05-8:35 a.m.	4.1 **(INVITED)** RTN analysis as a tool to link physical device characteristics to electrical reliability in nanoscale devices—Francesco Puglisi, Univ. of Modena and Reggio Emilia
8:35-9:00 a.m.	4.2 On the distribution of the FET threshold voltage shifts due to individual charged gate oxide defects—Gerhard Rzepa, IMEC
9:00-10:05 a.m.	**Tutorial #3:** Ab initio modeling of defects in SiO_x and HfO_2 for reliability predictions—Al-Moatasem El-Sayed, UCL
10:05-10:35 a.m.	Coffee and Snack Break

Session #5 (*Angora Room*) — **Silicon MOSFET Reliability,** Chair: Steve Ramey, Intel

10:35-11:00 a.m.	5.1 Time Dependent Junction Degradation in FinFETs—Tzung Yu Ho, TSMC
11:00-11:25 a.m.	5.2 Layout Dependent Effect: Impact on device performance and reliability in recent CMOS nodes—Cheikh Ndiaye, STMicroelectronics/IM2NP-ISEN
11:25-12:00 p.m.	Group Picture (*Flag Pole*)
12:00-1:00 p.m.	LUNCH (*Dining Room*)
1:00-1:05 p.m.	Announcements (*Angora Room*)

Session #6 (*Angora Room*) — **High Voltage Devices,** Chair: Zakariae Chbili, GlobalFoundries

1:05-2:10 p.m.	**Tutorial #4:** SiC MOSFET Reliability – A Similar Elephant but with Different Spots—Kevin Matocha, Monolith Semiconductor
2:10-2:40 p.m.	6.1 **(INVITED)** SiC Power Device Reliability—Don Gajewski, Wolfspeed/Cree
2:40-3:10 p.m.	6.2 **(INVITED)** Reliability of power devices—Gaudenzio Meneghesso, Univ. of Padova
3:10-3:40 p.m.	Coffee and Snack Break
3:40-4:10 p.m.	6.3 **(INVITED)** The Elegant Complexity of a Simple Capacitor: Revisiting the Reliability Physics of Thick Insulators—Asraf Alam, Purdue
4:10-4:35 p.m.	6.4 Hot carrier degradation improvement for high voltage n-channel LDMOS in BCD technology—Jifa Hao, ON Semiconductor
4:35-5:40 p.m.	**Tutorial #5:** Process Induced Damage (PID): Challenges and Overview—Andreas Martin, Infineon
6:00-7:30 p.m.	DINNER (*Dining Room*)
7:30-8:30 p.m.	**Discussion Groups:** Chair: Stanislav Tyaginov, TU Vienna, and Jim Lloyd, SUNY Polytech (60 minute parallel sessions for each topic.) Attendees are to participate in one of the groups.
8:30-10:00 p.m.	Social (*Old Lodge*)

WEDNESDAY, October 12

7:00-8:00 a.m.	BREAKFAST (*Dining Room*)
8:00-8:05 a.m.	Announcements (*Angora Room*)

Session #7 (*Angora Room*) — **Advanced Characterization 2,** Chair: Ricki Southwick, IBM

8:05-8:35 a.m.	7.1 **(INVITED)** Reliability of electronic devices: nanoscale studies based on the conductive atomic force microscope—Mario Lanza, Suzhu U.
8:35-9:40 a.m.	**Tutorial #6:** Scalpel SPM toward the three-dimensional characterization of confined volumes—Umberto Celano, IMEC

Session #8 (*Angora Room*) — **Self-Heating,** Chair: Gavin Hall, ON Semiconductor

9:40-10:05 a.m.	8.1 Self-Heating Confounds, Correlates, and Redefines Front and Backend Reliability of Modern Surround Gate Transistors—Ashraf Alam, Purdue
10:05-10:30 a.m.	Coffee and Snack Break
10:30-10:55 a.m.	8.2 Self-Heating impact on TDDB in bulk FinFET devices: Uniform vs Non-uniform Stress—Zakariae Chbili, GlobalFoundries

Session #9 (*Angora Room*) — **TDDB,** Chair: Andreas Aal, Volkswagen

10:55-11:20 a.m.	9.1 A Physical Manifestation of Interfacial Roughness Pitfalls in Assessing Dielectric TDDB Lifetimes—Lieyi Sheng, ON Semiconductor
11:20-11:45 a.m.	9.2 Fast TDDB for Early Reliability Monitoring—Charles Larow, Gobalfoundries
12:00-1:00 p.m.	LUNCH (*Dining Room*)
1:00-6:00 p.m.	Open—The afternoon is free for discussion, hiking & other recreation. All attendees are required to be back before dark.
6:00-7:30 p.m.	DINNER (*Dining Room*)
7:30-8:30 p.m.	**Poster Session** (*Cathedral Room*), Chair: Dave Estrada, Boise State; Vice-Chair: Pat Lenahan, Penn State

8:30-9:30 p.m.	**Discussion Groups:** Chair: Stanislav Tyaginov, TU Vienna, and Jim Lloyd, SUNY Polytech (60 minute parallel sessions for each topic.) Attendees are to participate in one of the groups.

THURSDAY, October 13

7:00-8:00 a.m.	BREAKFAST (*Dining Room*)
8:00-8:05 a.m.	Announcements (*Angora Room*)
	Session #10 (*Angora Room*) **— Harsh Environments,** Chair: Jean Yang-Scharlotta, JPL
8:05-8:35 a.m.	10.1 **(INVITED)** Automotive system level reliability dependence on semiconductor capabilities and market dynamics — Andreas Aal, Volkswagen
8:35-9:05 a.m.	10.2 **(INVITED)** Reliability-performance evaluation for scaled multi-materials device stacks—Gennadi Bersuker, The Aerospace Corp.
	Session #11 (*Angora Room*) **— Back End of Line,** Chair: Jean Yang-Scharlotta, JPL
9:05-10:10 a.m.	**Tutorial #7:** Scaling and Variability Challenges to Advance Node BEOL Reliability—Patrick Justison, Globalfoundries
10:10-10:40 a.m.	Coffee and Snack Break / Check Out of Room
10:40-11:05 a.m.	11.1 Effect of Texture and Elastic Anisotropy of Copper Microstructure on Reliability—Adarsh Basavalingappa, SUNY Polytech
11:05-11:30 a.m.	**DG Summary / SIG Report / Wrap-up**
12:00-1:00 p.m.	LUNCH (*Dining Room*) & then the Workshop Ends—Attendees must leave the Stanford Sierra Camp

Poster Presentations (not including Walk-in Posters)

Refereed Posters

RP01	V_{th} is Dead – Long Live the Threshold Voltage—T. Hillebrand, M. Taddiken, K. Tscherkaschin, S. Paul, and D. Peters-Drolshagen (Univ. of Bremen)
RP02	Humidity and polarity influence on MIM PZT capacitor degradation and breakdown—J. Wang, C. Salm, E. Houwman, M. Nguyen, and J. Schmitz (Univ. of Twente)
RP03	Reliability of integrated resistors and the influence of WLCSP bake— S. Jose, J. Bisschop, V. Girault, L. v. Marwijk, J. Zhang, and S. Nath (NXP Semiconductors)
RP04	AC TDDB Analysis for Circuit-Level Gate Oxide Wearout Reliability Assessment—T. E. Kopley, K. O'Brien, and W.-C. Chang (ON Semiconductor)
RP05	1/f Noice Analysis of Hafnium Oxide based ReRAM Devices Using AC+DC Measurement Technique—N. Mahmud, A. J. Narasimham, and J. R. Lloyd (SUNY Polytechic Institute)
RP06	Intrinsic Reliability Characterization for Stand-Alone MEMS Switch Technology—E. M. Ceccarelli, J. Browne, C. Heffernan, P. Fitzgerald (Analog Devices)
RP07	Improved Analysis of NBTI Relaxation Behavior Based on Fast I-V Measurement—D. Nouguier, G. Ghibaudo, M. Rafik, X. Federspiel, and D. Roy (STMicroelectronics/Univ. Grenoble Alpes)
RP08	Increasing Velocity of Wafer Level Reliability Characterization: Novel Approaches and Limitations—B. Bittel, S. Vadlamani, S. Ramey, and S. Padiyar (Intel)
RP09	Study of Off-State Hot-Carrier Degradation and Recovery of NMOSFET in SWD Circuits of DRAM—K. G. Kim, D. Sun, S. J. Rhe, I. G. Kim, H. Hwang, K.Y. Cho, G. Y. Jin, and I. S. Chung (Samsung/Sungkyunkwan U.)

LN01 On the Effect of Interface Traps on the Carrier Distribution Function During Hot-Carrier Degradation—S. E. Tyaginov, A. Makarov, M. Jech, J. Franco, P. Sharma, B. Kaczer, and T. Grasser (TU Vienna/Ioffe Inst./IMEC)

Open Posters

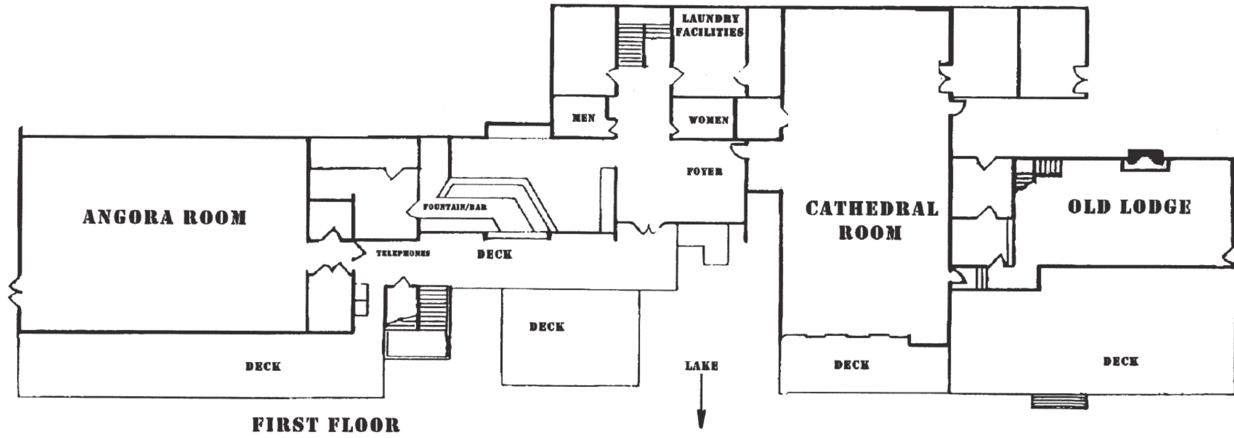
OP01 High and Low Volume Practices and Approaches to Semiconductor Reliability—J. Siddiqui, J. Ortega, B. Albus, and S. Hihath (DMEA)

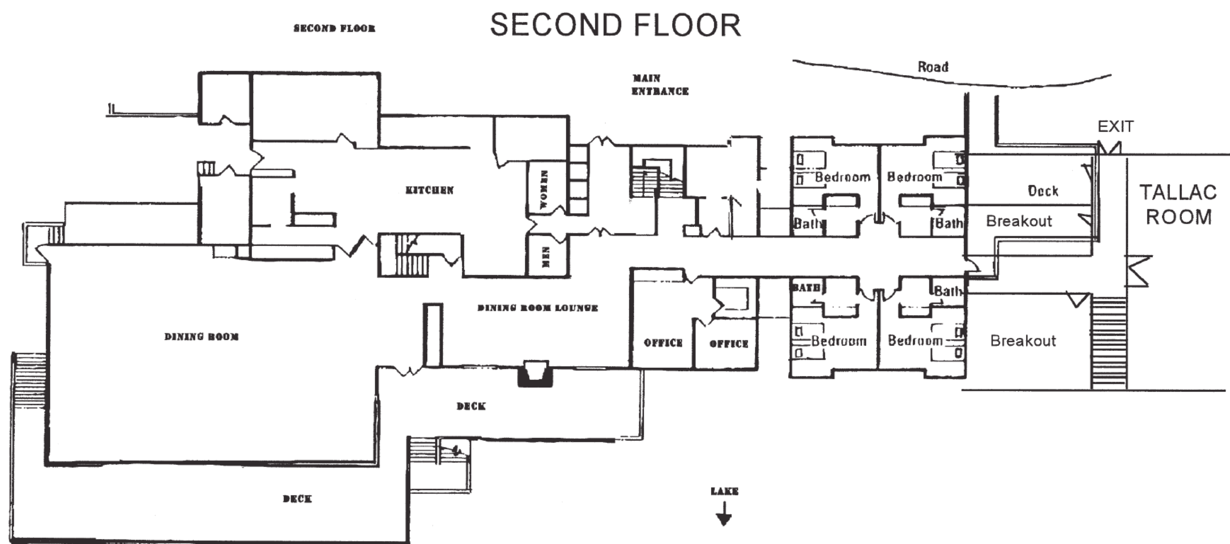
OP02 Reliability Characterization Strategy for a Thick Copper Metallization—M. Pohl, M. Erstling, V. Hein, and P. Lammert (X-Fab)

LN02 Radiation Induced Leakage Currents in Dense and Porous Low-k Dielectrics—R. J. Waskiewicz, M. J. Mutch, P. M. Lenahan, and S. W. King (Penn State U./Intel)

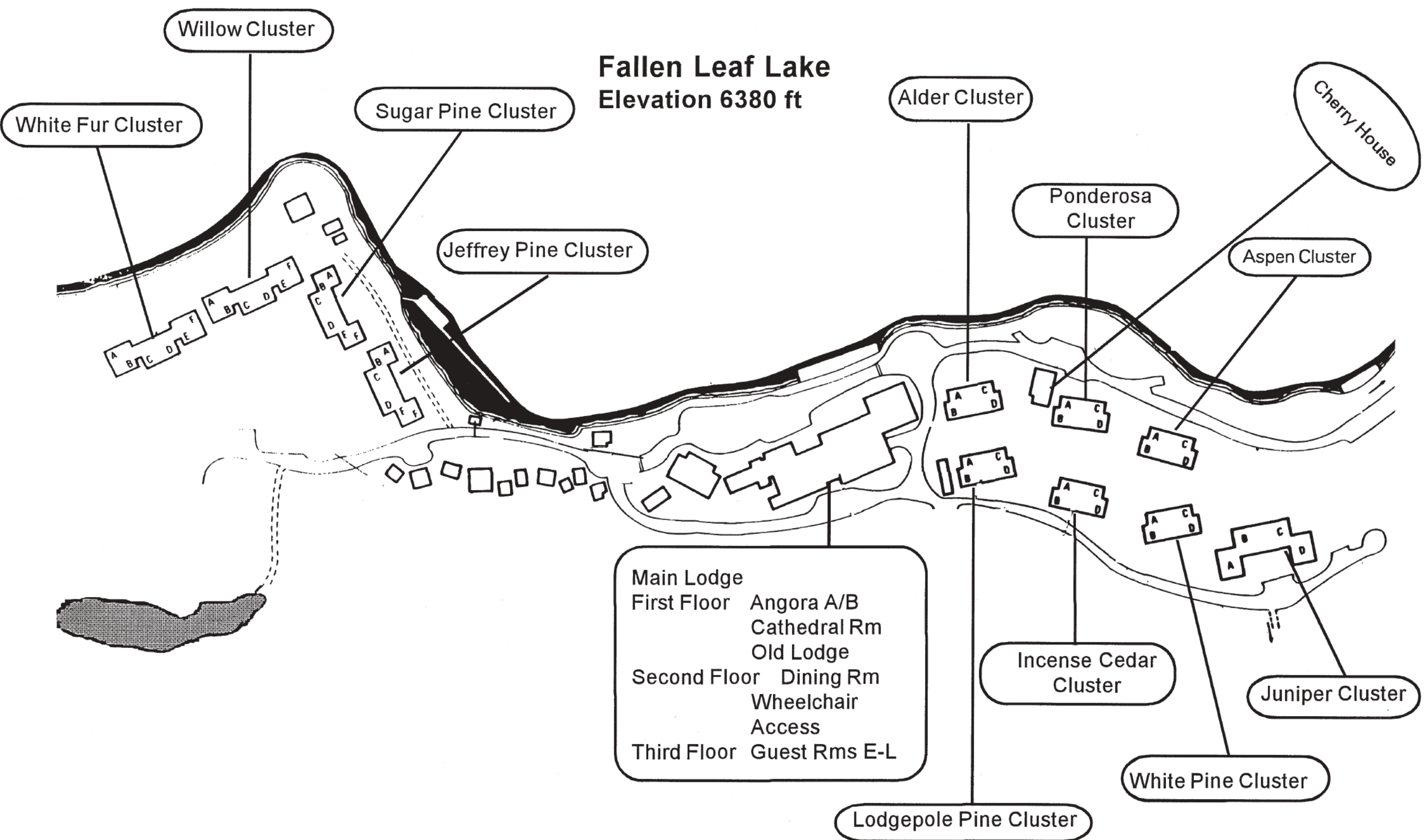
LN03 Bias Temperature Instability and Its Correlation to Flicker (1/f) Noise in FinFETs—Y. M. Ding, K. Misra, and P. Srinivasan (NJIT/GlobalFoundries)

Main Lodge Map





Stanford Sierra Camp Map



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Reliability continues to be a significant concern and challenge for IC designers at all process nodes. Extensive research and simulation has been done to characterize the behavior of interconnect and devices and account for degradation over time. Of particular importance is the ability to apply the results of these findings to full-chip verification, in an easy-to-use and repeatable manner, while validating reliability best practices during the IC development process. Calibre® PERC™ is a reliability verification platform that extends verification beyond "traditional" DRC, LVS and ERC. By understanding the design from a topological perspective, focused checks can be performed to ensure compliance. This capability has been used in many areas, and has been very successful in validating ESD structures and enforcing design methodology rules. The native point-to-point (P2P) resistance, current density (CD), and electromigration (EM) simulation capabilities enable interconnect reliability verification and study. We are actively researching and investigating ways to provide superior solutions to the reliability community in these areas. Calibre PERC is the first industry tool able to fulfill these complex verification requirements. For more information, please contact matthew_hogan@mentor.com or visit our webpage:

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