Preserving Polar Modulated Class-E Power Amplifier Linearity under Load Mismatch

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***Abstract*— Power amplifiers (PAs) need digital predistortion (DPD) linearization to handle high-order complex modulation schemes in next-generation communication systems. While load variation is inevitable, DPD is generally designed considering only the nominal load impedance for PAs. This paper presents a polar class-E PA with an on-chip waveform characterizer enabling adaptive digital predistortion (ADPD) to preserve the linearity of the PA under load mismatch. The presented ADPD corrects both AM/AM and AM/PM distortions, which are prominent in the demonstrated PA, while simultaneously correcting for slow memory effects without the need for complex memory DPD algorithms. Load-pull measurements demonstrate that target error vector magnitude (EVM) and adjacent channel power ratio (ACPR) can be maintained in a significantly larger area on the Smith chart going from 50 Ω optimized static DPD to our ADPD for a 2 GHz 1024 QAM signal with 1 MSym/s symbol rate.**

***Keywords*— CMOS integrated circuits, power amplifiers, linearity, distortion, predistortion, impedance, antennas, adaptive control, quadrature amplitude modulation.**

I. Introduction

Modern wireless communication devices use high-order complex modulation schemes like 1024 QAM. These signals have a high peak to average power ratio (PAPR) and impose stringent linearity requirements on the power amplifiers (PAs). Given the large share of power consumed by the PAs in a communication system, highly efficient switched-mode PAs are attractive. However, due to inherent efficiency-linearity trade-offs [1], digital predistortion (DPD) becomes necessary for these PAs to meet linearity requirements [2], [3] of increasing order complex modulation schemes.

The antenna impedance depends on the electromagnetic environment of the antenna and therefore vary over time [4]. In switched-mode PAs, load mismatch from the nominal 50 Ω load detunes the resonant network. For class-E PAs, this degrades the output power, efficiency, linearity and also jeopardizes the reliability [5]. For a *polar* class-E PA, this translates to variation in AM/AM and AM/PM characteristics, which renders 50 Ω optimized static DPD ineffective under load variation [6].

Previous works use various techniques to preserve PA linearity under load mismatch. These can be categorized into methods that keep the PA load impedance at its nominal value, and methods that deal with PA load variation. Implementations of the former methods are presented in [7], [8]. In [7], an adaptive tunable matching network (TMN) ensures the nominal load for the PA and thereby preserves linearity under antenna mismatch conditions. However, TMNs are

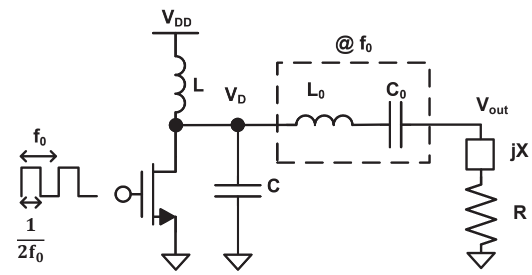


Fig. 1. Schematic representation of a single-ended class-E PA.

lossy, bulky and hence not suitable for easy integration in ever-miniaturizing CMOS integrated circuits. A solution with similar disadvantages is the addition of circulators or isolators with the PA. In [8], a phase detector at the collector of the PA combined with a controlled phase shifter at the output are used. The increase in size and high driving voltage prevents the above approach from being practically integrated into the latest CMOS technology. Implementation of the latter method is described in [9], where a peak detector at the collector of the PA combined with an adaptive feedback control loop to tune the input drive signal is used. However, such a system improves linearity at the cost of transmitted power because it reduces the input drive level. Another way to deal with load-dependent non-linearity is to implement DPD for different loads and select the suitable DPD setting using load impedance estimation. For class-E PAs, to the best of the authors' knowledge, there is no work focusing on integrated adaptive linearity improvement under severe load mismatch.

We present a proof-of-concept polar class-E PA with an integrated waveform characterizer, which allows the implementation of fully automated adaptive digital predistortion (ADPD) to preserve the linearity of a PA under load mismatch, aiming at 1024 QAM modulation.

In section II, the linearity of polar class-E PA under load mismatch is discussed. In section III, the principle of adaptive preservation of PA linearity with the integrated waveform characterizer and implementation of the system are discussed. The measurement results demonstrating the effectiveness of the system under load mismatch are presented in section IV. Conclusions are summarized in section V.

II. Linearity of a polar class-E PA under load mismatch

Fig. 1 depicts a single-ended (non-polar) class-E PA where the MOSFET operates as a switch driven by a 50 %

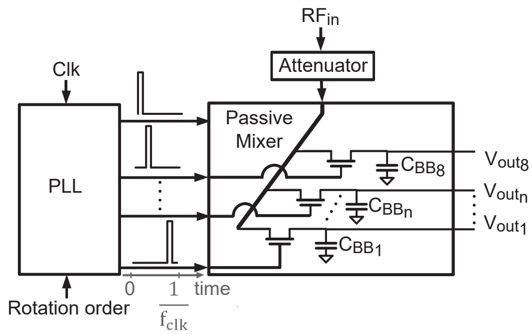


Fig. 2. Block diagram of RF waveform characterizer.

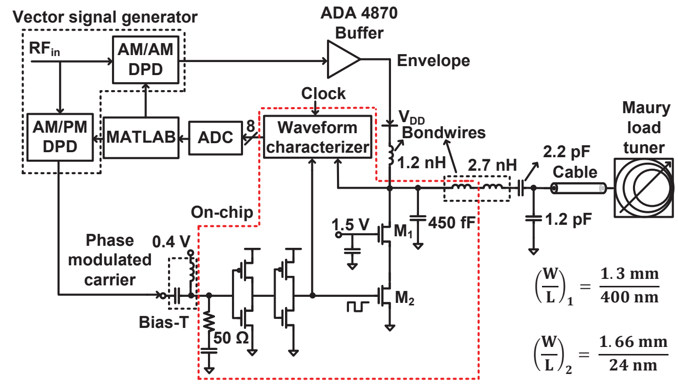


Fig. 3. Schematic of the implemented polar class-E PA with ADPD using the integrated waveform characterizer.

duty cycle square wave with a frequency f_0. The LC tank shapes the switch's drain voltage waveform V_D, and the L_0C_0 resonant tank ensures that the output current is sinusoidal with frequency f_0. A matching network (not in Fig. 1) transforms the antenna impedance to the PA's load impedance: Z_L = R+jX. Voltage V_D depends on both the real and imaginary parts of Z_L [5]. This Z_L-dependent switch voltage translates to Z_L-dependent magnitude and phase of the first harmonic of the output voltage signal of the class-E PA.

In communication systems, the PA must handle modulated signals. In this paper, we aim at 1024 QAM. To deal with complex modulated signals, the class-E PA can be used in outphasing or polar configuration; we use the latter.

In polar modulated class-E PA, distortions are due to AM/AM and AM/PM conversions. AM/AM represents the non-linear relation between the modulated supply voltage V_{DD} and the amplitude of the output RF signal V_{out}. AM/PM is V_{DD}-dependent phase modulation of V_{out}. Any change in Z_L leads to a change in the class-E PA's switch voltage waveform and consequently leads to Z_L-dependent AM/AM and AM/PM characteristics. Other causes of AM/AM and AM/PM conversions in a polar class-E PA include feedthrough of the drive voltage of the switch via its relatively large gate-drain capacitance, non-zero on-resistance of the switch, and drain-bulk junction capacitance of the switch [10]. Note that the feedthrough signal is only phase modulated and hence has a wide bandwidth. Therefore, it leads to broadening of the output spectrum, increasing the adjacent channel power ratio (ACPR). The cascode PA topology minimizes the effect of the feedthrough signal.

III. Demonstration of ADPD with Polar Class-E PA

We present a polar class-E PA with an on-chip RF waveform characterizer that enables ADPD to correct AM/AM, AM/PM distortions, temperature changes and slow memory effects as the load changes.

A. *Waveform Characterizer*

The RF waveform characterizer is based on the work in [11]. Fig. 2 shows the block diagram of this waveform characterizer. It can measure up to three harmonics of an RF signal up to a fundamental frequency of 3 GHz. Hence, the waveform characterizer can be used for ADPD in PAs with operating frequencies up to 3 GHz; we target 2.4 GHz for demonstration.

The (internal) drain voltage signal in class-E PAs is harmonic rich. These harmonics are filtered by series L_0C_0 tank and external matching network to obtain fundamental harmonic at the output. Therefore, any feedback system operating on an *internal* PA signal must estimate the magnitude and phase of the first harmonic of the transmitted signal.

Using conventional loopback systems, harmonic rejection quadrature mixers are needed to obtain the magnitude and phase of first harmonic. A sufficiently accurate harmonic rejection quadrature mixer at RF frequency is difficult to achieve [2].

Our characterizer mixes the RF waveform using an N-path approach and produces 8 quasi-DC samples per period of the RF waveform. These 8 samples are input to ADCs, the output of which is processed in a computer running MATLAB. The waveform characterizer uses the (unmodulated) carrier frequency as the clock signal: an extra clock is not required and the phase information of the measured signal can be obtained. An 8-point discrete fourier transform (DFT) is performed in MATLAB to get the magnitude and phase information of the three harmonics of the sampled RF signal. In such systems, accuracy is generally limited by sample timing inaccuracies which in this case is mainly due to delay mismatch in a 4-stage differential inverter ring oscillator inside the phase-locked loop (PLL). To significantly enhance the accuracy of sampling, statistical properties of the delay mismatches are exploited to cancel the impact of delay spread [11]. The characterizer consumes 3 mW power under continuous operation at 2 GHz.

B. *Adaptively Preserving PA Linearity*

Fig. 3 presents the schematic of the polar modulated PA employing ADPD. For the ADPD, the input and output signal of the PA are required. The transmitted data is known in a transmitter while the waveform characterizer samples the modulated data at the drain of the switch. The DFT yields magnitude and phase information of the first 3 harmonics in the drain voltage signal; the fundamental harmonic is used for ADPD. Magnitude and phase data are compared with the corresponding transmitted magnitude and phase data derived

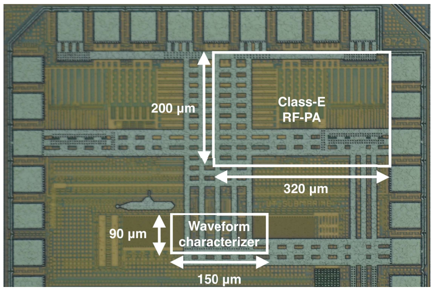


Fig. 4. Chip microphotograph.

from IQ data transmitted by the vector signal generator (VSG) to generate AM/AM and AM/PM correction signals. For flexibility, signal processing is done on a computer running MATLAB. The correction signals are then input to the lookup table (LUT) based DPD inside the VSG. The VSG outputs the predistorted envelope and phase signals for the polar class-E PA. The loop is executed periodically making the PA linearity robust against any relatively slow process that impacts linearity.

The time constant of the waveform characterizer is $\tau = 16$ ns. For 40 dB accuracy, 5τ is required which makes the effective settling time of the characterizer 80 ns. Hence the maximum symbol rate measured by the waveform characterizer is 12.5 Msym/s. Transmitted and the sampled data are read from a mixed-signal scope in blocks. Reading one block takes 0.65 s; reading data from 8 channels requires 5.2 s. The bottleneck for effective sample rate in our demonstration is due to latency while reading data. Antenna environment changes on a time scale of ms [12]. Removing data latency bottleneck can reduce the response time of the complete system to order of ms making the system adapt to changes on a ms time scale such as temperature changes, slow memory effects [13] and antenna impedance variations.

C. Implementation

The chip includes a single-ended cascode class-E PA and the RF waveform characterizer fabricated in 22 nm FDSOI CMOS technology packaged in QFN 40; Fig. 4 shows the microphotograph. The PA occupies 0.064 mm^2 area, and the waveform characterizer occupies 0.014 mm^2 area. The PA is designed for zero voltage switching and zero slope switching conditions at frequency f_0 = 2.4 GHz. The peak-power frequency is shifted to 2 GHz from the target 2.4 GHz, which may be due to the bondwires at the PA output. The component values for the designed PA are shown in Fig. 3. The 1.2 nH inductor is implemented using bondwires; the parasitic capacitance of the MOSFET is included in the 450 fF capacitor. Two cascaded inverters are used as switch driver ensuring hard switching of the switch transistor. The input of the on-chip waveform characterizer is connected to the drain of switch and the outputs of the characterizer are fed to MATLAB through ADCs. The predistorted input signal is fed to the PA through an R&S SMW200A VSG. An ADA 4870 IC implements the envelope tracking buffer for the demonstrator.

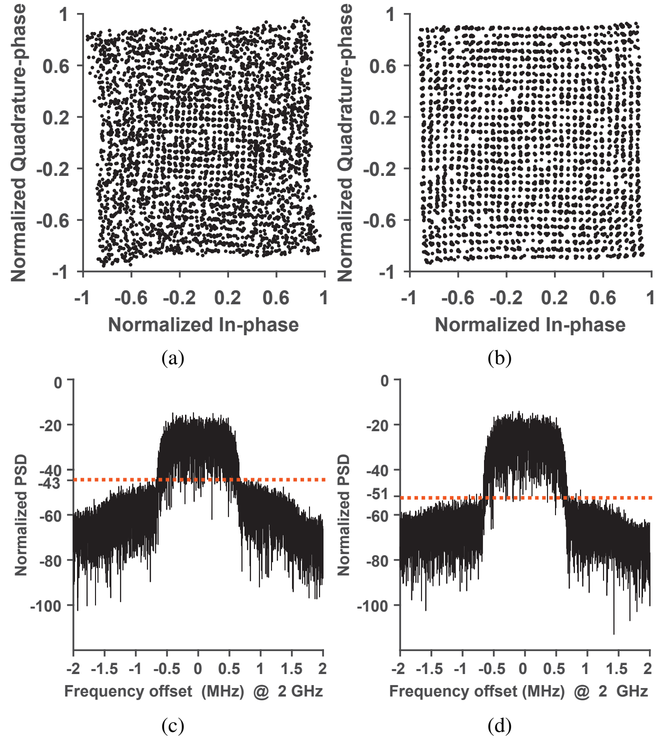
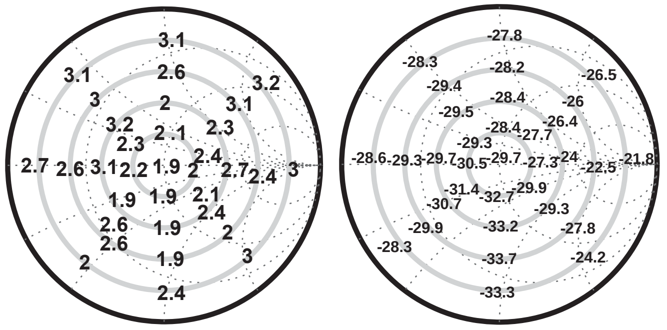


Fig. 5. Measured performance for a 1 MHz 1024 QAM signal at 2 GHz at 50 load. Normalized symbol constellation (a) before DPD, (b) after DPD. Normalized output power spectral density (c) before DPD, (d) after DPD.

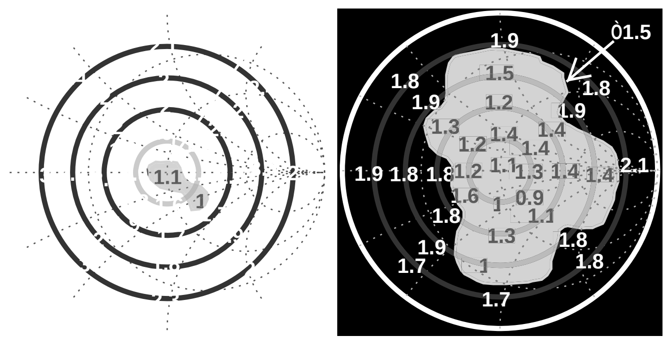
IV. MEASUREMENTS

Single carrier modulated signal measurements are performed on the polar class-E PA to demonstrate linearity preservation using the presented ADPD under load mismatch. A 1024 QAM signal at 1 MSym/s symbol rate with pseudo-random bit sequence (PBRS) 23, pulse-shaped using root-raised cosine filter with a roll-off factor 0.35 and decomposed into the envelope and phase-modulated carrier at frequency 2 GHz are generated using the VSG. 400 symbols are used to construct AM/AM and AM/PM correction signals. Load-pulling is performed with a Maury load-pull tuner for voltage standing wave ratio (VSWR) up to 9:1. The PA is operated at 15 dB back-off for the nominal load condition to avoid breakdown during load-pull [5] while no class-E tuning for reliability [14] is done in this work to focus only on the linearity. Fig. 5 (a), (b) show the normalized output symbol constellation and (c), (d) the normalized output power spectral density (PSD) before and after DPD, respectively at 50 Ω load. Fig. 6 (a) and (b) show the Smith charts of EVM (%) and ACPR (dB) of the polar class-E PA without any DPD. Fig. 7 (a) and (b) show Smith charts of EVM (%) up to VSWR 9:1 with 50 Ω optimized static DPD and with ADPD, respectively. The EVM is normalized to root mean squared (RMS) power. The EVM standard for 1024 QAM signal is considered 1.5 %. The load-pull Smith charts without DPD, with 50 Ω optimized static DPD and with ADPD include a shaded area for which EVM 1.5 %. A significant increase in area under the shaded region can be observed from no



(a) (b)

Fig. 6. Load-pull measurements for VSWR up to 9:1 without DPD with a 1 MHz 1024 QAM signal at 2 GHz. (a) EVM (%), (b) ACPR (dB).



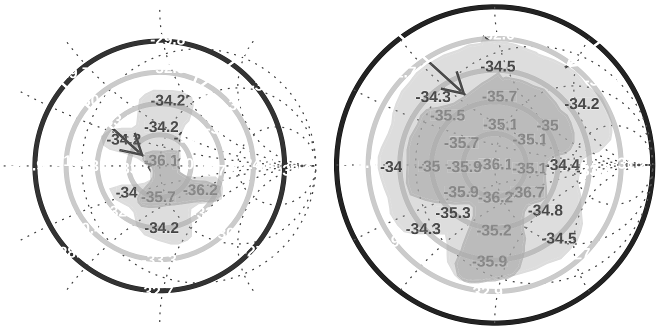
(a) (b)

Fig. 7. Load-pull measurements of EVM (%) for VSWR up to 9:1 with a 1 MHz 1024 QAM signal at 2 GHz. (a) after 50 optimized static DPD, (b) after ADPD.

DPD to 50 Ω optimized static DPD to ADPD. Fig. 8 (a) and (b) show Smith charts of ACPR (dB) up to VSWR 9:1 with 50 Ω optimized static DPD and with ADPD, respectively. For ACPR calculation, the higher and lower adjacent channel bandwidth is considered to be 1 MHz each. The centers of adjacent channels are situated at an offset of 1.35 MHz from the carrier frequency. The ACPR Smith charts show the area covered for values -34 dB and -35 dB for all three cases: without DPD, with 50 Ω optimized static DPD and with ADPD. Similar to the Smith chart showing EVM, there is a significant increase in area under the shaded region for ACPR -34 dB and ACPR -35 dB from no DPD to 50 Ω optimized static DPD to ADPD.

V. Conclusion

The linearity of high-efficiency class-E PAs can be drastically compromised in the presence of load mismatch. We presented a single-ended polar class-E PA with an on-chip integrated waveform characterizer, in 22 nm FDSOI CMOS technology to implement ADPD. For VSWR up to 9:1 when the PA is excited with a 1 MHz 1024 QAM RF signal at 2 GHz, we showed that using our ADPD system sufficiently low EVM and ACPR values can be maintained across a relatively large area on the Smith chart compared to that when using a static (50 Ω optimized) DPD. The ADPD system can be used to optimize performance for relatively slow processes such as antenna load variation, temperature variation, and slow



(a) (b)

Fig. 8. Load-pull measurements of ACPR (dB) for VSWR up to 9:1 with a 1 MHz 1024 QAM signal at 2 GHz. (a) after 50 optimized static DPD, (b) after ADPD.

memory effects. This system allows practical application in next-generation mobile communication systems with complex modulation schemes that demand stringent linearity and are subjected to inevitable load mismatch.

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