Anomalous Scaling of Parasitic Capacitance in FETs with a High-K Channel Material

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***Abstract*—We investigate the operation of FETs with a high-K channel material, $SrTiO_3$ ($K = 300$). The transistors show low-leakage, high-capacitance operation with a sub-nm equivalent oxide thickness, in line with expectations. In depletion however, the gate-source capacitance appears to have an unusual 1/3-power dependence on the device length and width. This awkward scaling behaviour is analyzed in detail in this paper and possible consequences for $SrTiO_3$ devices and related 2D-material transistors are discussed. It is argued to relate to the high-permittivity channel. This high permittivity is further experimentally shown to result in strong short-channel effects in 10-μm-long FETs, in spite of the highly scaled equivalent oxide thickness, when the operation temperature is lowered to 4.2 K.**

I. Introduction

In the search for new types of field-effect transistors, a wide variety of two-dimensional channel materials is actively researched. Among the many possible materials, the class of complex oxides holds much promise for their wide variety of physical properties [1], which in principle can be combined at will by interfacing them with other materials of the same class [2]. To make use of these unique physical properties in electronic devices requires the development of advanced device fabrication techniques and of deep understanding of how these properties affect the device operation.

Here, we investigate the operation of field-effect transistors based on such a complex-oxide material, strontium titanate ($SrTiO_3$). At room temperature, $SrTiO_3$ has a dielectric constant (K) of 300 [3], a factor 25 higher than that of silicon. Undoped $SrTiO_3$ is a band insulator with a band gap of 3.3 eV, but the deposition of selected other insulators on top induces a conducting region at the oxide-oxide interface. This region can host a very high 2D charge carrier density (exceeding 10^{14} cm^{-2}), giving rise to a gate-tunable superconducting state at cryogenic temperatures [4], [5], [6], and can be tuned through a metal-insulator transition [7], which could enhance transistor operation, especially improving the subthreshold swing.

II. Device Structure

In our devices, the metal-oxide-semiconductor stack consists of Au-$LaAlO_3$-$SrTiO_3$, in which the $LaAlO_3$ dielectric has a nominal thickness of 1.5 nm (sample A) and of 5.6 nm (sample B). A cross section of the stack of sample A is presented in Figure 1, showing a high crystallinity of the dielectric and a highly disordered 'dead' layer forming at the Au-$LaAlO_3$ interface. The latter increases the physical layer thickness of the dielectric effectively by 0.8 nm to about 2.3 nm. The physical distance between the gate charge and the 2DEG is probably even larger as the charges presumably reside deep inside the $SrTiO_3$ substrate [8]. We argue this to be the origin of the low gate leakage current in our devices. Figure 2 presents the current-voltage characteristics of a representative device on sample A, with $W = L = 10$ μm. All other measured devices (>20 FETs on two identically fabricated, different samples) display similar behavior with ON/OFF ratios of 10^2 to 10^4, subthreshold swings of 80 to 110 mV/dec and threshold voltages of -1 to -0.6 V; all at room temperature.

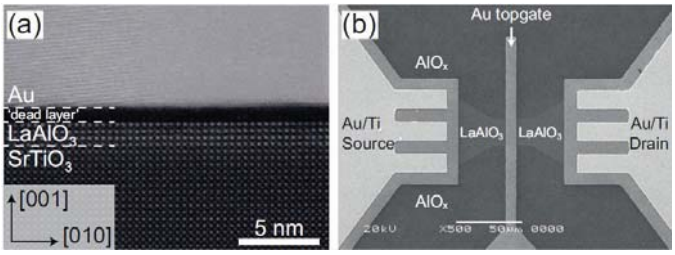

Fig. 1. (a) High-Angle Annular Dark Field (HAADF) Scanning Transmission Electron Microscopy (STEM) image taken along the [100] direction of a $SrTiO_3$-$LaAlO_3$-Au stack. (b) Scanning Electron Micrograph (SEM) of a FET with width, $W = 20$ μm and length, $L = 10$ μm, and indications of the source, drain and (top)gate contacts.

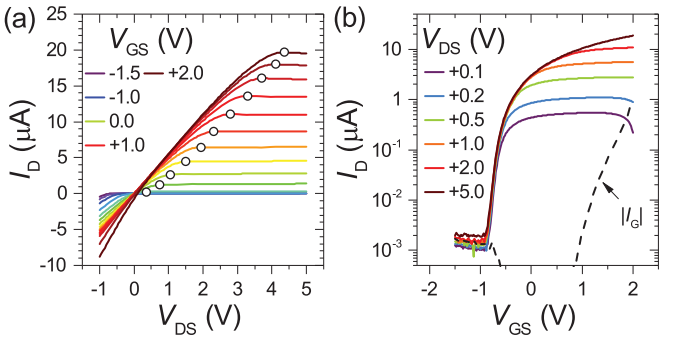

Fig. 2. Current-voltage characteristics of a FET with $L = W = 10$ μm. (a) Drain current, I_D, versus drain-source voltage, V_{DS}, with 250-mV steps in the gate-source voltage, V_{GS}. The open symbols separate the ohmic and saturation regimes for each V_{GS}. (b) Transfer curves for varying V_{DS}, and the gate current (dashed line) for $V_{DS} = 0$ V.

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III. Capacitance-Voltage behaviour

In this work, our main focus is on the gate-source capacitance of these FETs, as a function of gate voltage and device dimensions. As can be observed in Figure 1(b), the device design was limited by materials science considerations (the materials involved are hard to pattern into structures) and not for high-quality $C(V)$ measurements. Especially the long leads are problematic as they give rise to series resistance.

This, and the relatively high channel resistance in inversion, reduces the optimal frequency for the capacitance measurement [9], which in this case was about 10 kHz. The $C(V)$ measurements were carried out using a Keithley 4200-SCS parameter analyzer with a 4210 capacitance-voltage unit, using an ac voltage of 25 mV, inside a shielded probe station. The chuck is grounded, but it is separated from the active device by an insulating substrate of 500 μm $SrTiO_3$ and therefore not further considered in this work.

The conductance of the gate insulator, g_P, was determined by numerical differentiation of the $I_G(V_{GS})$ curve as shown in Figure 2(b). We measured the modulus, $|Z|$, and phase, θ, of the impedance and extracted C_P and R_S as a function of the applied gate bias using the calculated g_P and following Ref. [9].

For the same device as in Figure 2, the thus extracted parameters are plotted in Figure 3 as a function of gate voltage. The $C(V)$ measurement in Figure 3(a) shows that, below threshold, the capacitance of all our devices is at a constant low value, in good agreement with previous reports [10]. Below V_{th} no inversion channel exists, and contrary to semiconductor-based FETs, the depletion layer extends all the way through the substrate. Therefore, any capacitance measured between gate and source (or gate and drain) in depletion must be fringe capacitance. It should be emphasized that, compared to a more conventional semiconductor device, the substrate permittivity is very high and therefore coupling between gate and source or drain is more prominently through the substrate.

On sample A, this depletion capacitance increases monotonously with L and W. However, the scaling is in a highly unusual manner: fitting a power law to the data yields a dependence of $(W \times L)^{1/6}$ for devices with $W = L$. On the contrary, the inversion capacitance, C_{GS}, measured at $V_{GS} = 0.5$ V, does not follow a power law. Only after subtraction of the depletion capacitance, we find the expected linear dependence of the capacitance on device area. Therefore, we interpret this corrected value to be the capacitance between the metal gate and the channel and the depletion capacitance to represent solely parasitic (or stray) contributions to the capacitance. From the area scaling of this "channel capacitance" in Figure 4, we extract a capacitance per unit area of about 32 mF/m^2; this value corresponds to an equivalent oxide thickness (EOT) of 0.96 nm, which is the first reported sub-nm EOT for any complex-oxide based FET.

Sample B was processed to investigate the gate-source capacitance further, as a function of W and L independently.

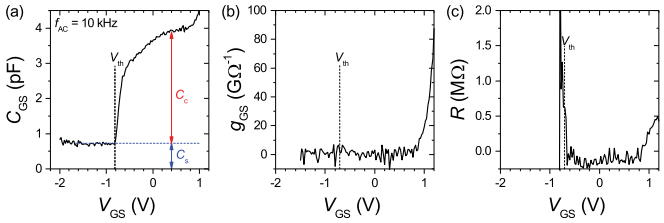

Fig. 3. Extracted parameters from a $Z-\theta(V_{GS})$ measurement across the Au-$LaAlO_3$-$SrTiO_3$ stack, with $f = 10$ kHz: (a) Capacitance, C_{GS} (b) Shunt conductance, g_{GS} (c) Series resistance, R. Above $V_{GS} \approx 0.9$ V, g_{GS} starts to increase sharply due to gate leakage; hence, the values for C_{GS} and R become inaccurate. In (a), we indicate the extraction of the voltage-dependent and -independent contributions to the capacitance, for the scaling analysis in Figure 4(a).

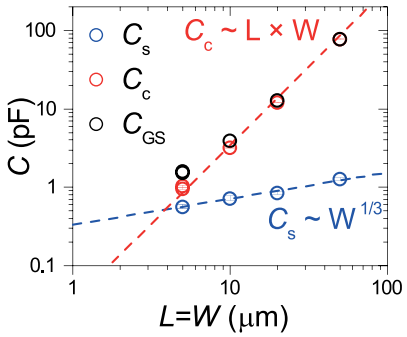

Fig. 4. Scaling of inversion capacitance, C_{GS}, channel capacitance, C_c, and depletion capacitance, C_s, with device dimensions on sample A, for devices with $L = W$. Dashed lines are power-law fits to the data for C_c and C_s.

Devices with common gates were designed with a wide range of lengths and widths as specified in Table I. The $LaAlO_3$ thickness was chosen somewhat higher than for sample A, at 15 unit cells (5.6 nm), in order to further suppress the gate leakage which simplifies the data analysis.

The well-behaved trend of C_S as shown in Figure 4 does not reappear on sample B. In fact, only a very weak correlation between depletion capacitance and gate area can be seen in the raw data as collected: see Figure 5. The inversion capacitance of the same devices also shows a huge scatter. A yield problem was suspected and therefore a rigorous analysis was conducted on a subset of devices in order to find an objective criterion that distinguishes "good" from "defective" devices. The analysis showed that the source and drain contacts are ohmic and reproducible, but do create a significant series resistance in the 10^5 Ω range. However, the gate contact is not reliable; some devices are not connected, others are poorly connected. Using $I-V$ measurements, good devices can be

TABLE I
Designed lengths and widths of the transistors on sample B.

Dimension	Value (μm)
Width W	2, 3, 4, 5, 7, 10, 15, 20, 30, 50, 80, 100, 150, 200, 300
Length L	2, 3, 4, 5, 7, 10, 15, 20, 50, 100, 150, 200

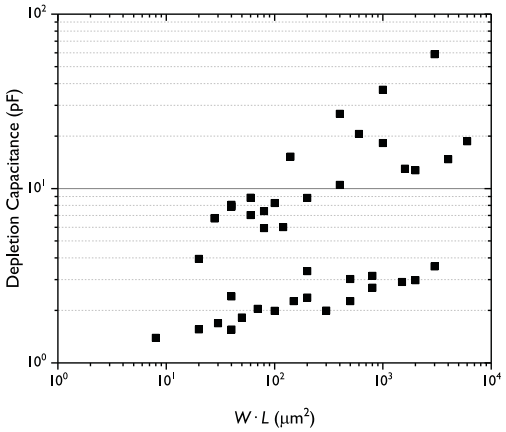

Fig. 5. Gate capacitance in depletion for devices with a wide variety of W and L on sample B.

recognized through their subthreshold characteristic; a device with a (partly) missing gate does not turn off. Because the devices are connected with common gates, this manufacturing problem (probably related to etching of gold in a buffered KI solution) affects more devices than would be strictly necessary when each device would have its own gate contact pad.

A subset of "good" devices delivers a more consistent trend in both the inversion and the depletion capacitance. Figure 6 shows these data. As in the earlier experiment, abnormal area scaling is observed.

To investigate the scaling behavior in more quantitative terms, it is important to correct for offsets in W and L due to the fabrication process. We define the effective channel length as:

$$L_{\text{eff}} = L - \Delta L \tag{1}$$

and similar for W. The gate length offset ΔL can be determined in several ways. From SEM inspection and line resistance measurements we find $\Delta L \approx 2\ \mu$m. Source-drain resistance measurements on devices with a designed length of 2 μm (i.e. no gate is present) and varying width indicate a width offset of $\Delta W \approx$ -2 μm on sample B.

The length scaling in these devices can be qualitatively understood as follows. Were the substrate of low permittivity, then negligible stray capacitance connects the gate through the depleted substrate to the source and drain. But the higher the K, the stronger this coupling becomes. As a result, at short gate lengths a longer gate will exhibit more capacitive coupling to source and drain than a shorter one. This is indeed visible in Figure 6 for the gate lengths until 10–20 μm. For longer channels, the distance between the center of the gate and the source/drain regions becomes so large that the additional coupling is negligible. The gate-to-source capacitance then tends to saturate towards some length-independent limit value. Finite-element simulations could be used to further quantify this effect.

Concerning the width dependence, again the high permittivity plays a role. Fringe capacitance occurs laterally outside the device area as sketched in top view in Figure 7.

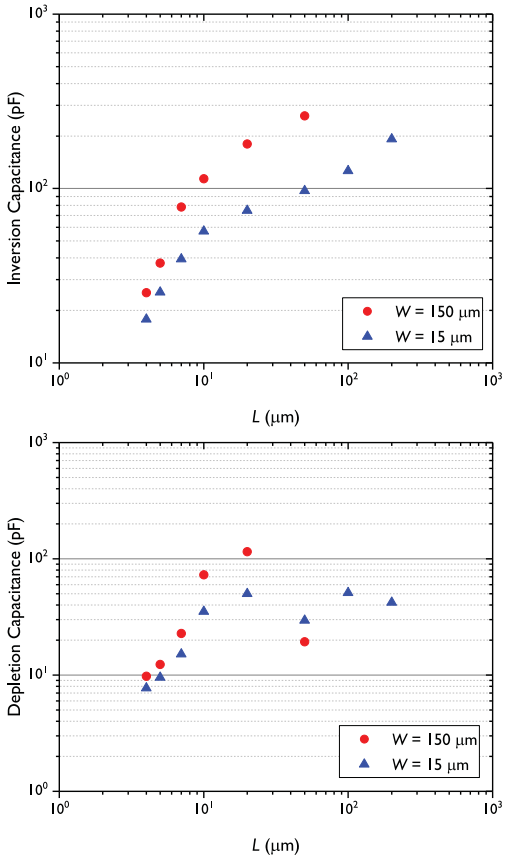

Fig. 6. Inversion (top) and depletion (bottom) capacitance of a subset of known good devices from sample B.

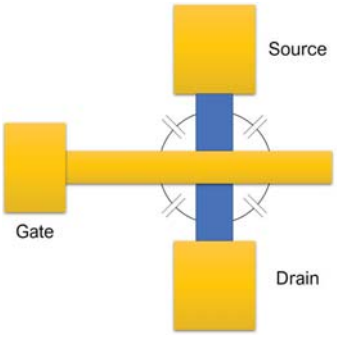

Fig. 7. Top view sketch of the device layout, indicating the gate-to-source and gate-to-drain stray capacitance contributions. These parasitic capacitances can be substantial with a high-K substrate.

The effect of a ten times larger W has only little effect on the overall measured capacitance (see Figure 6). We assume that the length scale of the lateral parasitic capacitance between gate and source/drain is similar to that of the gate coupling mentioned above. Then, the effective width of a 15-μm device in terms of capacitance should be corrected not only for ΔW but also for this lateral parasitic, of the order of 10-20 μm on both sides of the devices. The effective width then becomes several tens of micrometers larger, explaining the small difference of a factor 2–3 between the W = 15 μm

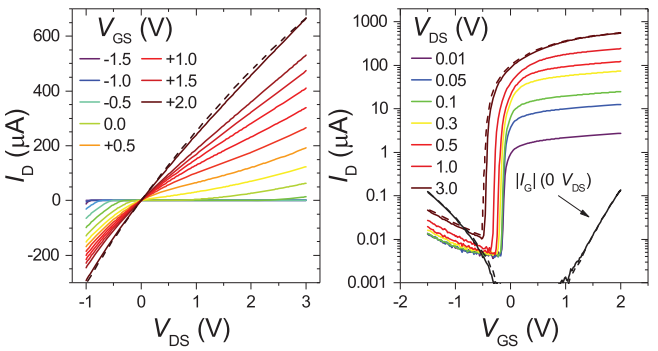

Fig. 8. Low-temperature current-voltage characteristics, measured at $T = 4.2$ K. (a) Drain current, I_D, as a function of drain-source bias, V_{DS}, for varying gate-source voltage, V_{GS}. All sweeps taken with increasing V_{DS}, except the dashed line. (b) Drain current versus gate-source voltage for varying V_{DS}. The black lines indicate the gate current I_G for a drain-source bias of 0 V.

and $W = 150$ μm capacitances in Figure 6.

IV. Short Channel Effects

Short-channel effects should be more prominent in a higher-K channel material. Although this follows from the generalized scaling theory [11] it remains actual in literature for various reasons, both in experimental work [12] and in TCAD simulations [13]. Because the dielectric constant of $SrTiO_3$ increases strongly with decreasing temperature [3], we measured the $I(V)$ characteristics of the same device as Figure 2 at $T = 4.2$ K, where $K \approx 24000$. (It should be noted that in absence of dopant freeze-out, the Debye length does not change much with temperature because the product $\varepsilon_r T$ remains roughly constant.)

Compared to the room-temperature curves, Figure 8 shows no saturation regimes in the V_{DS} sweeps; furthermore, the threshold voltage decreases monotonously with increasing V_{DS}. These are the signatures of drain-induced barrier lowering (DIBL) [14], indicating that our FET is in the short-channel regime, despite the channel length of 10 μm. Given that the gate insulator thickness in this device is already scaled to subnanometer EOT, this finding implies that the high permittivity of $SrTiO_3$ leads to an inherent scaling limitation in the 10-μm channel length range.

V. Conclusion

The use of a high-K channel material has considerable effects on transistor operation as shown in this paper. We find that in these materials, it is especially important to quantify the parasitic components of the measured capacitance to properly determine device characteristics, for example the equivalent oxide thickness. In our devices, the thus extracted parasitic capacitance scales in an unusual way with the device width and length, and does not depend on the gate-source voltage.

A rigorous analysis requires a large set of devices, even more so in case of yield issues. Common-electrode designs are not recommended in that case as multiple devices may be affected by a single defect. Area scaling as normally observed on classical semiconductor-based transistors may not occur in transistors based on 2D material channels.

This work further confirms, using experiments conducted on a single transistor at cryogenic temperatures, that short channel effects are more prominent in transistors with a high-K channel, heavily reducing the scalability of devices.

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