Towards a single-photon energy-sensitive pixel readout chip: pixel level ADCs and digital readout circuitry

David San Segundo Bello, Bram Nauta and Jan Visschers

Abstract— **Unlike conventional CMOS imaging, a single photon imager detects each individual photon impinging on a detector, accumulating the number of photons during a certain time window and not the charge generated by the all the photons hitting the detector during said time window.**

The latest developments in the semiconductor industry are allowing faster and more complex chips to be designed and manufactured. With these developments in mind we are working towards the next step in single photon X-ray imaging: energy sensitive pixel readout chips. The goal is not only to detect and count individual photons, but also to measure the charge deposited in the detector by each photon, and consequently determine its energy. Basically, we are aiming at a spectrometer-in-a-pixel, or a "color X-ray camera".

The approach we have followed towards this goal is the design of small analog-to-digital-converters at the pixel level, together with a very fast digital readout from the pixels to the periphery of the chip, where the data will be transmitted off-chip.

We will present here the design and measurement on prototype chips of two different 4-bit pixel level ADCs. The ADCs are optimized for very small area and low power, with a resolution of 4-bits and a sample rate of 1 Msample/s. The readout architecture is based around current-mode sense amplifiers and asynchronous token-passing between the pixels. This is done in order to achieve event-by-event readout and, consequently, on-line imaging. We need to read event-by-event (photon-by-photon), because we cannot have memory on the pixels due to obvious size constraints. We use current-mode sense amplifiers because they perform very well in similar applications as very fast static-RAM readout.

Keywords—**X-ray imaging, analog to digital conversion.**

I. Introduction

SEMICONDUCTOR hybrid pixel detectors have proven their feasibility as photon-counting imaging devices for X-rays at room temperature[1], even for X-ray energies as low as 5 keV [2].

In a hybrid pixel detector, the detector and the readout electronics are manufactured independently and they are connected afterwards using flip-chip bonding techniques as figure1 shows . This allows for separate optimization of the detector and the readout electronics. The main advantages of hybrid pixel detectors with respect to other pixelated X-ray imaging detectors (such as CCDs, CMOS imagers, film, phosphor plates, etc) are *direct conversion* and *individual photon detection*. *Direct conversion* means that the photon deposits an amount of charge in the detector directly proportional to the energy of the photon. The signal generated in the detector can then be processed by the readout electronics. Other semiconductor-based detectors for X-rays such as CCDs or CMOS imagers need some intermediate step to convert X-ray photons to visible-light photons. *Individual photon detection* refers to the fact that photons are detected individually one by one in each pixel.

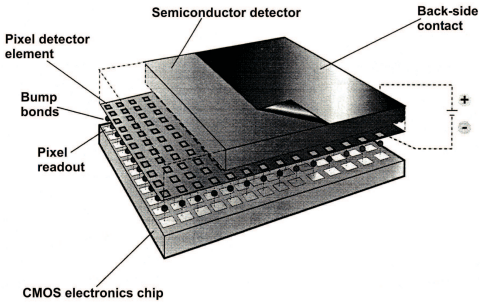

Fig. 1. Drawing of a hybrid pixel detector.

So far, hybrid pixel detectors for X-ray imaging have been limited to counting the number of photons above a certain energy threshold. The energy information carried by each photon is then lost in the electronic processing of the signal from the detector. However, the knowledge of the number of X-ray photons which impact each pixel as well as of their respective energy levels can provide a variety of functions which, with a very high probability, will improve the resulting image, given the same X-ray dose.

The individual photon detection performed in pixel detectors allows the addition of pixel-level energy sensitivity by adding circuitry that converts, stores and sends off-chip the energy information. The conversion can be performed using analog-to-digital converters (ADCs) in the readout chip, for example in the pixel electronics.

Section II gives a description of the full system. In sec-

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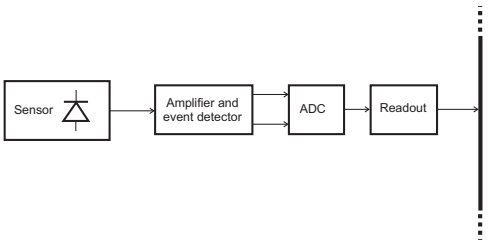

Fig. 2. Block diagram of the pixel electronics.

tion III we focus on the design and measurement of the ADCs. Section IV describes the readout architecture and circuitry we plan to use, and finally we offer some conclusions and indicate future work.

II. System description

A hybrid pixel detector system with energy sensitivity can be achieved in different ways. For example, the analog value after the signal conditioning can be read out of the chip and processed accordingly. A better approach is to include some kind of analog-to-digital conversion in the readout chip itself. If high precision is needed, the analog-to-digital conversion must be performed in the periphery (or non-active part) of the chip. However, the precision of the system is typically limited by the energy resolution of the detecting medium. If one takes a typical GaAs or Cd(Zn)Te detector, its energy resolution falls in the 4-bit to 6-bit category. One can then think of including the analog-to-digital converter in the pixel itself. This is, in fact, a trend that can also be seen in conventional CMOS imagers, where more and more electronics are being put in the pixels, thanks to Moore's Law and the advantages of pixel-level processing [4].

We assume that the pixel electronics have a structure such as the one shown in figure 2. The signal deposited in the detector by each individual photon is first amplified and integrated (for example, using a charge sensitive amplifier[3]). This is needed in order to convert the deposited charge to a voltage or current that can be converted by the ADC, and also to increase the signal-to-noise ratio. At the same time, a pulse is generated if the signal is above the noise level. The analog signal and the digital pulse coming out of this first block are the inputs to the analog to digital converter. The pulse is used to start the conversion, and the output of the amplifier is the signal that will be converted.

After the ADC, a fast digital readout circuit is needed in order to allow a new photon hit to be processed in the pixel. In most pixel readout chips there is a clear distinction between the image acquisition and the data readout. In our case, however, the digital readout has to be working while an image is being acquired, as we do not intend to provide means for storing more than one hit in the pixel. This means that an *event by event readout* is needed for this kind of circuit.

III. Design of the ADCs

We have chosen a resolution of 4-bit for our design, as this corresponds approximately to the energy resolution that can be achieved with a room temperature GaAs detector [5]. The area for the pixel (including amplifier, ADC and readout) should not exceed 100 μm by 100 μm. Although this is a very big number compared to visible light imagers, it is a typical size for X-ray imaging. Assuming a typical active imaging area in excess of 1 cm^2, the number of pixels will be in the order of a few tens of thousand. In order to calculate the typical conversion rate for our converters, we assume a photon rate of 10^6 photons per second and per mm^2. This is the typical rate for radiological applications.

With these photon rate and pixel size, the photon rate per pixel would be of the order of 10^4 photons per second. Taking a conservative approach (as we have yet to add the integration and readout time), we will use a conversion time of approximately 1 μs. This time is also comparable to the counting frequency in photon counting pixel detectors [3].

After some exploration of the possible ADCs that can be implemented with little area and power overhead, we decided to further investigate the possibilities of successive approximation and algorithmic analog-to-digital conversion.

The designs discussed in this paper have been manufactured in a 0.25 μm CMOS process. Although the process allows 6 metal layers, our designs were processed with only 3 metal layers, due to limitations in the organization of the multi-project runs where our chip is included.

A. Successive Approximation ADC

Figure 3 shows a schematic diagram of a typical successive approximation ADC. This converter needs a number of clock cycles equal to the number of bits in order to perform the conversion. We use a current-mode binary-weighted DAC, and a comparator based on the one reported in [6]. The complexity of the circuit lies mostly in the digital circuitry, as it is responsible for switching ON and OFF the current sources in the DAC in response to changes in the comparator output. This can be seen clearly in figure 4, which shows the layout of our ADC. At the bottom side one can see the comparator and the DAC, while the top side is the digital part of the ADC.

The speed of our comparator is proportional to the difference of currents applied to its input. This means that by

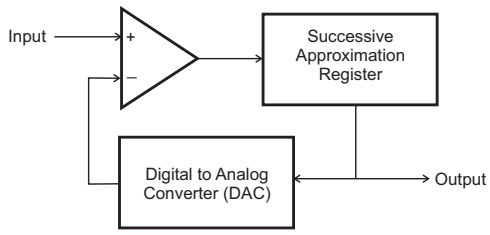

Fig. 3. Block diagram of the successive approximation ADC.

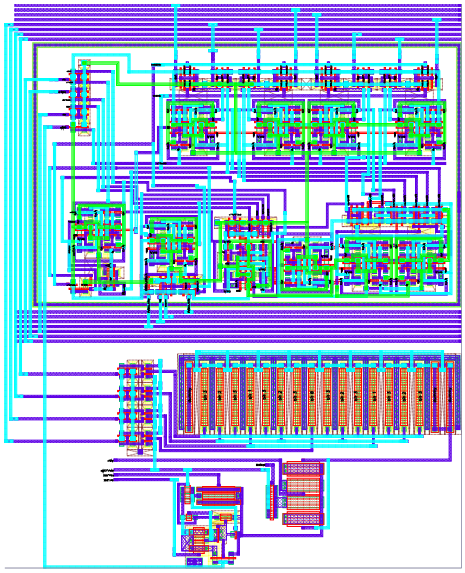

Fig. 4. Layout of the successive approximation ADC. The size of the circuit is 104 μm by 84 μm.

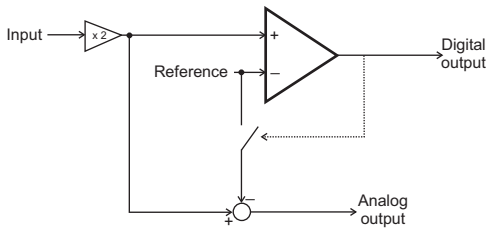

Fig. 5. Schematic view of the basic building block of the algorithmic ADC.

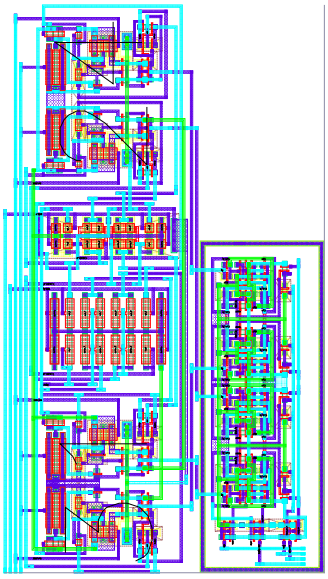

Fig. 6. Layout of the algorithmic ADC. The size of the circuit is 98 μm by 55 μm

increasing the full scale current (and hence the I_{LSB} value) we could achieve higher conversion speeds at the price of a higher power consumption.

B. Algorithmic ADC

The problem with the previous converter is the need for a relatively complex digital circuitry in the pixel. This can lead to crosstalk as well as substrate coupling noise problems. One can think of moving some (or all) the processing done in the digital domain to the analog domain.

A converter that does such a thing is the current-mode algorithmic ADC, as originally described in [7] and later in [8]. The basic building block of this converter can be seen in figure 5. By using the same comparator used in the successive approximation we can save power with respect to the design in [8]. The reason is that in our comparator we can reuse the difference current flowing in the comparator as the input to the next block, instead of having to copy the currents as [8] does.

In this ADC, the input signal is multiplied by 2 and compared with a reference value equal to the full-scale current of the converter. If the reference is higher, the analog output is set equal to the input multiplied by two, and the digital output is set low. If the reference is lower, the analog output is set equal to the input multiplied by two minus the reference, and the digital output is set high. By connecting N such blocks one after the other so that the analog output of one block is the input to the following block, we can obtain an N-bit ADC.

In fact one can say that this ADC is a successive approximation ADC, but instead of doing the comparison for each bit in different clock cycles, it does the comparisons in different circuit blocks. Obviously the current consumption will be larger, but the amount of digital circuitry is dramatically reduced, as one can see in the layout of the ADC shown in figure 6. Additionally, the size of the ADC is also reduced.

C. Measurement results

To prove the feasibility of such small area and low power ADCs we designed a prototype chip which included both ADCs. Figure 7 shows a photograph of the chip.

Fig. 7. Chip photograph showing the ADC structures at the top. The chip is 2mm x 2mm.

TABLE I
SUCCESSIVE APPROXIMATION ADC CHARACTERISTICS

Characteristic	Simulated	Measured	Units
$\|INL\|$	< 0.2	< 0.3	LSB
DC current	1.8	< 2	μA

Table I compares the simulated with the measured values for the integral non-linearity (INL) and the current consumption for the successive approximation ADC; and table II does the same for the algorithmic ADC. The conversion time was 1 μs in both cases and the supply voltage is 1.8 Volts. At the moment of writing this paper two chips have been measured giving practically the same results.

IV. PIXEL DATA READOUT

The final chip should have all non-pixel circuitry (biasing, I/O, etc...) located on only one side, to allow imaging arrays of more than one chip (i.e.: 2x2). The chip readout circuitry will be then located in one side of the periphery of the chip, and all pixels have to communicate with it.

Once the conversion is finished, the pixel has to be readout in order to allow further photons to be processed. In order to do this we are faced with two different problems: which architecture to choose in order to address the pixels to be read and which circuitry to use in order to read the digital data from the pixels for minimum delay.

A. System architecture

One way to address the pixels would be as in a memory array or a CMOS imaging array. Each pixel has a row and column line, and the row and column addresses are decoded in the periphery of the chip. This is probably the best approach when the whole array is to be read, or when we know in advance which portion of the array has to be read. In our case, however, the amount and location of pixels in the array to be readout varies widely with the application and the object to be imaged.

TABLE II
ALGORITHMIC ADC CHARACTERISTICS

Characteristic	Simulated	Measured	Units
$\|INL\|$	< 0.1	< 0.2	LSB
DC current	6.4	< 7	μA

The solution we have chosen is a pixel-driven readout. Similarly to some hybrid pixel detectors used in high energy physics experiments, a token is passed asynchronously through the pixels and when a pixel that has been ”hit” receives the token, it can send its data to the periphery. By grouping the pixels per columns and using a similar ”token passing” scheme at the column level one can achieve high readout speeds with relatively little circuit overhead.

B. Digital data readout

The ultimate goal of this project is to have relatively big chips (about 2 cm per side), which means that the connection from a pixel to the periphery can be as long as 2 cm. It is well known [9] that for the most recent CMOS technologies, chip interconnects above 3-4 mm will be limited by the delay introduced by the interconnect itself and not by the gate-delay. This means that when driving a long interconnect line from one pixel, the major source of delay and capacitance loading is not the input of the next block, but the interconnect wire. Another additional problem is the amount of power spent at the pixel in order to drive the wires from 0 to V_{dd}. The use of current-sensing circuitry solves to a certain extent both problems. These circuit techniques have been used in the world of random access memories since the early 90s [10] and have proven very successful so far [11]. Given the clear parallel between our system and a RAM array (an array of thousands of elements with digitally stored data that must be read at the maximum speed possible), the use of current-sensing readout is perfectly suited for us.

In this readout scheme, instead of driving the interconnect from 0 to V_{dd}, only a very small voltage change (typically a few tens to a couple hundred mV) is forced in the line and the information is sent in the form of electrical current. At the periphery of the chip this current can be easily detected and amplified in order to obtain the full voltage swing.

We have designed a chip in order to test this approach where an array of the ADCs presented in section III is to be read out via the current-sensing mechanism. This chip was just received at the moment of writing this paper, so no results are presented here.

V. Conclusions and future work

We have shown that analog-to-digital conversion can be feasible for hybrid pixel X-ray imagers at moderate photon rates and pixel sizes. We have designed and tested two different candidates for this purpose: a successive approximation ADC and an algorithmic ADC. The performance of both ADCs is as expected from simulations.

We have also designed a chip in order to test the readout of the digital data from the pixel-level ADCs. The last step of our project is to design a full system and connect it to a sensor in order to test the feasibility of energy-sensitive hybrid pixel detectors for X-ray imaging

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