Small-Delay Fault BIST in High-Speed Chip Interfaces

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Abstract— **During the past years, due to the decrease of the minimum feature size in CMOS technology, the on-chip clock frequencies have increased dramatically ranging into the GHz domain. This increase has also pushed the need for higher data-transfer rates between these high-speed ICs, in order to optimize the entire PCB system. As a result, the clock/data skew can span tens of clock cycles. In order to cope with this skew, synchronization strategies have been developed which rely on either analogue or digital multi-tap delay-lines. In order for the synchronization mechanism to function properly, all tap-delays of the delay-line should have the same values within few percentages.**

This paper presents a technique, based on the oscillation method, to measure tap-delays of a delay-line with an accuracy of $\pm$10ps. A chip has also been implemented in an UMC 0.18μm CMOS technology to prove our assumption. The measurements carried out on the chip confirmed the above mentioned accuracy.

Keywords— **Delay-fault testing, BIST, High-Speed Chip Interfaces, Oscillation-based**

I. Introduction

SoC design is being facilitated by the development of new deep sub-micron technologies. More and more cores can be squeezed on the same die, resulting in ever more complex systems. While the number of devices per SoC is increasing at an exponential rate, the number of access pins of the SoC is not. A huge amount of information generated/received by the SoC should pass via a small number of pins. In order not to hinder the SoC design strategy, the transfer rate per pin should be increased dramatically. High-speed synchronization strategies between ICs have been developed to address this issue.

This paper is organized as follows: section II will provide an overview of some existing high-speed inter-chip synchronization strategies. The main part of every synchronization module is found to be a high-speed multi-tap delay-line. A DfT-aware implementation of such a delay-line will be shown in section III. Section IV will present how an oscillation technique can be used to measure tap delays. The next section V will present the real scheme implemented in the UMC 0.18μm CMOS process. The obtained measurement results are shown in section VI. Finally, the conclusions are given in section VII.

II. Functional Descriptions of High-Speed Interfaces

Many papers [7, 5, 4, 10] have been published that address the high-speed data synchronization between SoCs. All of the synchronization mechanisms have something in common, being a delay-line either digital or analogue, controlled or not, tapped or not. The synchronization mechanism is dependent on these delay-lines and any manufacturing fault, either catastrophic or not, will hamper the functionality of the synchronization mechanism.

A generic architecture of a high-speed synchronization mechanism is presented in Figure 1. The data can be transmitted from one chip to another using low-voltage differential signaling (LVDS). In Figure 1, the differential inputs are represented by the "*inP*" and "*inN*" signals. The transmitted data is synchronous with the clock signal "*clk*" but

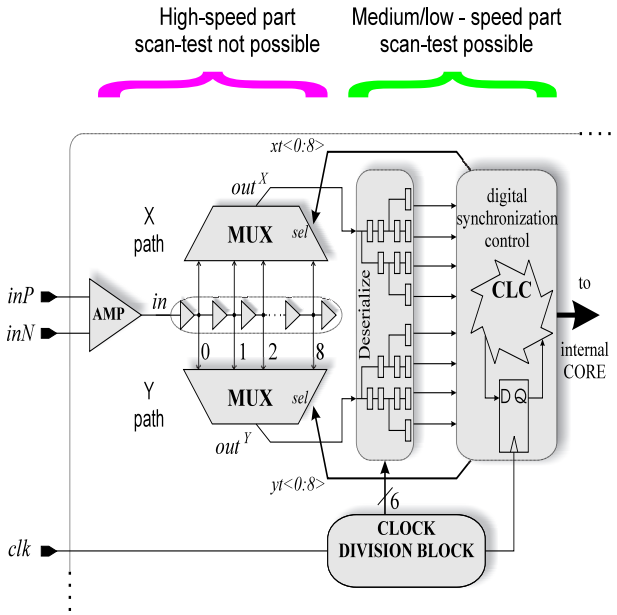

Fig. 1
Generic architecture of a high-speed synchronization mechanism

the skew between the data and the clock can span many clock cycles. The differential signal is transformed on-chip in a single-ended signal ("*in*") by the **AMP** operational amplifier. This signal then passes a multi-tap delay-line. Different delayed versions of the "*in*" signal can be selected by the two MUXs. There are two symmetrical paths. These two paths are necessary for the **digital synchronization control** module, seen on the right side of Figure 1. Following the selection of a certain tap, the data is transformed from serial to parallel by the **deserialiser** module (Figure 1). This module comprises of only flip-flops, which are clocked by different phases and frequencies of the initial clock "*clk*". The **clock division block** is the one that takes care of the generation of the clocks for the whole design.

The **digital synchronization control** module is generating all the select signals for the two access MUXs. In this block, the correct sampling point of the incoming data is calculated and the proper tap is selected.

Testing these type of interfaces in general, and the delay-lines in particular, is very difficult while using a classical scan-test method. A list of reasons is given below why the scan-test technique cannot be easily applied:

- Most of the time, the high-speed interface design comprises some analogue modules, while the scan-test is intended for digital testing only.
- Even if the synchronization mechanism is pure digital, scan-test cannot be applied due to the negative impact on the speed performance of the interface.
- Scan-test has been mainly designed for stuck-at faults. However, for a high-speed interface especially delay faults are crucial.
- At-speed test using the scan-test strategy can be prohibitively expensive because it can only be performed using costly high-speed ATE systems.
- Scan-test of a delay-line will introduce several undetected stuck-at faults due to the inability to provide different inputs to the access multiplexers [8, pages 48-49].

The **digital synchronization module** requires that all tap-delay values should be very well matched at the layout level. Therefore a technique to accurately measure these tap-delays within an accuracy of $\pm$10ps had to be developed in our case. The following sections will present a delay-line used as a core part in a high-speed synchronization mechanism together with the differential oscillation technique which is able to measure the tap-delay values with the requested accuracy. In reference [9], a similar measurement accuracy is achieved in simulations by using a mutual exclusion (MUTEX) element. However, an accurately calibrated delay line is required to obtain this accuracy.

III. Block Scheme of a Multi-Tap Delay-Line

Figure 2 shows a multi-tap delay-line scheme used in a high-speed synchronization mechanism. For the time being, the reader should ignore the shaded transmission gates which belong to the DfT hardware. They will be referred to in the next section. An intrinsic buffer, as the one between the "*a*" and "*b*" signals, is comprised of an odd number of inverters, where the exact number is application specific. Usually the number of inverters inside a buffer is 2; therefore the delay associated with these tap-delays is very small (around 400ps).

In functional mode, the signal "*data_in*" is propagating to the output signals "out^X" and "out^Y" via a certain number of taps selected by one of the signals "*xt<0>*" ... "*xt<8>*" and "*yt<0>*" ... "*yt<8>*". Only one of the signals "*xt<0>*" ... "*xt<8>*" can be logic one at a certain moment. This also holds for the signals "*yt<0>*" ... "*yt<8>*".

IV. Tap-Delay Measurements using a Differential Oscillation Technique

Oscillation techniques have been extensively used in the past to characterize, measure and analyze delays. The ring oscillator was probably the first design utilized to characterize the speed of a new technology using the oscillation technique. Since then, the same oscillation technique has been also used to test analog and digital circuits [2, 1]. The power of this technique lies in the fact that twice the *average* delays, between falling and rising propagation delays, in an oscillation loop is equal with the oscillation period. Therefore, if the oscillation period or the frequency is precisely known, the average delay of the oscillation loop can be calculated.

Our aim is to measure the tap-delays of a delay line and not the delay of an oscillation loop. Therefore, a plain oscillation technique is not very useful for determining these tap-delays. Instead, a differential oscillation technique, as explained bellow, is used.

The shaded transmission gates in Figure 2 are belonging to our inserted DfT hardware. Their purpose is to generate shorter oscillation periods by closing the oscillation loops inside the delay-line. These short oscillation periods permit an increase in the measurement accuracy due to a smaller influence of the power supply and temperature [8, page 137].

Let us presume that an oscillation loop T^X_{8-6} (Figure 2) is activated by selecting tap#8 (signal "*xt<8>*" is logic one) and closing the loop in front of tap#6 (signal "*xf<6>*" is logic one). At the same time the transmission gate in front of tap#6, controlled by signal "*xyp<6>*" should be

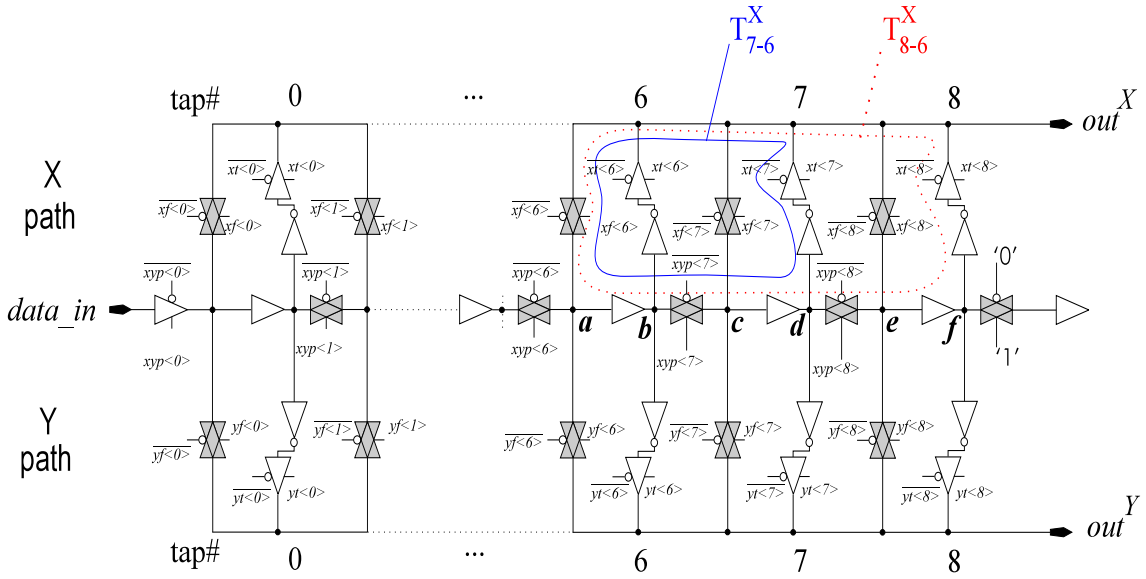

Fig. 2
A DELAY-LINE SCHEME USED IN A HIGH-SPEED SYNCHRONIZATION MECHANISM (THE SHADED COMPONENTS BELONG TO THE DFT HARDWARE)

disabled ("*xyp<6>*" is logic zero). Let us denote:

- T_8^X, the oscillation period when the T_{8-6}^X oscillation loop is activated.
- t_{76}, the average delay between the nets "*b*" and "*d*"
- t_{87}, the average delay between the nets "*d*" and "*f*"
- t_7^X, the average delay between the nets "*d*" and "*out*^{X}"
- t_8^X, the average delay between the nets "*f*" and "*out*^{X}"
- t_{err}^X, the average delay between the nets "*out*^{X}" and "*b*"

All of the average delays above should be considered as the average delays of the rising and falling propagation delays.

If the loop T_{8-6}^X is activated, an oscillation will start. Equation (1) shows the relation between the oscillation period of the induced oscillation and the average delays in the loop.

$$t_{err}^X + t_{76} + t_{87} + t_8^X = \frac{T_8^X}{2} \quad (1)$$

Following the same reasoning as for the oscillation loop T_{8-6}^X, equation (2) shows the relation between the oscillation period of the induced oscillation and the average delays in the loop T_{7-6}^X (Figure 2).

$$t_{err}^X + t_{76} + t_7^X = \frac{T_7^X}{2} \quad (2)$$

Subtracting the two oscillation periods from equations (1) and (2) one can deduce:

$$T_8^X - T_7^X \stackrel{def}{=} T_{87}^X = 2(t_{87} + t_8^X - t_7^X) \quad (3)$$

In equation (3), $T_{87}^X/2$ represents the value of the tap-delay between tap#8 and tap#7 at the path *X* access points, and not the intrinsic tap-delay (t_{87}). From a functional point of view, the tap-delays at the path *X* access points are of more importance than the intrinsic tap-delays, since the signal out^X is the one used afterwards by the synchronization mechanism. However, in a fault-free situation, one expects $T_{87}^X/2$ to be very close to the t_{87} value. This is because the inverters and the tri-state buffers on the path *X* at tap#8 and tap#7, which are a source of uncertainty, will be very well matched in the layout, and therefore $t_8^X \simeq t_7^X$. As can be noticed, the parameter t_{err}^X does not appear in equation 3.

The measurement of all oscillation periods will be performed on-chip by using a digital counter clocked by a buffered version of the signal "*out*^{X}". In reference [8, page 117], more information regarding this technique is presented. Also the measurement accuracy of the proposed method is analyzed in this reference.

V. DESIGN IMPLEMENTATIONS FOR THE DELAY-LINE

Our delay-line scheme presented in Figure 2 and its additional DfT hardware has been implemented in a real design. The following subsections, V-A and V-B will present the details of the chip implementation. The demonstrator chip has been called **DLLINE**.

A. Delay-Line Scheme

The top level of the delay-line scheme and the associated DfT hardware is presented in Figure 3.

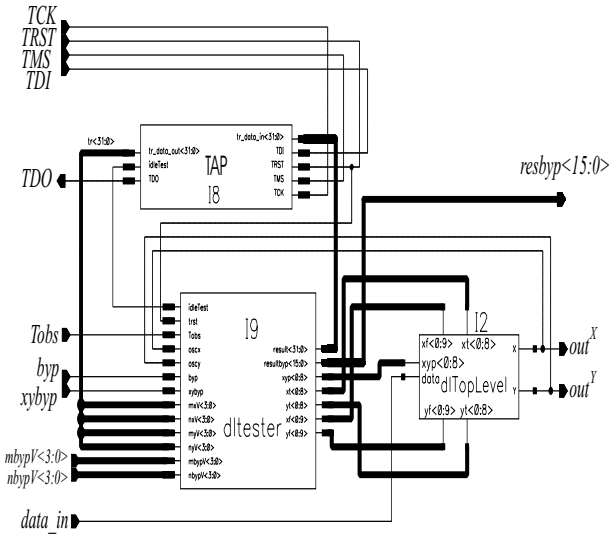

Fig. 3
TOP-LEVEL IMPLEMENTATION OF THE DLLINE CHIP

Instance **I8** represents the TAP controller of the IEEE standard 1149.1-2001 [6]. Via this TAP controller it is possible to select different taps and feedback loops in the delay-line. The TAP controller will also collect the results of the internal counter and serialize them out via the "*TDO*" signal.

In Figure 3, instance **I2**, called dlTopLevel, is the delay-line as presented in Figure 2. The control signals, for selecting the taps of the path *X* are "*xt<0:8>*". The feedback selection of the taps in test mode is carried out by the signals "*xf<0:9>*". One may notice an extra signal "*xf<9>*" as compared to the delay line of Figure 2. This is used in functional mode and has not been shown in Figure 2. It has no influence on the proposed testing method and can be ignored. Signals "*xyp<0:8>*" control the transmission gates in front of the intrinsic buffers (see Figure 2).

In Figure 3, together with the delay-line (**I2**) and the TAP controller (**I8**), there is also a block called dltester (**I9**). This block takes care of decoding the signals "*nbypV<0:3>*" and "*mbypV<0:3>*" (explained later) in the control signals "*xt<0:8>*", "*xf<0:9>*" and "*xyp<0:8>*" of the delay-line.

The complete design has two testing modes, being "TAP mode" and "backup mode". During the TAP mode, control signals of the delay-line are scanned-in via the "*TDI*" input and the results of the counter are scanned-out via the "*TDO*" output. The backup mode has been provided, as the name suggests it, as a backup solution in case the TAP mode is faulty. The backup mode is activated by providing a logic one in the "*byp*" signal. The signal "*xybyp*" is used to select which path, either *X* or *Y*, is tested during bypass mode. The two paths cannot be tested in parallel due to the chip-limited number of pins (48). In backup mode, the delay-line is controlled by "*nbypV<0:3>*" and "*mbypV<0:3>*" input signals via the **dltester** block. The **dltester** block takes care that no conflicting combinations can be applied to the delay-line, which can damage the design by having two drivers of different values (zero and one) on the same net. The results of the internal counter that is counting the number of rising edges of the internal self-generated ring-oscillations can be observed outside via the signal "*resbyp<15:0>*".

B. The Delay-Line Layout

The scheme presented in Figure 3 has been implemented in an UMC 0.18μm CMOS technology.

The layout of the design is shown in Figure 4. The pic-

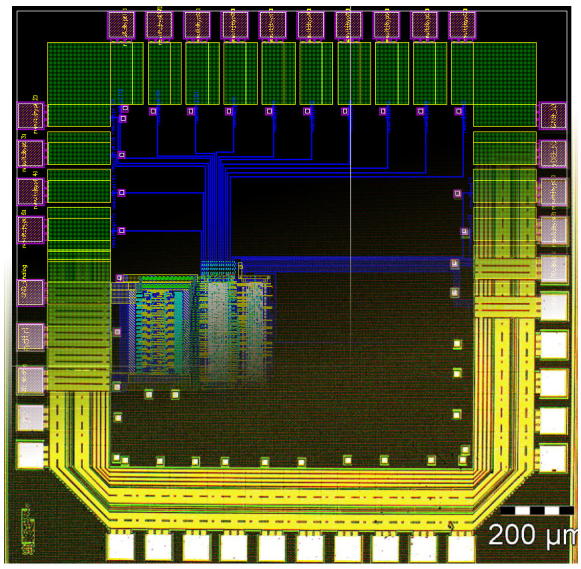

Fig. 4
"DLLINE" CHIP LAYOUT; MANUFACTURED LAYOUT SUPERIMPOSED ON THE CADENCE LAYOUT

ture of the manufactured chip has been superimposed on the the layout as seen in "Virtuoso Layout Editor" of CADENCE. The core area of the chip is 0.3mm×0.4mm. The total chip area (including pads) is 1.5mm×1.5mm.

VI. TAP-DELAY MEASUREMENTS

The "DLLINE" chip measurements have been carried out using a Logic Master ATS1 test system [3].

Figure 5 shows a screen dump of a basic test. After the reset signal "*TRST*" is set to one in sequence number 18, the internal test structure is activated. Following two falling edges of the signal "*Tobs*", the results on the

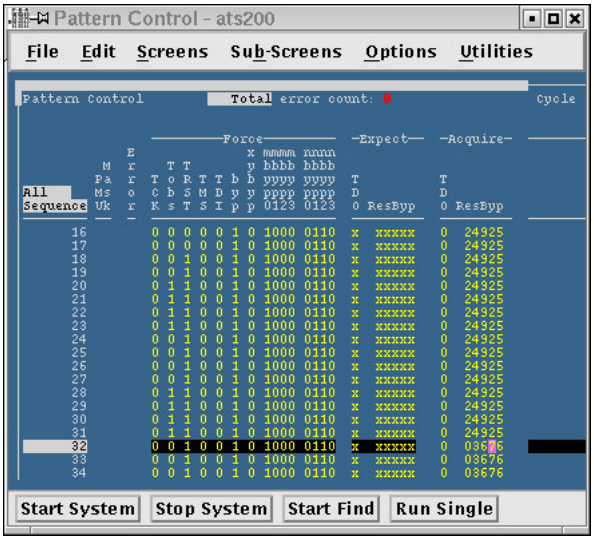

Fig. 5
IMS SCREEN DURING AN OSCILLATION MEASUREMENT

"*resbyp<15:0>*" bus signal can be read out. In this particular case, tap number six is selected ("*nbypV*"=6) and its signal is fed back to tap number one ("*mbypV*"=1). Please note that the LSBs for the binary signals "*mbypV*" and "*nbypV*" are at the left in Figure 5. The signal "*resbyp<15:0>*" is displayed in decimal form in the same figure. The cycle time for the measurements is $4.992\mu s$. The counting happens only once when the "*Tobs*" signal is logic one. The internal generated ring-oscillation is clocking the internal counter 3676 times during an interval of $4.992\mu s \cdot 4 = 19.968\mu s$ (T_{obs} is logic one for four cycles). The expected column in Figure 5 should be ignored since simulation results have not been entered in the test system. Hence the oscillation period can be calculated as $19.968\mu s/3676 = 5.432ns$.

Many measurements, as the one presented above, have been performed for determining the delays between taps. The delay between tap#7 and tap#8 has been chosen to prove that the measurement accuracy is within $\pm$10ps. The reason for selecting this delay is that it permits the maximum number of measurements (7) for its determination. One of the many ways in which the delay t_{87} can be measured has been shown in Figure 2. In this figure, tap#6 has been chosen as feedback. The following steps have been carried out in order to determine the accuracy of the measured delay between tap#7 and tap#8:

- Oscillation periods have been calculated based on the number present in the internal digital counter for the following setups:
  - tap#8 is selected and fed back in tap# 0, 1, 2, 3, 4, 5, 6 and 7
  - tap#7 is selected and fed back in tap# 0, 1, 2, 3, 4, 5, 6 and 7

For each of the above setups, 160 values of the number stored in the counter have been recorded. Therefore, 2560 values have been considered.

- For each feedback tap (0, 1, ..., 7), the values of the delay between tap#7 and tap#8 have been calculated by subtracting the oscillation period T_7^X from the oscillation period T_8^X.

All calculated delay values based on the number stored in the internal counter are shown in Figure 6 for path *X* and in Figure 7 for path *Y*. On the horizontal axis of Figures 6 and 7, the tap number used for measuring the tap-delay between tap#7 and tap#8 is shown. On the vertical axis of the same figures, the value of the tap-delay between tap#7

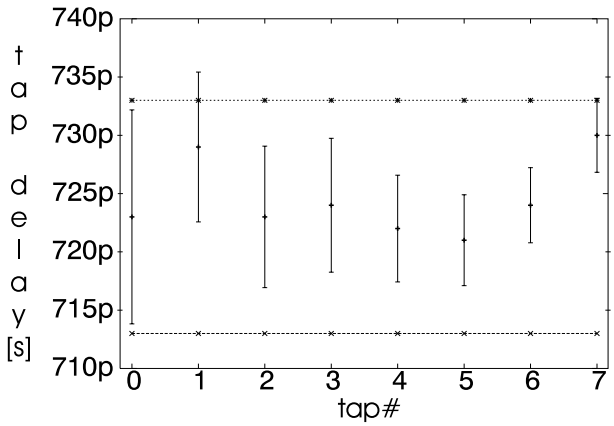

Fig. 6
MEASURED VALUES FOR THE DELAY BETWEEN TAP#7 AND TAP#8 FOR PATH *X*

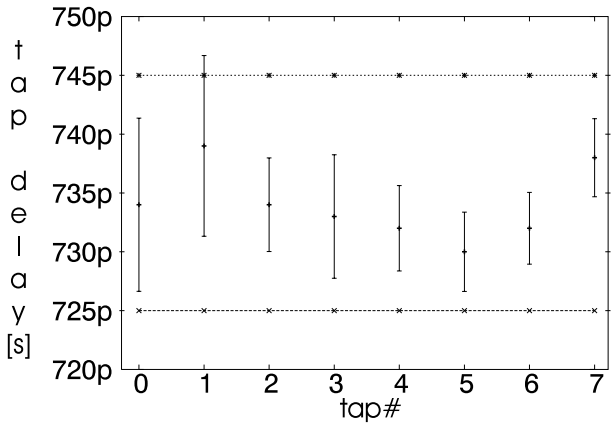

Fig. 7
MEASURED VALUES FOR THE DELAY BETWEEN TAP#7 AND TAP#8 FOR PATH *Y*

and tap#8 is given, together with the associated measurement error. On the same axis, the minimum and maximum of the accepted error of $\pm$10ps can also be seen. As one can notice, all the measurements (with the exception of the measurement via tap 1) are within the accepted tolerance. It can also be seen that the measurement error is improving if the oscillation period is smaller because the influence of the power supply and the temperature is decreased during adjacent measurements as has been presented in reference [8, page 137]. Another effect that can be seen in Figures 6 and 7 is the 'false' increased value of the delay between tap#7 and tap#8 if very short oscillation periods are used (tap#7 is used for measurements). This effect is caused by high capacitive loads on some nets which prevent the signal to reach the power supply or the ground. This effect is analyzed in more detail in reference [8, pages 132-134].

VII. Conclusions

A new method, based on the oscillation test technique, has been presented for measuring the tap-delays of a digital delay line used for high-speed data synchronization. The design of the presented delay-line together with its associated DfT hardware has been implemented in an UMC $0.18\mu m$ CMOS technology. By measuring and subsequently calculating the tap delays it has been shown that the measurement accuracy can be less than $\pm$10ps which is equivalent with 1.4%. The results are important since it has been proven that the proposed method can be used to accurately measure the tap delays of any delay-line.

Acknowledgments

The authors would like to thank Benoit Jerry for implementing the "DLLINE" chip, Rob Tijink for providing CAD tools support and Marcel Weusthof for CAT tools support.

The Technology Foundation STW, applied science division of NWO, has financially supported this research.

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