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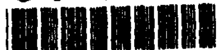

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DTIC QUALITY INSPECTED 2

Process Maturity Grids used as a Decision Support Tool

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Summary

Failure rates of modern ASICs and ASSPs can not be demonstrated using reliability tests on product level. Reliability demonstration must be done by quantifying the quality of the process that produces these integrated circuits. Process capability however, is not fixed over time. As a process gets more mature process capability tends to improve. In this paper we introduce the concept of process maturity growth to quantify the quality of suppliers processes as a function of time. The method is illustrated for a submicron double metal CMOS process in which many mixed standard cell and full custom designs are processed.

Introduction

Traditionally qualification of application specific integrated circuits (ASICs) and application specific standard products (ASSPs) is done on product level. This means that after design, manufacturing and evaluation of the integrated circuits, product tests are carried out to ensure product quality and reliability. For several reasons this approach will become obsolete in the near future (Refs. 1-3). Most important reasons are:

- currently required low failure rate levels can no longer cost effectively be measured on product level because this would require too many test samples
- decreasing time to market of new ASIC designs does not allow a long qualification phase
- there is a trend towards more functional diversity and smaller manufacturing volumes, full product qualification does not pay off for these small manufacturing volumes

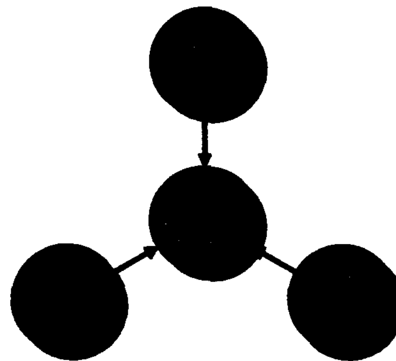

Fig. 1. *Changing prerequisites for IC qualification processes*

These developments are schematically given in Fig. 1 and they require a change in vendor/customer relationships with respect to qualification and reliability demonstration (Ref. 3). From consumer electronics industry we observe two changes that are going on at this moment. First, the number of suppliers delivering integrated circuits are minimised to a number of preferred suppliers.

Secondly, as a consequence, not only the products of these preferred suppliers are qualified but more important, the design and manufacturing processes of the supplier are qualified. For a semiconductor supplier these are the IC design process, the wafer fab process and the assembly process. This change from product qualification to process qualification is schematically given in figures 2 and 3.

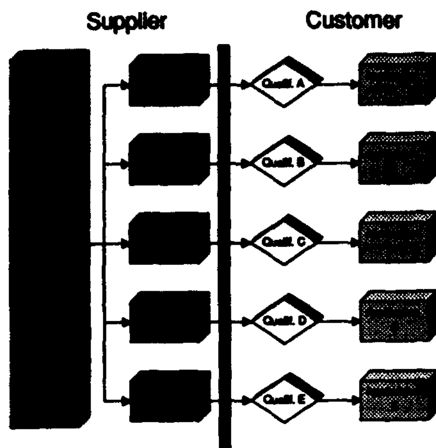

Fig. 2. *Traditional type related IC qualification processes*

The approach, given in Fig. 3 is conceptually very simple. It is important, however, to emphasise three major prerequisites, necessary for a successful completion of this process.

1. A supplier and a customer of an integrated circuit should agree to exchange information beyond the normal product specifications

2. A supplier and a customer should agree what parameters in (design and production) processes of a family of ICs are relevant for a customer

3. A supplier and a customer should agree how the results of such a process assessment are monitored; not only during a first qualification but also in time

This process based approach towards device qualification is not new in electronics industry. Today already many ASICs that are used in consumer electronics products are qualified by their design and production processes. Some examples are gate arrays and digital standard cell designs. These design technologies have in common that design and production processes can be highly standardised. The design freedom is limited and device qualification can be done on basis of design and production processes for two reasons:

1. There is a large structural similarity between the devices
2. Performance and reliability are regularly monitored respectively demonstrated using a representative test device. For standard cell this can be a special designed IC with part of the library and test structures on it.

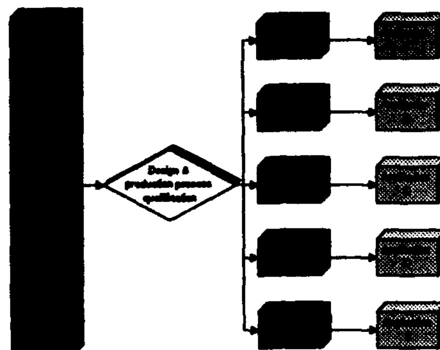

Fig. 3. *Qualification, based on design and production processes*

The opposite regarding design freedom are ASSPs that are full custom designed. This is given in Table 1. The freedom in this design style is such that electrical characterisation and reliability demonstration are typically done for each IC type. Many ASIC designs that we face in consumer electronics products are standard cell designs with some custom designed instances or mixed digital/analogue ASICs. For cost and/or performance reasons they may be realised in a new production technology. Given the developments from Fig. 1 it are these type of ASICs where it is most difficult for, to develop efficient standard process based qualification procedures.

IC type	type of qualification
FPGA/ gate array	process
standard cell	process
mixed std./custom mixed analogue/dig.	process/type
full custom ASSP	type

increasing design freedom

increasing qualification effort on type basis

Table 1: *Different types of ASICs in consumer electronics industry have different qualification strategies*

At this moment for most of this type of ASICs type qualification is performed. For reasons mentioned before our goal is to come to a process way of qualification also for these type of circuits. In this paper such an approach is described for IC production process. Design- and assembly are not included. It is a two step approach:

1. Assess the IC production process for the risks involved for the customer

2. Limit the type specific qualification tests to the items that pose a risk for the customer

This approach is not so straightforward as it may seem because in general process capability is a function of time. As more products are made in a specific process the maturity of the process will increase. To monitor this, we will introduce the concept of process maturity growth to be able to quantify the capability of the suppliers processes with regard to customer products as a function of time.

Process maturity growth

With a simple example we will illustrate what is meant by process maturity growth. For this example we will use "process defect induced" early failure rate (EFR) as a set of failure mechanisms that needs to be described over time. What typically is found when a new production process grows towards a mature process is given in Fig. 4. Typically once the process is able to make ICs that perform to function and reliability (end of life) requirements (this is called potential phase) the EFR is still much higher than the ultimate capability of the manufacturing line. Due to all sorts of improvement actions (e.g. on scratches, particles) the EFR of the new process improves rapidly. However due to special failure modes the performance is not continually decreasing but in the beginning of the lifetime of the new process some "humps" are seen in EFR rate due to some special failure modes. This period is called consistency phase. At the end of the consistency phase these special causes are eliminated and remaining defects are successfully contained the EFR of the new process will become stable. Containment of the defects can not only be done on process level by the control of particles but also by yield screening on wafer level (Ref. 4) or by I_{DDQ} testing on product level (Ref. 5). Most interesting for the customer of products from the new process is the point in time where the process defect induced EFR from the new process begins at the performance phase.

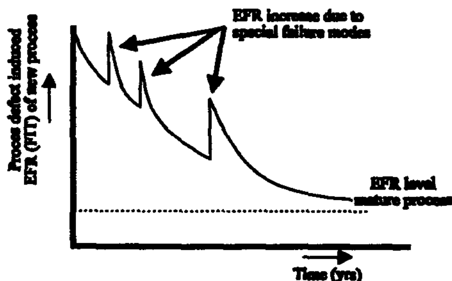

Fig. 4. *Process defect induced EFR maturity growth*

As an example we have sketched the development of process defect induced EFR as a function of time. The maturity growth is valid for many process aspects. Some of these can be PCM parameters, random yield, PPM levels, etc. Process parameters that are under SPC typically develop in the same way. This is given in Fig. 5.

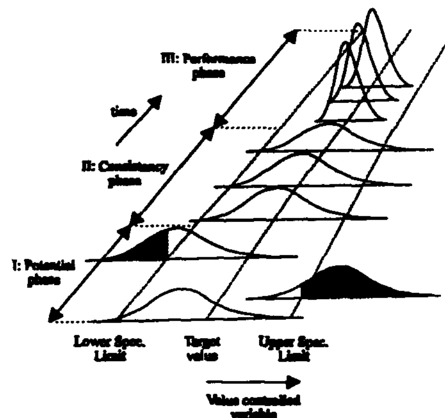

Fig. 5. *Different phases during process life of process variables under SPC*

In Fig. 5 the following three phases can be distinguished.

1. Potential	At the end of this phase the process is able to produce devices that conform to function and reliability (end of life) requirements.
2. Consistency	At the end of this phase all special causes of variation are eliminated so that the yield and early life failure rates are stable.
3. Performance	During this phase common cause (inherent) variation is reduced such that quality and early life failure rates are met.

In the previous examples we have shown how the SPC controlled variables as well as non SPC controlled variables typically develop as the production process grows to a mature process. This trend is valid for many process aspects and therefore a similar trend can also be found in the overall process capability. In Fig. 6 an example is given of how the overall process capability changes during a process lifetime.

In Fig. 6 two lines are drawn. One is indicating the process capability of an existing mature process. The other line describes the process capability of a new process which technology resembles the mature

process (e.g. only the minimum dimensions are smaller).

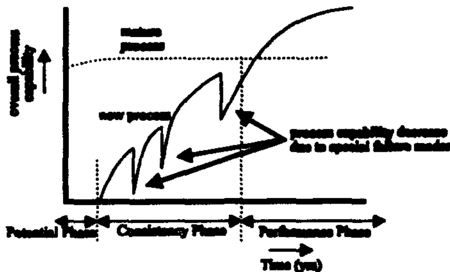

Fig. 6. *Typical process capability of a mature and new manufacturing process*

We see that the mature process has a stable process capability. The capability of the new process is at the start less than the capability of the mature process but when the new process becomes mature its capability will become better than the existing process. Most interesting for customers is the point in time where the capability of the new process becomes better than the capability of the existing process.

Because the process capability of a new production process depends so much on the maturity of the process we developed a simple method to monitor process maturity growth.

Monitoring process maturity growth

In order to monitor the maturity of the process on a regular basis we will use maturity grids. Maturity grids are two dimensional drawings in which the maturity of one process aspect can be indicated. The maturity grid can have any size but for the sake of simplicity we will use example grids that have four columns and four rows making a total of sixteen fields. This grid is shown in Fig. 7. The maturity grid is a risk assessment tool. This means that a customer can rate the risk that certain process aspects has for the products he buys from the supplier for his application. A risk for the customer can be defined as the product of the chance on failures and the severity of these failures for the customer. Thus:

Risk for customer =
P(failures) * Severity(failures)

Along the horizontal axis of a maturity grid the chance for failures is indicated. Along the vertical axis the severity of the failures for the customer are indicated. An example maturity grid is drawn in Fig. 7.

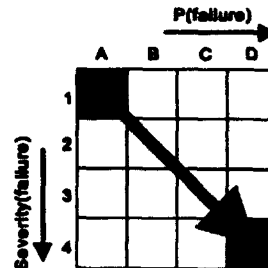

Fig. 7. *An example of a maturity grid*

Position A1 is the area with the highest risk. Position D4 is the area with the lowest risk. As the suppliers process gets more mature process items will shift from the upper left corner to the lower right corner in the maturity grid, typically somewhere along the diagonal line, as indicated by the arrow in Fig. 7.

To give a technical example of a maturity grid, in Table 2 we have given the values along the axis for the risk for the customer with respect to EFR. Although the values along the horizontal axis are purely illustrative the chance for failures is given by the EFR of similar products in the same production process. The consequence of a failing device due to process defects is likely to be that the application of the customer does not work according to specification. The severity of this problem for the customer largely depends on the ability of the supplier to decrease the EFR. There is a large difference in severity between the situation that the supplier faces a process limit or the situation that the supplier will on short term be able to improve the EFR. Therefore the vertical axis indicates the severity of the problem.

X-axis		Y-axis EFR (FIT)	
A	no improvement, equipment/ process capability limit	1	> 100
B	50% of all failures are of known cause	2	< 100
C	most failure modes are known, long term improvement	3	< 50
D	most failure modes are known, short term improvement	4	< 10

Table 2. ***Values along the axis for the maturity grid regarding EFR***

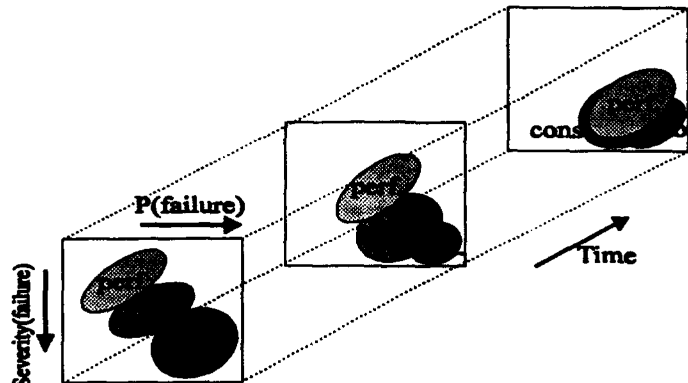

Fig. 8. *Expected process maturity growth*

In the approach presented in this paper such a grid is made for many process aspects that influence product quality and reliability. By stacking all the grids on top of each other it becomes clear which process items need most attention from the supplier and/or customer in order to improve product quality and reliability. In Fig. 8 a set of maturity grids is given that describes how the maturity of the process typically will develop as a function of time. In this figure the axes of the maturity grids have become continuous (Ref. 6). Given the maturity growth from Fig. 6 it is expected that process items from the potential phase will be mature before items from the consistency phase. After the consistency phase items from the performance phase will become mature.

An example

As was described before, during the maturity growth of a semiconductor manufacturing process for many process aspects three phases can be distinguished. These are the potential phase, the consistency phase and the performance phase. In Table 3 the customer concerns regarding these three phases are described.

process maturity phase	customer concern
potential phase	Is the process capable of delivering ICs that conform to functionality and reliability (end of life) requirements?
consistency phase	Are special causes identified and removed on time such that no delivery problems will occur?
performance phase	Are EFR and quality levels (PPM) met?

Table 3. *Customer concerns during process phases*

Process defect induced EFR has been the only failure mechanism that has been treated so far in this summary as an example failure mechanism. Of course in an actual process maturity assessment many more process items are reviewed. In this section we will shortly give an overview of the maturity grids that are used to assess an industrial submicron double metal CMOS process. Table 4 lists the most important items of which maturity grids are made. The items mentioned here are only top level items. In order to be able to assess process details while keeping an overall picture we have implemented a hierarchy in this process assessment. For example the EFR related maturity grid in the performance phase was given in Table 2. However if the maturity of this item is not D4 the supplier is asked to fill in more detailed maturity grids. These are based on a pareto of the most important failure modes (e.g. gate oxide, litho defects, inter-metal oxide particles). For each failure mode the maturity status must be indicated.

Potential	Technology maturity
	Library functionality
	Library reliability
	Reliability evaluation modules
Consistency	Special causes in-line failures
	Special causes ESORT failures
	Special causes PCM failures
	Special causes EFR failures
Performance	PPM risk factor
	Cpk PCM parameters
	Cpk in-line parameters
	EFR risk factor

Table 4. *Main groups of process items*

Within many of these groups detailed maturity grids are drawn. By stacking all top level maturity grids

we get a good overview which process aspects are the least mature for the product. At this moment we have implemented the approach outlined in this paper with one supplier of ASICs and ASSPs in a submicron CMOS technology. Since the method has been recently developed, at this moment only one maturity assessment has been done. Because the tool is still in an evaluation phase at this moment the method is used in addition to the traditional way of type qualification. In our experience so far, we have found that there are several advantages in using maturity grids for describing process maturity. Some of these are:

- the tool is easy to use, people responsible (e.g. process engineers, test engineers, reliability engineers) can fill in these maturity grids easily
- the maturity grids give a good overview which process items pose the highest risk for the customer of the ASICs
- by filling out the maturity grids on a regular basis it is possible to assess the process maturity as a function of time

Conclusions

Future reliability targets of ASICs and ASSPs can not be demonstrated by product life tests. These figures must be shown by the production process that produces these products. This requires a change in vendor/customer relationship.

The capability of the production process is not constant. As the process gets more mature the capability tends to improve. This is an important aspect for qualification of production processes.

Once the axes along the maturity grids are established, maturity grids are easy to use. By performing process maturity assessment on a regular basis the maturity can be found as a function of time.

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