Dealing with electrostatic discharge in a capacitive fingerprint sensor fabricated in amorphous silicon thin film technology

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Abstract—**In this paper a capacitive fingerprint sensor will be presented with ESD related considerations. The sensor is developed in our laboratory. The manufacturing process will be explained. The behaviour under ESD stress will be analysed. A solution for ESD protection will be proposed.**

Keywords—**fingerprint, electrostatic discharge, thin film transistor, amorphous silicon**

I. Introduction

A fingerprint is unique for each of us. Therefore it is since the middle of the nineteenth century used to identify a person. Nowadays a small electronic fingerprint sensor could be used to provide automatic recognition of individuals. It can be used to protect access to, for example, mobile electronic devices such as mobile phones or laptop computers, instead of a PIN (personal identification number) code, a key or a password. The area of possible application is very wide. The whole recognition system has to satisfy in the first place extraction of the features of a finger (the sensing element), and secondly matching and accuracy of the characteristics of an individual with previously recorded characteristics is needed.

Different types of the electronic fingerprint sensors are currently in use. Some of the possible image capture principles are:

- **Solid state sensors: based on the principle of capacitive coupling or temperature differences. Since this technology was introduced in the late 1990's, it is increasingly applied.**
- **Ultrasonic sensors: using acoustic waves. This technology is still in its infancy and has not yet been widely used.**
- **Optical sensors: reflection principle or with a tactile sensitive light-emitting foil. Optical technology is oldest, and is demonstrated and proven technology, but the optical sensors are bulky and costly.**

In this paper we will deal with the α-Si:H TFT sensor with capacitive coupling.

II. Capacitive principle

The capacitive fingerprint sensor in thin film technology was developed in Philips Research Laboratories, Redhill, UK, [1], back in 1994. Nowadays it is commercially manufactured by companies like Veridicom (OpenTouch), SGS Thomson (TouchChip), Infineon (fingertip), Sony (Puppy FIU-700). It is commonly known that the capacitive fingerprint sensor has a very good image quality but a poor durability due to ESD.

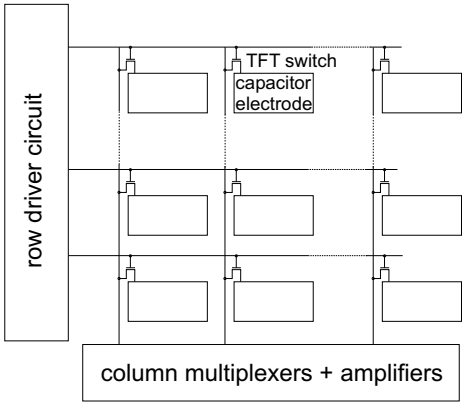

Fig. 1. A simplified schematic diagram of the sense elements together with associated addressing circuitry.

A fingerprint sensing device is a row/column array of sense elements which are coupled to a driving circuit. The sense elements are addressable by the drive circuit. An output from the sensing circuit in analysed in the recognition system. Characteristical data is compared with stored characteristical data for identification and verification purposes. A simplified schematic diagram of the array of the sense elements with the addressing circuit is shown in Fig. 1.

A. Working of the sense element

Each sense element contains a sense electrode and a switching device (e.g. a TFT) for active addressing of that sensing electrode. The sense electrodes of the sense elements are covered with an insulating layer, for example of silicon nitride or polyimide. If a person touches the sensor a capacitor is formed between the finger and each sensing plate. These capacitances are sensed by the sense circuit by applying a potential to the sense electrodes and measuring charging characteristics. Depending whether a ridge or a valley of a finger touches the sensor surface, the capacitor will have a higher or a lower value. A schematic representation of a sense element is shown in Fig. 2. The pixel plate

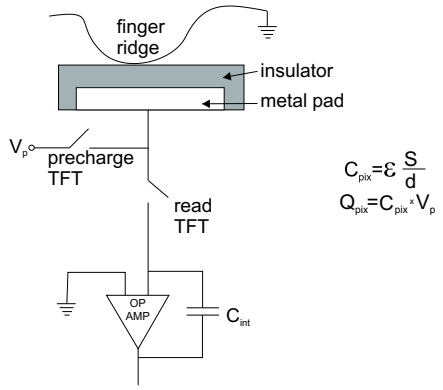

Fig. 2. Schema of the capacitive fingerprint sensor.

mask	material	thickness [nm]
1	Al	300
2	SiNx	350
3	α-Si:H	300
4	SiNx	300
5	Al/Mo	300
6	SiNx	350

TABLE I

TFT process flow with layer materials and thicknesses. Mask 1: gate metallisation, mask 2: etch stop, mask 3: drain and source implantation, mask 4: opening bottom metallisation, mask 5: topmetallisation, mask 6: passivation.

is precharged to the value V_p. The capacitance of the pixel is determined by the pixel plate area S and the distance between the pixel plate and the finger d. The amount of charge at the pixel plate is proportional to the precharge voltage and the pixel capacitance, $Q_{pix} = C_{pix} \times V_p$. An operational amplifier with capacitive coupling is used to integrate the charge. The output current is further handled by column multiplexers.

B. Fabrication of the capacitive fingerprint sensor

We made the capacitive fingerprint sensor based on thin film technology. The sensor is based on the bottom gate (inverted-staggered) α-Si:H TFT. The TFT's were n-channelled, with a silicon-nitride gate insulator. A schematic cross-section of a fingerprint cell is given in Fig. 3. As the thin film technology is used in well established technologies such as liquid crystal display devices, and as such it is described well (see for example [2]), here the technology of making the capacitive fingerprint sensor will be described only briefly.

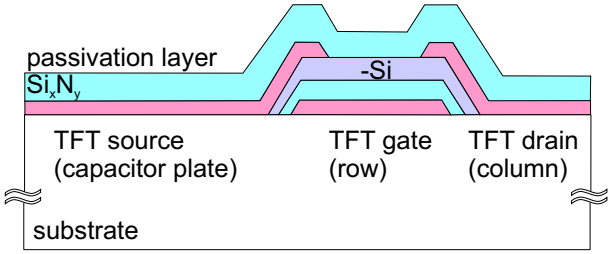

Fig. 3. Cross section of a pixel in the capacitive fingerprint sensor.

The fabrication process involves six photolithographic processes. These processes are listed in Table I.

As substrate material we used a Si wafer with a thick (1 μm) layer of thermally grown SiO_2. For the deposition of Al and Mo we chose sputtering. For the deposition of amorphous silicon and silicon nitride we used PECVD (Plasma Enhanced Chemical Vapour Deposition). The deposition temperature was 250 ^oC and the discharge frequency 13.56 MHz. Three layers (SiNx as the gate dielectric, α-Si:H as the TFT channel and SiNx as the etch stopping layer, protecting the channel from the following etching processes) are deposited without breaking the vacuum. Wet etching was used for etching of all layers, except for the second metallisation layer made with Molybdenum. To make a highly doped α-Si:H for the source and drain contacts, ion implantation through a thin (10 nm) Al layer, or 20 nm Mo layer was used. Implantation through Mo layer produced a better contact. We implanted both phosphorus and arsenic. Phosphorus implanted TFT's gave lower contact resistance. We also made a variations with the dose and energy when implanting phosphorus in order to optimise the implantation parameters for source/drain contacts. The devices were annealed at 280 ^oC for 1 hour.

C. Characterisation of α-Si:H and SiN:H films

The thicknesses of the films are determined by spectroscopic ellipsometry. The thickness of the α-Si:H layer is estimated at 295 nm (mean value) and the thickness of the SiN:H layer is estimated at 373 nm. Also the refractive index of SiN:H was measured and it showed the value of 1.71, which implies that the quality of the SiN:H is relatively good, as the value of the refractive index of the stoichiometric silicone nitride is about 2.

The structure of the α-Si:H layer has been verified by X-Ray Diffraction (XRD). There are no visible effects of annealing on the state of material.

The composition of the SixNy:H layer has been determined by X-ray Photoelectron Spectroscopy (XPS). The results show that the ratio between silicon and nitride is Si:N=1:1. The stoichiometric silicon nitride would have Si:N=1:1.33. The result implies that the composition of the silicon nitride could be improved. The presence of hydrogen is also determined by XPS. Hydrogen is found in 12.5 $\%$. The target value is 14%, so this could be improved as well.

D. Electrical measurements of deposited structures

On the wafer with a fingerprint sensor a number of testing structures , such as TFT's and capacitors, ESD protection chains, etc. was deposited in order to fully understand

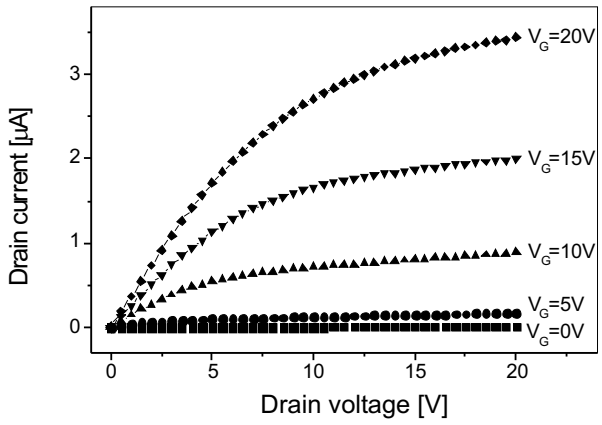

Fig. 4. Output characteristics I_D/V_D under different gate voltages V_G=0, 5, 10, 15, 20 V of a TFT with W/L=100/12.

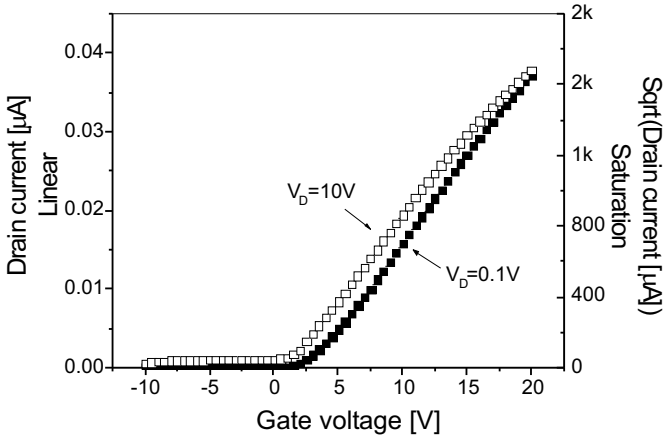

Fig. 5. Transfer characteristics I_D/V_G under different drain voltages V_D=0.1, 10 V of a TFT with W/L=100/12.

the performance of the fabricated sensor. Electrical measurements performed on these testing structures and on a pixel in the sensor matrix will be presented.

TFT's with different W/L ratios were deposited. In Fig. 4 and 5 measured output and transfer characteristics of a TFT with W/L=100 μm/12 μm are shown. From the measured characteristics electron mobility and threshold voltage are calculated. The threshold voltage is determined from the interception of linear fit of the linear part of the transfer characteristic in the linear regime of working with the x-axis (V_D=0.1 V). The value of the threshold voltage for the given TFT (Fig. 5) is 2.8V. From the same linear fit of the transfer characteristic in the linear regime of working, the field-effect mobility in linear regime μ_l is determined. The calculated value is μ_l=0.37 V/cm^2. The field-effect mobility in the saturation regime μ_s is calculated by fitting a straight line through $\sqrt{I_D}(V_G)$ curve measured in the saturation regime under V_D=10 V. The μ_s is 0.26 V/cm^2. For an ideal transistor, the field-effect mobilities calculated in both the linear and the saturation regime should be equal. But due to the neglection of the series resistance and also due to imperfect linear fitting a mismatch between μ_l and μ_s happens in practice.

The electrical characteristics of a pixel of the fingerprint sensor matrix measured before it was passivated are shown in Fig. 6. The figure shows that the TFT in the matrix does operate as a switch. The dimensions of the TFT's in the matrix are W/L=21 μm/8 μm and therefore the level of the drain current is proportionally lower then in Fig. 4.

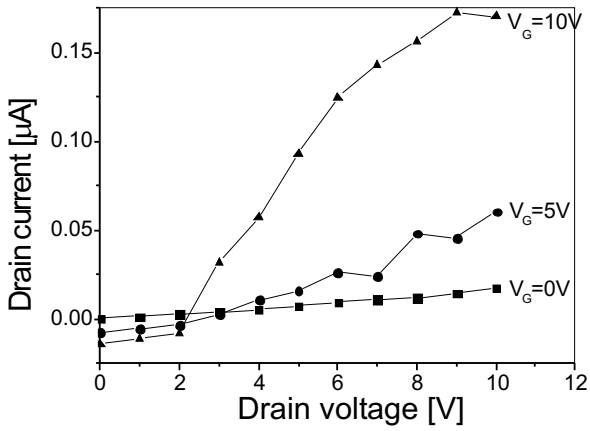

Fig. 6. Output characteristics of a TFT switch in the fingerprint sensor matrix.

D.1 Testing of TFT chains

Chains of five TFT's in a serial connection (Fig. 7) are used for each row and column protection. The chains are connected to a single guard ring. Single protection chains were designed on the test part of the sensor. The chains were built in three variations of TFT's, with channel width and length of $160\mu m/64\mu m$, $80\mu m/32\mu m$ and $40\mu m/16\mu m$. The chains were tested, applying the stepped voltage up to 100V on the one side of the chain, having the other connec-

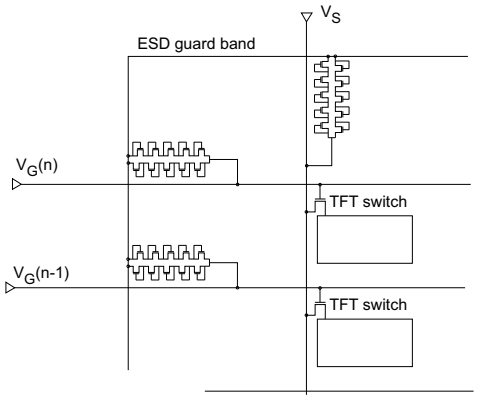

Fig. 7. TFT's chains in the fingerprint sensor.

tion grounded. The result of the measurements is shown in Fig. 8.

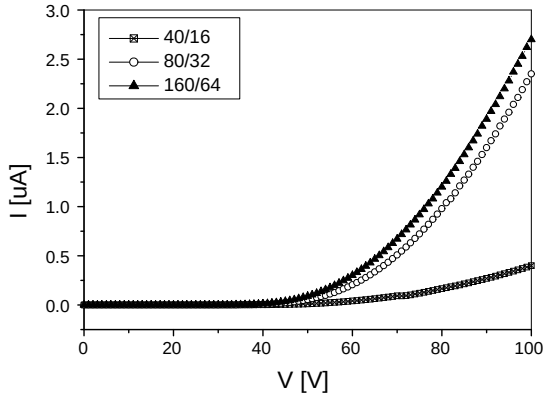

Fig. 8. Measured characteristics of TFT's chains with different channel widths and lengths.

From the Fig. 8 it can be seen that all of the three chains switch on at about the same voltage of 40 V. That is consistent with the measured threshold voltage of a single TFT. The larger TFT's produce a higher current under the same voltage. The current is in the order of μA.

III. Description of the ESD problem

In a capacitive fingerprint sensor a possible ESD zap is applied either directly to the capacitive sensing element by the person who is using it or during the assembly process by a machine. The latter problem is successfully solved using the diode/TFT chains, and shortening all columns and rows during the manufacturing.

In the case when an ESD zap is applied directly to the sensing element, it is very difficult to find a good solution to protect the circuit. Under ESD stress, a possible current path goes through the top capacitance down to the ground Fig. 9). The elements in this path that have to be protected against ESD are:

1. the capacitor
2. the column "read" TFT
3. the amplifier circuits.

The most difficult task is to make the capacitor (actually the top dielectric layer) ESD insensitive. The idea is that the top layer must not be fully insulating. A resistive path must exist.

One solution that comes to mind immediately is to construct protection rings, i.e. walls of a conductive material connected to the ground around each pixel. These walls are generally obtained by gold electroplating in order to prevent oxidation [3] or of copper encapsulated by ruthenium, which is well known as a contact material and whose oxide is conductive [4]. This solution would certainly protect the sensor against the ESD up to a certain level, but it will introduce some additional problems. First is that the number of photolithographic masks will be increased, making the sensor more expensive (for applications like mobile phones it is very important to keep the price low). In some cases it can cause water penetration from the sensor surface to the active area [3].

Another possible solution is to make good choice of material used for the top dielectric layer. It should satisfy three conditions: to give ESD protection, to avoid charge loss in the capacitor and to not allow reduction of effective resolution. The easy solution for the last condition is good choice of the capacitor dimensions. In case the dimensions of the capacitor are: area $A = 50\mu m$ x $50\mu m$, insulator thickness $d = 500nm$ and distance between two cells $x = 10\mu m$ then the ratio of resistances in lateral and vertical direction is $R_s/R_p = 1600$. This ratio should provide good effective resolution of the sensor, as the lateral component of the current is almost negligible. Also, it may be possible to use material which is conductive in only one, for example vertical and not in lateral direction.

To avoid charge loss it is desirable to keep the insulator thin. This may counteract to the ESD robustness of the layer. The effect of the resistive layer may be presented as a parallel connection of a capacitor and a resistor, as it is shown in Fig. 9. Considering ESD conditions, the resistance R_p

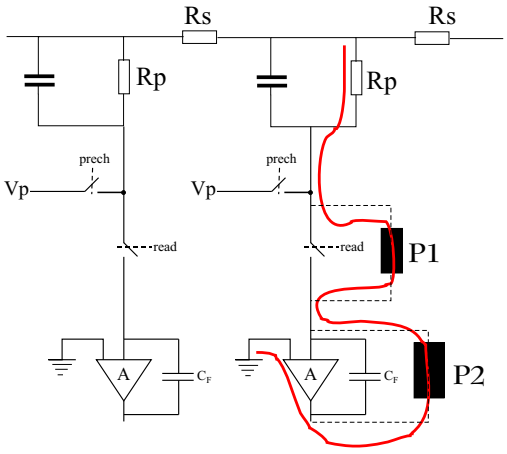

Fig. 9. Current path in the capacitive fingerprint sensor.

will take the ESD current (the current through R_s may be neglected as sufficiently lower). We have to determine how large this resistance should be in order to protect the surface layer and also not to influence too much the operation of the circuit under both DC and ESD conditions. There are two issues that have to be mentioned. First is that the current through the surface layer will produce power dissipation, $P = V_{Rp}^2/R_p$, which leads to heating. To simulate thermal behaviour of the surface layer would be straightforward using Silvaco tools, if the material (which will be used for the capacitor) were included in the simulator. If the resistive layer is a moderate thermal conductor it can be expected that the peak of the temperature distribution will be at the surface, and that the peak of the temperature in the resistive layer will be lower when the layer is thicker (R_p higher). On the other hand, this resistive material could be a very

poor thermal conductor or a very good thermal conductor. In both cases the thickness of the resistive layer would not play a role at the temperature distribution, as in the former case the temperature would be localised at the surface, and in the latter case the temperature would be transfered without losses to the rest of the sensor. Another issue important for ESD protection is that the current through the resistor R_p should produce a voltage drop sufficiently large to provide that the voltage on the TFT switch, which is directly connected to the surface layer via a metal plate, is never higher then the breakdown voltage of the TFT gate dielectric layer? In our case that is 330 nm Si_xN_y, having around 350 V breakdown voltage. In this way the TFT switch would be protected and the element P1 in Fig. 9 would not be needed.

Considering the ESD protection under the TFT switch (Fig. 9), it would be necessary to design the protection devices that will provide the path to the ESD current. It seems to be the second most important issue, after setting a proper material for surface. If this part of the sensor would be realised also in amorphous silicon thin-film technology, choice of the elementary structures for building a ESD protection would be very limited. The devices that one could use for protection elements P1 and P2 are only non-snapback type of protection structures, like:

- **chains based on TFT's used as diodes - made by coupling the gate and the drain directly together. This structure is already successfully used for each of the input and output terminals at the edge of the glass substrate.**
- **TFT's - as this devices never go to snapback, they can be used only in a non-breakdown mode. Normal MOS design can be used, as well as GC TFT (Gate coupled TFT) (Fig. 10). Considering transient regime, an appropriate choice of R and C would help to provide that TFT would turn-on only under a ESD zap.**
- **It would be also possible to use TFT's with a thick gate dielectric, to increase the breakdown voltage. A specific structure based on thin film technology could be designed and implemented for the protection element P1/P2 in Fig. 9.**
- **High voltage TFT. For the switch a high voltage TFT (with the drain extension L_D, as shown in Fig. 11) could be used. It would be used in connection to the resistor R_p with its drain, and would ensure that the electric field in the gate dielectric is such that TFT can withstand higher voltages. Instead of typical breakdown voltage of 350 V, it could be easily increased up to 600 V, as reported in [5].**

A. ESD robust concept: resistive or pressure sensing?

From the manufacturing point of view, the simplest way to protect the capacitive fingerprint sensor from the electrostatic charge of the human operating the sensor, would be a surface layer, which would provide both good dielectric properties to allow for the capacitive sensing and good resistive properties for giving the "low"-resistive path for the ESD current [6]. Unfortunately it is very difficult to optimise material properties to satisfy all above mentioned conditions.

Another possible solution is to change slightly the concept

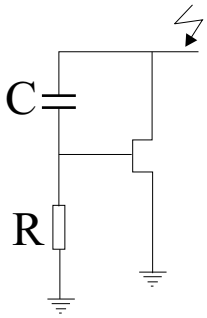

Fig. 10. Gate coupled TFT.

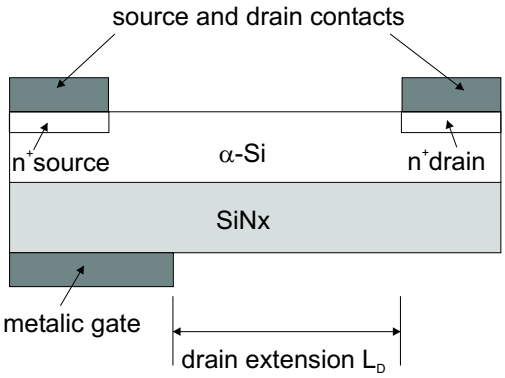

Fig. 11. High voltage TFT.

of the sensor and to use resistive instead of capacitive sensing. The basic schema of the circuit could remain similar as in Fig. 9. Instead of the integrator an operational amplifier would be used for the amplification of the signal. The problem with the resistive sensor is that the current path would have to be closed through the human body. Although that is an almost negligible effect, many people would object to this approach.

The idea of the resistive fingerprint sensor could be also combined with the pressure sensing, using the piezo-resistive effect. In the piezo-resistive effect the electrical resistance of silicon changes with external pressure. At constant temperature, the resistance R of a semiconductor element of area A, length l, resistivity ρ is $R = \rho\frac{l}{S}$. When the element is strained (e.g. pressed) the resistivity changes by an amount:

$$\Delta R = (\frac{\delta R}{\delta l})\Delta l + (\frac{\delta R}{\delta \rho})\Delta \rho + (\frac{\delta R}{\delta A})\Delta A = \frac{\rho}{A}\Delta l + \frac{l}{A}\Delta \rho + \frac{\rho l}{A^2}\Delta A \quad (1)$$

$$\frac{\Delta R}{R} = \frac{\Delta l}{l} + \frac{\Delta \rho}{\rho} - \frac{\Delta A}{A} \quad (2)$$

A CMOS compatible micromachined tactile fingerprint sensor has been reported in [7]. It would also be possible to use this approach in amorphous and polysilicon thin film technology. Piezoresisistive properties in polysilicon are affected by microstructure (fabrication process) and electrical properties (doping level). Unfortunately the micromachining part of the circuit would be quite expensive. The rest of the circuit is very simple, composed from passive compo-

nents only. This concept is ESD robust, as the micromachining part, which is in direct contact with the human body, is not electrically active.

IV. SUMMARY

We have manufactured a capacitive fingerprint sensor with α-Si:H TFT's used as switches. The design, the process flow and the test measurements have been showed in this paper. The sensor is used for an theoretical ESD analysis. The behaviour under an ESD stress has been described, and possible ESD solutions have been discussed. Some ideas for an ESD robust fingerprint sensor have been proposed.

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