Range Pre-selection Sampling technique to reduce input drive energy for SAR ADCs

Harijot Singh Bindra[1], Joeri Lechevallier[1], Anne-Johan Annema[1], Simon Louwsma[2], Ed van Tuijl[1,2], Bram Nauta[1]

[1] Integrated Circuit Design, University of Twente, [2]Teledyne DALSA

Enschede, The Netherlands

Abstract*—A Range Pre-selection Sampling (RPS) technique is introduced to reduce the input drive energy for SAR ADCs and is applied to a 10-bit 2MS/s SAR ADC in 65nm CMOS in this paper. Using the proposed RPS technique, the peak input sampling current and hence the input drive power requirement is reduced by a factor 2.4 as compared to conventional sampling (CS). Considering an ideal Class A operation for the buffer circuit driving the ADC, this translates into a minimum (theoretical) driver power consumption of 50µW for our RPS based ADC whereas it is 130µW for the conventional sampling, both much larger than the ADC power consumption of 3.25µW at 1MS/s operation. Our ADC occupies an area of 0.08 mm^{2}and achieves an SFDR of 64 dB, an SNDR of 55 dB with a Walden Figure of Merit, FoM$_W$ of 6.8fJ/conversion-step at up-to 2MS/s.** ***Keywords—Nyquist sampling; input driver; SAR; Walden Figure-of-Merit

I. Introduction

SAR ADCs are widely used for low power data acquisition applications e.g. in wireless sensor nodes. Most of the recent techniques found in literature [1-4] emphasize on lowering the Walden Figure of Merit, FoM$_W$ which now seems to saturate near to 1fJ per conversion-step [1,2]. In data acquisition systems targeted for low power wireless sensor nodes in IoTs, peripherals for microcontroller units (MCUs), the energy consumption of the associated signal processing and the analog front end circuitry to drive the ADC inputs can be much higher than the ADC power consumption. More importantly, for these IoT applications, the analog front end driving the ADC has to be always ON to present the signal to the ADC for conversion and further processing without significant latency or loss of critical information in case of any event detection. This calls for a greater attention to be paid to minimize the *input drive energy* of an ADC [10]. The goal of this work is to present a Range Pre-selection Sampling (RPS) based SAR ADC which helps to reduce the amount of energy required to drive the ADC inputs, so that the combined energy per conversion of driver plus the ADC is reduced.

II. Walden FoM vis-à-vis Input Drive Power

For state-of-the-art FoM$_W$ ADCs, V_{SUPPLY} is below 1V, typically 0.4-0.7V [1-3,7,9]. Although this aids in lowering the power consumption of the mostly digital SAR ADC, it presents a greater challenge in driving the ADC as the supply voltage scaling demands a higher sampling capacitor, C_S in order to meet its kT/C requirement. The minimum required input power to drive an ADC is estimated for state-of-the-art FoM$_W$ SAR ADCs and compared with the ADC power consumption P_{ADC}. An estimation for an ideal Class A driver current required for slewing and linear settling, for near Nyquist rate sampling is $I_{DR,MIN} = N \cdot C_S \cdot (\Delta V_{MAX}/T_{TRACK})$. Here ΔV_{MAX} is the maximum signal change on the sampling capacitor C_S and N is the number of time constants (assuming 1 for slewing and SNR/9 for linear settling) required for ½ LSB settling at the end of tracking period T_{TRACK}. T_{TRACK} is typically 10-20% of the clock period, $1/f_S$ [8,11]. As shown in Table 1, $I_{DR,MIN}$ is typically orders of magnitude higher than the ADC supply current for the respective ADCs. For a driver operating at a supply voltage, V_{DD} and considering a track period of 10% of the clock cycle, the minimum (theoretical) required input drive power for an ideal Class A driver $P_{IN,MIN} = V_{DD} \cdot I_{DR,MIN}$ [5,6,8] for state-of-the-art FoM$_w$ ADCs is also shown in Table 1.

It can be concluded that the actual bottleneck for low power data acquisition systems lies in driving C_S which is not represented by FoM$_W$. This paper presents a 10b charge redistribution DAC (CDAC) based SAR ADC which introduces a Range Pre-selection Sampling (RPS) technique to reduce the ΔV_{MAX} and thereby reducing the input driver power without affecting the Dynamic Range. Compared to conventional sampling (CS), the RPS technique results in lower peak input sampling currents thereby resulting in a lower input drive power P_{IN} and consequently reduced energy consumption for the driver and ADC together.

III. Sampling technique and ADC Architecture

To demonstrate the RPS technique, we designed a SAR ADC that can be configured for either RPS or CS modes through an RPS_EN signal, Fig.1. For simplicity the single-ended architecture is shown. In actual differential implementation, V_{DAC+} is compared to V_{DAC-} (instead of V_{HALF}). The system consists of 3 CDACs, each sampling 1/3rd of single-ended input voltage range 0-V_{PK}. This range pre-selection sampling technique limits the maximum voltage change at each sampling capacitor to $V_{PK}/3$ while ensuring overall full-scale operation. Effectively this reduces the maximum required input drive power at high (near Nyquist-rate) frequencies, where conventionally it is the highest.

The ADC uses a split-capacitor DAC with a unit element of only 140aF. The total DAC capacitance for each CDAC is 145fF which is close to the kT/C limited value of 100fF for 10bit accuracy for 2V peak-peak differential input. To minimize glitches due to offsets between the 3 CDACs they share a common comparator. Each of the CDACs employ step-wise (dis)charging for the 3 most significant bits in the DAC array [4]. In addition, the ADC uses an event-driven control logic designed to operate at sampling rates from 10kS/s (limited by the bootstrapping S/H circuit) up-to 2MS/s at a 1V supply, maintaining almost constant FoM$_W$ for a fixed supply voltage for the wide sampling range.

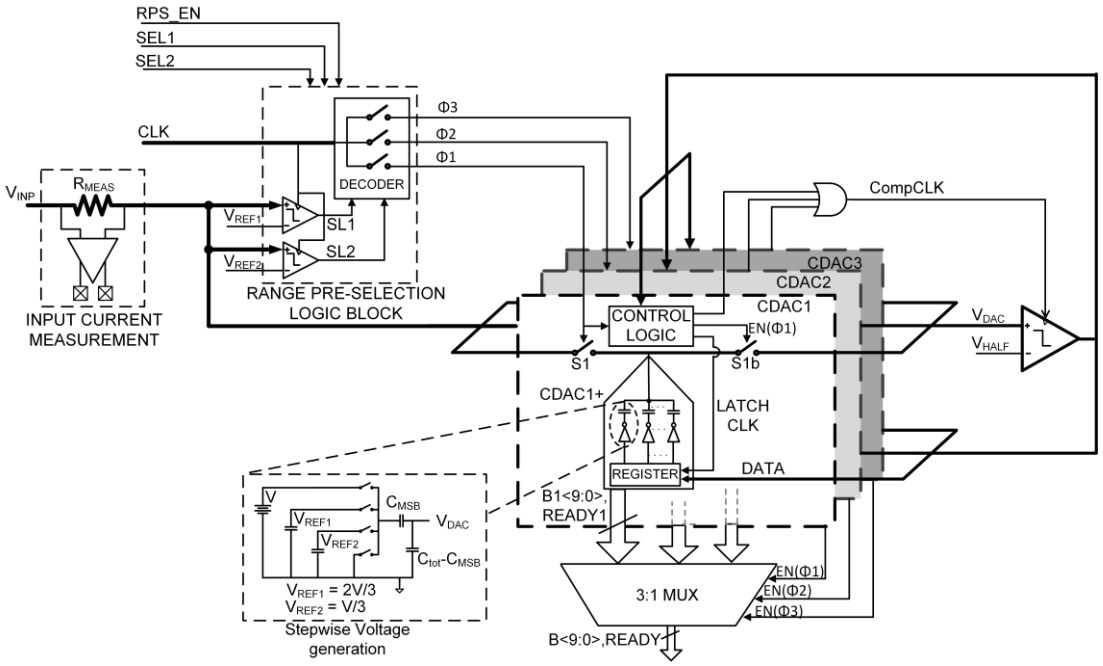

Fig. 1. Charge redistribution SAR ADC Architecture integrated with Range Pre-selection Sampling (RPS) technique

As shown in Fig.1, for the RPS mode, the range pre-selection (RPS) block determines before sampling in which range the input signal lies by comparing V_{INP} and V_{INN} to V_{REF1} (generated from the stepwise (dis)charging in the DAC array [4]). Depending on the RPS block output, CDAC1, CDAC2 and CDAC3 samples the inputs for Range 1, 2 and 3 respectively. Please note that in Fig.1 for simplicity, only V_{INP} is shown to be compared with V_{REF1} and V_{REF2} in the RPS block. However, in actual implementation due to symmetrical nature of differential inputs, both V_{INP} and V_{INN} are compared to only V_{REF1}. In the presented RPS technique, the three ranges expressed in terms of V_{INP} and V_{INN} are :

Range 1: $V_{INP} > V_{REF1}$ and $V_{INN} < V_{REF1}$,
Range 2: $V_{INP}, V_{INN} < V_{REF1}$,
Range 3: $V_{INP} < V_{REF1}$ and $V_{INN} > V_{REF1}$.

Based on the output of RPS block, either the signal Φ_1, Φ_2 or Φ_3 enable the corresponding CDAC and disables the other two. For e.g. if CDAC1 is selected, the corresponding bootstrapped S/H switch (S1) is enabled. After sampling, the corresponding enable signal ($EN(\Phi_1)$) turns on the switch (S1b) to connect the selected CDAC (CDAC1) to the comparator input to perform the SAR conversion cycle. When the switch S1b is OFF during sampling, the main comparator inputs are pre-charged to zero to dispose of any charge from the previous SAR conversion, thereby resulting in no ISI.

Fig.2 shows the timing information together with the DAC voltages during an A/D conversion of near Nyquist rate inputs for both the RPS and CS techniques. In CS mode, RPS_EN is disabled and SEL1/SEL2 is used to select one of the CDACs to sample V_{INP}/V_{INN} on its differential DAC, CDAC+ /CDAC-. As shown, the maximum voltage change ΔV_{CS} occurs at the sampling capacitor when sampling full-scale inputs (0-V_{PK}) as V_{INP} and V_{INN} are always sampled onto the same CDAC+ and CDAC- respectively. This is in contrast for the RPS mode, wherein the RPS block selects

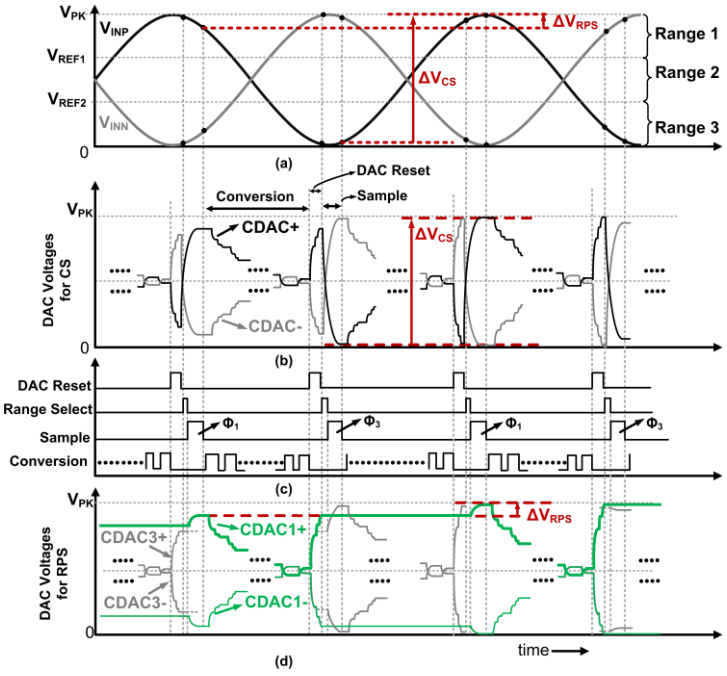

Fig. 2. (a) Input signals, V_{INP} and V_{INN} for near Nyquist rate sampling (b) DAC voltages for CS (c) Timing signals for RPS technique (d) DAC voltages for RPS based ADC highlighting the reduction in ΔV_{RPS}. For near Nyquist rate operation when V_{INP} & V_{INN} alternate between Range 1 and Range 3 at each successive sampling instant, then CDAC1 and CDAC3 are also selected alternately to respectively sample inputs in Range 1 and 3. This is highlighted by alternate selection of CDAC1 and CDAC3 in (d).

one of the CDACs to sample the inputs V_{INP} and V_{INN} depending on the range of the input signal. For example, for near Nyquist rate input frequencies when V_{INP} & V_{INN} alternate between Range 1 and Range 3, the RS block selects CDAC1 and CDAC3 alternately to sample the inputs. The maximum change (ideally) that can occur across CDAC+/CDAC- for any of the selected CDACs in RPS mode is thus $V_{PK}/3$. This happens for instance when V_{INP} changes from $V_{PK}(0)$ to V_{REF1} (V_{REF2}) for

CDAC1+(CDAC3+) or from V_{REF1} to V_{REF2} for CDAC2+ at successive sampling instants. This means that the peak input sampling current required for RPS is (ideally) 3 times lower than that required for CS and the input drive power requirement can be also lowered by a factor of almost 3 for the RPS technique. For low input frequencies, when the change in input signal is less than $V_{PK}/3$ at each successive sampling instant, both the RPS mode and CS mode have similar peak input sampling current. For minimum power, the comparators in the RPS block are scaled down in size compared to the ADC main comparator. Since the information from the RPS block is only used to select the S/H switches, the accuracy of its comparators and the reference voltages (V_{REF1}, V_{REF2}) does not affect the final conversion accuracy. So even if the comparator's output in the RPS block would be incorrect, the ADC output is still *correct*. In addition to the output bits and the READY signal, the output of RPS block (SL1, SL2) is also buffered as output from the chip, indicating to which CDAC the output bits correspond to.

A measurement resistor, R_{MEAS} is placed in series with the input paths leading to the S/H switches to measure the ADC's sampling current profile. In order to settle with > 10 bit accuracy, the input impedance R_{IN} should satisfy the ½ LSB linear settling requirement at the end of tracking period, $N \cdot R_{IN,MAX} \cdot C \leq 1/(10 \cdot f_S)$. R_{MEAS} is chosen as 1kΩ so that together with the bootstrapped S/H switch resistance (small signal) R_{SW} of approximately 7kΩ in our ADC, total input resistance $R_{IN} = (R_{MEAS}+R_{SW})$ is a factor 6 lower than the theoretical limit $R_{IN,MAX}$ (small signal) of approximately 50 kΩ. On-chip amplifiers measure the voltage across these resistors; their outputs are probed off-chip using a 20GS/s Keysight sampling scope.

IV. Measurements and Results

Fig. 3 shows the die micrograph fabricated in a standard 65nm CMOS process with an active area (including decaps) of 0.08 mm².

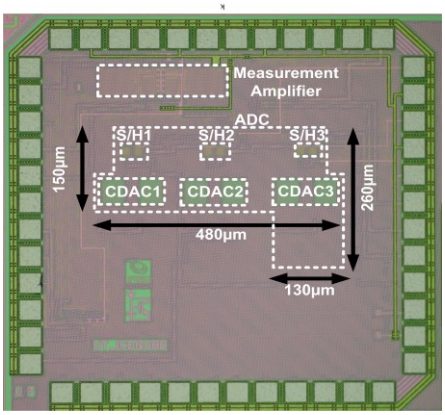

Fig. 3. Chip photograph

As evidenced by the sampling current profiles for RPS and CS in Fig.4 measured for near Nyquist rate sinusoidal input, the peak input current for RPS is reduced by a factor 2.4 for f_{IN} near to $f_S/2$. Note that the peak input current for the RPS based ADC occurs when sampling the inputs in range 2, and not in range 1 or 3 as for CS. Fig.5 shows the simulated peak input sampling current for both RPS and CS along with measured data points as function of f_{IN} for sinusoidal inputs. The overall peak input sampling current

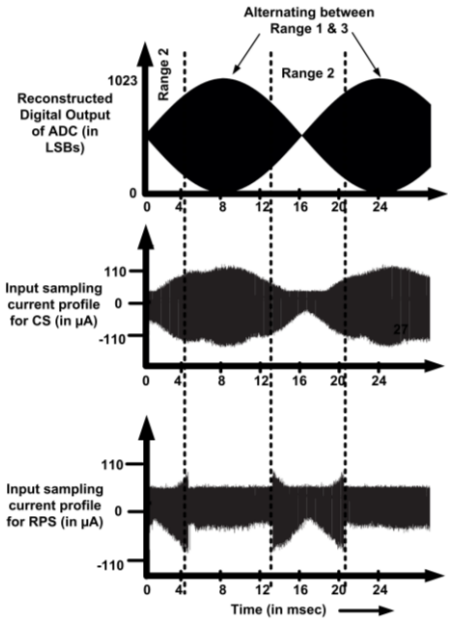

Fig. 4. Measured sampling current profile envelope at Fs–2*Fin, for both CS and RPS for Fin = 499.96875kHz and Fs = 1MHz. The high density in the plot represents the envelope of the near Nyquist input signal and the corresponding input sampling currents in CS and RPS mode, measured by a 20GS/s Digital Oscilloscope.

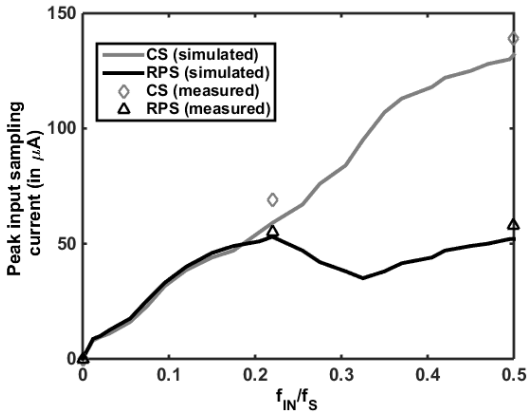

Fig. 5. Peak input sampling current of the RPS and CS based ADCs sampling current profiles as seen in Fig.4 for various input frequencies

for RPS over the entire input frequency range is 2.4 times lower in comparison to CS. Please note that the ADC drivers e.g. source followers are designed to handle maximum drive (peak sampling) currents to allow for initial slewing and linear settling. This implies that for a Class A input driver for the ADC, the input drive power P_{IN} can be decreased by at least a factor 2.4 using RPS. Using the expressions in Section II for e.g. for an ideal Class A behavior, P_{IN} is found to be reduced from 130µW for CS to 50µW for RPS, for P_{ADC} of only 3.25 µW at 1MS/s. This shows that the driver power is dominant over the ADC power consumption and hence the reduction in P_{IN} by a factor 2.4 for RPS technique is quite noteworthy. Please note that this reduction in peak input sampling current by factor 2.4 is less than the theoretical value 3 which happens in case of (ideal) impulse sampling with zero track time. Fig. 6 shows that the design achieves 64dB SFDR and 55dB SNDR with 8.9 ENOB at a 1.7V peak-peak differential input using RPS. A design error resulted in

unequal interconnect parasitic between each CDAC to the common comparator thereby resulting in systematic gain mismatch. The gain mismatch of the three CDACs was measured over 7 samples. The resulting systematic gain error was calibrated one-time in the foreground for the RPS mode. As shown in Fig.7, the ADC has +0.9/-0.95 LSB DNL and +1.4/-1.1 LSB INL (after foreground calibration) for RPS mode over 7 samples. This is similar to the measured +0.8/-0.85 LSB DNL and +1.1/-1 LSB INL for the CS mode. Our RPS based ADC achieves a FoM_W of 6.8fJ/conversion over a sampling rate from 10kS/s to 2MS/s, comparable to state-of-the-art SAR ADCs offering such a wide range of sampling frequency [7,9]. Please note that there is no degradation in FoM_W due to the RPS technique in comparison to CS, thereby confirming that it does not degrade the SAR ADC performance. Although the RPS technique does seem to have an area penalty, however from a system perspective (including driver) the reduction in the bias current requirement of the preceding driver stage by a factor 2.4 outweighs this DAC area overhead. Also the CDACs which are disabled for a selected range act as additional decap.

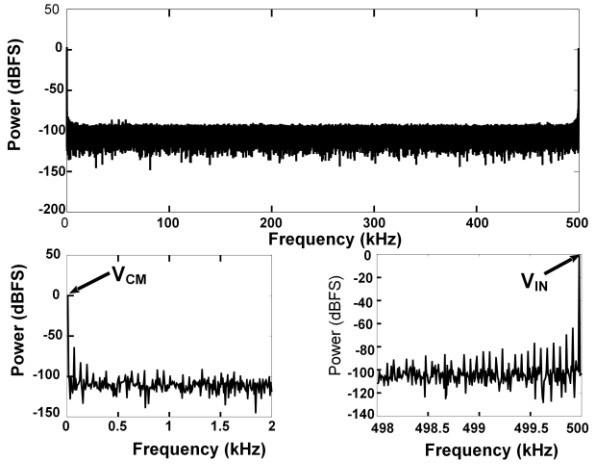

Fig. 6. FFT of the measured RPS based ADC output, normalized to the input tone Fin = 499.96875kHz and Fs = 1MHz.

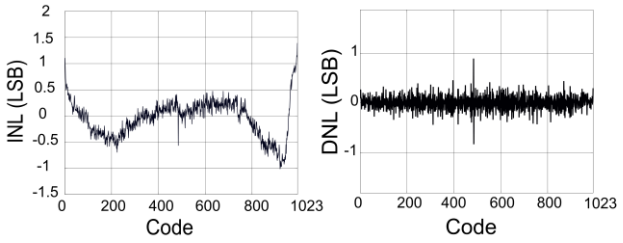

Fig. 7. INL DNL characteristics of the ADC in RPS mode. INL shown is obtained after foreground calibration done for systematic gain mismatch for 3 CDACs. DNL performance is not impacted by the gain mismatch.

Table 1 compares the performance of the proposed RPS based SAR ADC to state-of-the-art FoM_W SAR ADCs. It is to be noted that the measured power for both RPS and CS in our ADC is approx. a factor 3 more than the theoretical minimum. This is because R_{IN} (large signal) is almost 3 times less than $R_{IN,MAX}$ to avoid limiting the linearity of the SAR ADC at the front end sampler for the wide sampling range up to 2MS/s and to meet ½ LSB tracking bandwidth. Since the peak sampling current is equal to the maximum voltage step divided by this R_{IN}, hence the measured peak sampling current and consequently the input drive power is approx. a factor 3 greater than the theoretical value.

Table 1 : Comparison of RPS based ADC with state-of-art FoM_W ADCs

Architecture	This Work		[2]	[7]	[9]
	SAR with RPS	SAR with CS			
Technology	65nm	65nm	90nm	65nm	90nm
Resolution[bits]	10	10	11	10	10
Supply [V]	1	1	0.3	0.7	0.7
Maximum Sampling Rate	2 MS/s	2 MS/s	600 kS/s	2 MS/s	4 MS/s
Ideal Diff. Input Swing, V_{PK-PK} [V]	2	2	1.2	1.4	1.4
P_{ADC} (in µW)	6.25	6.25	0.2	3.6	11
$I_{DR,MIN}$ (µA), Calculated input (driver) current	16	40	60	70	860
$P_{IN,MIN}$ (in µW), Calculated input power	16 @2MS/s	40 @2MS/s	36	50	600
P_{IN} (in µW), Measured input power	50	130	No data	No data	No data
ENOB [bits]	8.9	9	9.4	9.3	9
FoM_w (fJ/conversion)	6.8	6.4	0.44	2.8	5.2
Area (in mm^2)	0.08 (incl.decap)	0.05	0.04	0.05	0.04

V. Conclusion

A proof-of-concept for the Range Pre-selection Sampling (RPS) technique has been demonstrated in a 10b 2MS/s SAR ADC to reduce its input drive power requirement which is very seldom addressed. The RPS based SAR ADC reduces the peak sampling current requirement by 2.4 times as compared to CS. This 2.4x reduction in peak sampling current by RPS is 1.65 times higher than the reduction through energy reduced sampling technique as reported in [10]. Considering an ideal Class A behavior, the input power can be reduced from 130µW for conventional sampling to 50µW for the case of RPS in our ADC, while the ADC dissipates 3.25µW. Since the input driver power consumption is order of magnitude greater than the ADC power, this reduction in input driver power by a factor 2.4 is significant in reducing the overall driver plus the ADC power dissipation.

References

[1] Hung-Yen Tai et.al, "A 0.85fJ/conversion-step 10b 200kS/s subranging SAR ADC in 40nm CMOS", *ISSCC 2014.*

[2] S.-E. Hsieh et al., "A 0.44fJ/conversion-step 11b 600kS/s SAR ADC with Semi-resting DAC", *VLSI Symposium 2016.*

[3] P. Harpe, et al., "A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAR ADC with Data-Driven Noise Reduction", *ISSCC 2013.*

[4] M. van Elzakker, et.al., "A 10-bit Charge-Redistribution ADC Consuming 1.9mW at 1MS/s", JSSC 2010.

[5] B. Murmann, "Energy Limits in Current A/D Converter Architectures", *ISSCC Short Course*, *Feb. 2012.*

[6] A.-J. Annema, et. al "Analog circuits in ultra-deep-submicron CMOS", *JSSC* 2005.

[7] P. Harpe et al., "A 0.7V 7-to-10bit 0-to-2MS/s flexible SAR ADC for ultra low-power wireless sensor nodes", *ESSCIRC 2012.*

[8] B. Murmann, "Limits on ADC Power Dissipation" in *Analog Circuit Design,* Springer, The Netherlands, 2006, pp 351-356.

[9] C.Y.Liou et. al, "A 2.4-5.2fJ/conversion-step 10b 0.5-to-4MS/s SAR ADC with charge-average switching DAC in 90nm CMOS", *ISSCC 2013.*

[10] H.S. Bindra et. al " An energy reduced sampling technique applied to a 10b 1MS/s SAR ADC", *accepted at ESSCIRC 2017.*

[11] R. Kapusta, "Advanced SAR ADCs for high throughput applications", *ISSCC Short Course*, *Feb. 2017.*