Capacitive probing of electronic phase separation in an oxide two-dimensional electron system

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Interfaces between specific complex oxides host two-dimensional electron systems (2DESs) with strong electron-electron interactions. This combination yields a rich phenomenology, including an apparently intrinsic electronic phase separation (EPS). We designed an experiment to study the origins and magnitude of EPS in oxide 2DESs in more detail. We measure the capacitance between the 2DES at the LaAlO3/SrTiO3 interface and an electrode on top of the LaAlO3 as a function of applied gate voltage. Our measurements reveal a significant reduction of this capacitance in the region of the phase diagram where the charge-carrier density is low. The tunnel conductance is reduced as well, which implies that part of the interface becomes insulating. These measurements allow us to directly estimate the magnitude of the EPS at a carrier density of several \(10^{11}\) cm\(^{-2}\), higher than the nominal carrier density in most experiments. The pattern in the capacitance-voltage measurements reflecting the local metal-insulator transitions suggests that the main driver for EPS is a strong variation of the electrostatic potential with a non-normal probability distribution. We study the effect of this in-plane potential variation on the electronic properties of the 2DES by mapping the full superconducting dome as a function of both backgate and topgate voltage. This map shows that, once insulating patches emerge, the global critical temperature \(T_c\) falls, while the onset temperature—i.e., highest local \(T_c\)—remains fairly constant.

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I. INTRODUCTION

Two-dimensional electron systems (2DESs) in complex oxides have received considerable attention since their discovery about two decades ago [1,2], because they combine the rich physical phenomenology of complex oxides with that of low-dimensional electronic systems [3–6]. Like classical semiconducting 2DESs, oxide 2DESs are highly susceptible to externally applied electric fields [7–9], holding promise for field-effect devices [3,10,11]. For example, the field effect can be used to tune \textit{in operando} physical properties such as the critical temperature for superconductivity \(T_c\) [9,12–15], electron mobility [16,17], spin-orbit coupling strength [18,19], and Fermi surface topology [20,21]. Possible correlations between these—fundamentally not yet fully understood—physical phenomena can be studied accordingly.

A major obstacle for proper studies of such correlations is the in-plane heterogeneity observed for many of these properties. The archetypal LaAlO3/SrTiO3(001) interface is the best-studied example [22]. Transport experiments showed that the interface responds to magnetic fields in a way that suggests multiple phases exist in parallel [23,24]. In addition, scanning-probe imaging revealed strong in-plane variations of the superfluid density [25,26], current density [27–29], surface potential [30], magnetic response [25,31], \(T_c\) [32], and conductivity [33,34]. Importantly, the magnitude of the variations is on the scale of the average for each of these quantities. Global superconductivity is affected accordingly: the transition as a function of temperature is wide [35–38], the system exhibits Josephson-like dynamics [39], and the superfluid density collapses on the “underdoped” side of the superconducting dome [40].

All these observations point towards electronic phase separation (EPS), which can be caused by several extrinsic and intrinsic phenomena. Compared to semiconductor compounds, oxide interfaces are more prone to both. Extrinsic causes for EPS include the rich palette of (charged) defects that can possibly form in oxides [41,42] and the different crystal symmetries oxides may attain—for example, SrTiO3 becomes tetragonal below 105 K [43]. Such phenomena cause lateral variations of the local electrostatic potential [30,44] and thus of the local charge carrier density.

Intrinsic EPS is typically the result of a thermodynamic instability characterized as a drop in chemical potential upon adding carriers—a phenomenon known as negative electronic compressibility (NEC). NEC emerges in all 2DESs close to depletion [45,46], where electron-electron interactions dominate the kinetic energy. The electron system at the LaAlO3/SrTiO3 interface is (quasi-)2D [47,48] and has long-range electron-electron interactions because of the high permittivity of SrTiO3 [49,50]. Hence, NEC was shown by capacitance measurements to be particularly strong in the 2DES of interest here [51]. Moreover, the nonlinear dielectric
response may yield NEC at much higher carrier densities, where additional bands become occupied [52].

To distinguish between extrinsic and intrinsic origins for EPS, measurements of the capacitance between the 2DES and a metal electrode are a powerful tool. Intrinsic EPS caused by negative electronic compressibility yields a capacitance enhancement [46,51]; extrinsic EPS caused by spatial variations of the electrostatic potential yields a capacitance suppression once parts of the 2DES become insulating.

Here, we perform capacitance measurements on the LaAlO3/SrTiO3 2DES over a particularly wide range of gate voltages. To study a heterogeneous medium over a wide gate voltage range, we use a radially symmetric device geometry that prevents contact pinch-off. We find a strong suppression of the capacitance in a large part of the phase diagram, evidencing that EPS at the LaAlO3/SrTiO3 interface is dominated by extrinsic effects. Already at a high nominal carrier density of several $10^{13}$ cm$^{-2}$, local patches turn insulating.

The rate at which these local transitions occur is not constant, but it rises and falls repeatably upon varying the nominal carrier density. This behavior in combination with the magnitude of the EPS suggests that charged defects are the main driver of EPS. In the final section, we characterize the effect of EPS on the superconducting dome. These experiments provide direct evidence that the global $T_c$ is particularly reduced once local patches are insulating.

II. EXPERIMENT

A. Device design

The typical geometry for accurate resistance measurements of a 2DES is the Hall bar. The material of interest is structured to form a channel with a well-defined geometry, through which a current $I$ is sourced. The response of the material to this current is measured using voltage contacts placed on the sides of the channel, perpendicular to the current flow. Current flowing into these contacts distorts the measurement; accordingly, voltage contacts must be narrow [53]. For heterogeneous systems, this approach poses a problem. Voltage contacts with low local $n_{2D}$ are pinched off upon globally depleting the 2DES by electrostatic gating. Hence, no resistance measurements are possible at low nominal $n_{2D}$.

By using voltage contacts oriented parallel to the current flow, the measurement is not distorted by current flowing into (part of) the voltage contacts. Hence, contacts can be patterned with much longer lines of contact with the heterogeneous system. This reduces the probability of pinch-off. In the disk-shaped geometry shown in Fig. 1(a), the current flows radially out- or inward [14]. The lines connecting the 2DES with the electrodes measuring the in-plane voltage are long, maintaining electrical contact between them down to much lower nominal $n_{2D}$. In this radially symmetric geometry, the sheet resistance $R_{\text{sheet}}$ is given by

$$R_{\text{sheet}} = \frac{2\pi V}{\ln(r_{\text{out}}/r_{\text{in}})}$$

where $r_{\text{out}}$ and $r_{\text{in}}$ represent the radii of the outer and inner current contact, respectively.

The disk geometry has a second advantage over the Hall-bar geometry, which more specifically applies to SrTiO3-based electron systems. The huge relative permittivity of SrTiO3 [49,50] causes a significant lateral contribution of the electric field on narrow features. This focusing enables more efficient backgating [54], but also accelerates the local depletion process and yields a significant lateral capacitance [55]. This effect is minimized in the disk geometry, because the whole device is (intended to be) conducting. Figure 1(b)
shows a sketch of the field lines in our device, which are all strictly perpendicular to the interface in case of a fully conducting interface.

In heterogeneous systems, we expect locally depleted patches to form at low nominal $n_{2D}$. In that case, the field lines bend toward the edges of the still conducting patches. The resulting enhancement of the capacitance is significant if two conditions are both fulfilled: (i) the distance between the conducting regions is at least of the order of the typical size of the conducting patches $\lambda$; (ii) the thickness of the dielectric $d \geq \lambda$. Condition (i) is fulfilled close to global depletion or by patterning the conducting region into small areas [54]. To assess condition (ii), we consider that scanning-probe and transport experiments showed that $\lambda \geq 100 \text{ nm}$ [24,30].

B. Device fabrication

The device fabrication started with the standard chemical preparation [57] of SrTiO$_3$(001) substrates with dimensions $5 \times 5 \times 0.5 \text{ mm}^3$, supplied by CrysTec, GmbH. On such substrates, LaAlO$_3$ and Au films were deposited in situ using pulsed laser deposition (PLD). The substrates were heated to the deposition temperature of 800°C in an O$_2$ process pressure of $8 \times 10^{-4} \text{ mbar}$. In these conditions, 10, 7, or 4 u.c. of LaAlO$_3$ were deposited by ablating a single-crystalline LaAlO$_3$ target (CrysTec, GmbH). The laser fluence was 1.2 J/cm$^2$, the spot size was 2.8 mm$^2$, and the pulse frequency was 1 Hz. The film thickness was determined in operando by monitoring reflection high-energy electron diffraction (RHEED) oscillations. After growth of the LaAlO$_3$ layer, the samples were cooled to 600°C to cool down to 400 mbar. The samples were annealed for 1 h and cooled to room temperature at a rate of 2°C/s. Directly after cooldown, $\sim 30 \text{ nm}$ of Au was deposited. For the Au deposition, we used an Ar process pressure of 0.11 mbar and laser fluence of 2.7 J/cm$^2$.

After growth, the Au layer was structured into disk-shaped topgate electrodes by standard photolithography and subsequent wet etching in a buffered KI solution [14]. These electrodes had an area of either 1.66 or 0.68 mm$^2$. The contacts to the interface were defined by another photolithography step. After Ar ion milling through the LaAlO$_3$ layer and part of the SrTiO$_3$, contact to the interface was made by Ti/Au electrodes, which were deposited by magnetron sputtering. Figure 1(a) shows a completed device.

C. Transport experiment

For our capacitance measurements, we use the two-port method of Ref. [56]. It allows us to simultaneously measure the capacitance between the 2DES and the topgate electrode $C_g$ and the dc tunnel conductance $G_p$. Figure 1 illustrates the electrical connections and the equivalent circuit used in this method. The two-port method assumes all subcircuits are equal, which appears to conflict with measurements of a heterogeneous medium. As discussed in the supplemental material, we estimate that the deviations resulting from this conflict amount to less than 1% in our measurements [58].

All transport measurements were performed in a dilution refrigerator with a base temperature of 10 mK equipped with a Delft Electronics IVVI rack for signal (pre)amplification. The samples were glued on a metal plate of an in-house-designed sample holder by Ag glue. This conductive glue served as both the backgate electrode and as a heat sink. The topgate electrode was contacted by bonding Au wires with Ag glue by hand; the interface electrodes were contacted using a wedge bonder for Al wires.

The backgate voltage was applied using a Keithley 2400 Source Measure Unit; all other currents and voltages were sourced and measured using the IVVI rack. dc voltages were sourced by the rack itself, and ac signals were generated and measured using Stanford Research 830 lock-in amplifiers, connected to the optoelectronic inputs and outputs of the IVVI rack. We note that proamplifiers with sufficiently high input impedance ($\geq 1 \text{ G} \Omega$) must be used to measure the ac voltages across the gate dielectric in the two-port method. The input ac voltage $U_{in}$ was 5 mV.

Prior to measurement, we swept the gate voltages multiple times to their extreme values to avoid irreversible behavior as a function of applied gate voltage [59–61]. After this “training process,” we characterized devices in terms of leakage current and ac losses across the LaAlO$_3$ layer [56,62] as described in the supplemental material [58]. In all measurements presented below, the gate voltages were always swept in the same direction.

In the following, we focus on one device with a LaAlO$_3$ layer thickness $d_{\text{LAO}}$ of 7 unit cells (uc) and a device area $A$ of 1.66 mm$^2$. Other devices with $d_{\text{LAO}} = 10 \text{ uc}$ showed very similar behavior to that described below. Devices with $d_{\text{LAO}} = 4 \text{ uc}$ had a too large tunneling conductance to determine the capacitance reliably. Moreover, these devices did not become superconducting down to $T = 13 \text{ mK}$.

III. CAPACITANCE MEASUREMENTS

The capacitance of a capacitor is given by the geometric capacitance $C_g$ connected in series to a quantum capacitance $C_q$ [46,51,63]:

$$C^{-1} = C_g^{-1} + C_q^{-1}.$$  \hspace{1cm} (2)

$C_g$ can be described as a simple parallel-plate capacitor. However, a full description requires us to consider two parallel-plate elements connected in series: a contribution from the dielectric—here, LaAlO$_3$—and a contribution from the extension of the charge distribution into the doped material—here, SrTiO$_3$. As discussed in the supplemental material [58], the contribution from SrTiO$_3$ is negligible, and we may write

$$C_g = \frac{\epsilon_0 \epsilon_r A_{\text{eff}}}{d},$$  \hspace{1cm} (3)

where $\epsilon_0$ is the permittivity of vacuum, $\epsilon_r$ is the relative permittivity of the used dielectric, $d$ is the (effective) distance
between the electrodes, and $A_{\text{eff}}$ is the effective area of the device.

$C_q$ is defined as

$$C_q = e A_{\text{eff}} \frac{dn}{d\mu}.$$  

(4)

where $dn/d\mu$ is the electronic compressibility, representing the change in the density of mobile carriers $n$ upon shifting the chemical potential $\mu$.

Equations (3) and (4) contain two parameters that may reflect electronic phase separation and can be tuned by gate voltages. The first is $dn/d\mu$, which is determined by the electronic density of states (DOS) at the Fermi level, augmented by the effects of several interactions of the mobile electrons with their environment [46]. If the interactions are strong and the DOS is small, $dn/d\mu$ can become negative, thus leading to an enhanced total capacitance [45,51]. Because this behavior is intrinsic to the nature of a 2DES, we refer to an EPS caused by negative compressibility as intrinsic.

The second parameter in Eqs. (3) and (4) signaling EPS is the effective device area $A_{\text{eff}}$. It is smaller than the structurally defined device area $A$ if parts of the device are insulating. The application of a gate voltage can change $A_{\text{eff}}$ in two ways: (i) Depending on the device geometry, channel edges may turn insulating before the “bulk” of the channel does [54,64]; (ii) in the case of EPS by extrinsic causes, the carrier density is heterogeneous and certain patches turn insulating earlier than others. Our device was designed specifically to avoid edge depletion: because the interface is not patterned into channels, the electric field is everywhere oriented perpendicular to the interface and thus homogeneous in the plane of the device. Hence, a reduction of $A_{\text{eff}}$ would imply extrinsic EPS.

Figure 2(a) shows the measured capacitance between the 2DES and the topgate electrode $C_p$ as a function of both $V_B$ and $V_T$. We present and discuss the simultaneously measured data for $C_p$ and $R_{\text{sheet}}$ in the supplemental material [58].

In the top-right corner of Fig. 2(a), $C_p$ is constant at 92.9 nF. We interpret this value as the geometric capacitance across the LaAlO$_3$ dielectric with fully metallic electrodes—i.e., $C_p$ in Eq. (3). Using this equation with $d_{\text{LAO}} = 2.7$ nm and $A_{\text{eff}} = A = 1.66 \text{ mm}^2$, we find $\epsilon_r_{\text{LAO}} = 17$. This value agrees well with measurements on thin LaAlO$_3$ films between bulk-metallic electrodes [65], and it is slightly lower than that of LaAlO$_3$ single crystals [66]. Other reports on metal/LaAlO$_3$/SrTiO$_3$ structures generally report lower values [51,67,68], except for one study on devices with thicker LaAlO$_3$ films, which reported $\epsilon_r = 21$ [69]. Together with the minute gate leakage current density [58], the high $\epsilon_r_{\text{LAO}}$ confirms the high quality of the LaAlO$_3$ dielectric in our devices.

Away from this plateau, the gate voltages reduce $C_p$ continuously. The lowest value for $C_p$, measured in the bottom-left corner of Fig. 2(a), is less than half of the value measured on the plateau. Unlike Li et al. [51], we do not observe any capacitance enhancement within the wide parameter space of our experiment. We argue that this absence is due to the carrier density in our devices being too high. Unfortunately, the device geometry does not possess transverse voltage contacts, and $n_{2D}$ cannot be determined directly via the Hall effect. Hence, we take $R_{\text{sheet}}$ as a benchmark to compare our results to those of Li et al. They observed that the capacitance enhancement occurred for $R_{\text{sheet}} \gtrsim 10^5 \Omega$. The maximum $R_{\text{sheet}}$ in our experiment is about an order of magnitude smaller [58]. This comparison suggests that the minimum $n_{2D}$ is up to an order of magnitude higher in our experiment—too high for a capacitance enhancement to occur.

A. Origin of the capacitance reduction

Following Eq. (2), the observed capacitance reduction is either of geometric or quantum origin [46,63]. We assess the scenario in which $C_p$ is constant—and all change in $C_p$ is thus due to $dn/d\mu$ and therefore of quantum origin—in the supplemental material [58]. This analysis yields an unrealistically large shift in the chemical potential $\mu$ of almost 1 eV across the gate-voltage parameter space. This hypothetical shift is...
The labels printed above the respective curves. For clarity, the curves at different values during the measurements, which are indicated by respective values at the tunnel conductance. The effects are the exclusive origin of the observed reduction of not observed. We can thus rule out that quantum-mechanical and calculated. Moreover, such a large shift in two orders of magnitude larger than experimentally measured [70] and calculated [52]. Alternatively, such a large shift in would also affect the tunnel conductance $C_p$ [70], which is not observed. We can thus rule out that quantum-mechanical effects are the exclusive origin of the observed reduction of the capacitance.

We conclude that the gate voltages must affect $C_p$ in our experiment. Indeed, all three parameters entering Eq. (3) may be affected. We outlined the effect of changing $A_{\text{eff}}$ above. The polarizability of the LaAlO$_3$ crystal may depend on the electric field across it, changing $\epsilon_r$. However, the effect of a backgate voltage is expected to be negligible, which is not reflected in the measurements. The effective thickness of the capacitor $d$ may change by shifting the out-of-plane distribution of mobile charges.

To distinguish between tuning $d$ and tuning $A_{\text{eff}}$, we compare the tuning of $C_p$ to that of the tunnel conductance $G_p$. Both are linear functions of $A_{\text{eff}}$. However, they depend differently on $d$: while $C_p$ is proportional to $d^{-1}$, $G_p$ is (roughly) proportional to $e^{-d}$ [71]. Figure 3 shows the relative change in both $C_p$ and $G_p$ as a function of $V_B$ for several fixed values of $V_T$. To eliminate the high sensitivity of the tunneling process to $V_T$, each curve is normalized to its value at $V_B = +180$ V.

We observe that $C_p$ and $G_p$ show almost the same relative change with varying $V_B$ for all values of $V_T$. This observation implies that $A_{\text{eff}}$ is the main factor underlying the capacitance reduction. Edge depletion is prevented by the device geometry, so this reduction of $A_{\text{eff}}$ implies electronic phase separation. We note that this reduction readily occurs at $V_B = V_T = 0$ V.

The total area covered by the insulating patches increases continuously towards the bottom-left corner of Fig. 2(a). The contours of equal $C_p$ correspond well with the contours of equal nominal $n_{2D}$ [58]. $A_{\text{eff}}$ is thus correlated with the nominal $n_{2D}$ in the region where $A_{\text{eff}} < A$. In the bottom-left corner, $A_{\text{eff}} \approx A/2$. Concomitantly, $R_{\text{sheet}} \approx h/e^2$ [58], revealing the vicinity of a metal-to-insulator transition (MIT). The global MIT thus appears to coincide with the point where about half of the patches are insulating. This coincidence corresponds with the 2D threshold for site percolation, which equals $1/2$ [72]. Recent scanning-probe measurements confirm that the MIT at the LaAlO$_3$/SrTiO$_3$ interface can be described by (modified) percolation theory [29]. A percolative MIT implies that the lateral size of the patches is orders of magnitude smaller than the size of the whole device.

B. Characterizing the phase separation

Figure 2(b) shows the derivative of $C_p$ to $V_B$ as a function of $V_B$ and $V_T$. In this map of $dC_p/dV_B$, three regions of different color can be distinguished, as marked by the roman numerals. In region III, $C_p$ is completely independent of $V_B$, representing the parallel-plate capacitor model with fully metallic electrodes. In region II, $C_p$ is weakly affected by $V_B$—we discuss this region in the next subsection.

In region I, both $C_p$ and $G_p$ are strongly affected by $V_B$. This region is filled with series of peaks and dips in $dC_p/dV_B$, which are tuned continuously by the gate voltages. We observe at least eight such features in Fig. 2(b) and in the corresponding diagrams for $dC_p/dV_T$ and $dG_p/dV_B$ discussed in the supplemental material [58]. Their positions follow the contours of equal $C_p$ in Fig. 2(a) and roughly the contours of equal nominal $n_{2D}$ [58]. Their heights are tuned smoothly and none of the observed features (dis)appears abruptly anywhere in the diagram. These observations allow us to make the following statements on the nature of the EPS: (i) The rate of change of $A_{\text{eff}}$ is not constant. The distribution of $n_{2D}$ around the nominal $n_{2D}$ is thus not normal, but characterized by a discrete number of preferred values for $n_{2D}$; (ii) the order in which patches undergo the MIT is always the same. Hence, the phenomenon underlying the phase separation is not significantly affected by the voltages, but rather a fixed property of the device. We note that for different devices, the pattern of peaks and dips in $dC_p/dV_B$ is also different.

A lateral variation of $n_{2D}$ implies a spatial variation of the electrostatic potential. Based on the statements above, we argue that this lateral variation is structural in origin. Tuning the Fermi level by the gate voltages drives patches insulating when the Fermi level falls below the (local) potential.

We estimate the magnitude of the in-plane potential variation by considering the change of the nominal $n_{2D}$ in region I, where $A_{\text{eff}} < A$. Within this region, the gate voltages tune the nominal $n_{2D}$ by about $4 \times 10^{11}$ cm$^{-2}$ [58]. Thus, even when changing the nominal $n_{2D}$ by this large value, parts of the interface remain insulating. The carrier
density in the patches with the lowest density (highest potential) must therefore be about $4 \times 10^{13} \text{ cm}^{-2}$ smaller than the nominal $n_{2D}$. To accommodate such a large variation in $n_{2D}$, the variation of the surface potential has to be of a certain magnitude. Schrödinger-Poisson calculations [52] suggest that changing $n_{2D}$ by $4 \times 10^{13} \text{ cm}^{-2}$ requires a potential difference of tens of meV.

C. Quantum capacitance

The final region of the capacitance-voltage phase diagram is labeled as II in Fig. 2(b). Here, $dC_p/dV_B$ has a positive value that is about an order of magnitude smaller than in region I. There is no local structure of peaks and dips: $C_p$ is thus tuned monotonically in this region. Simultaneously, $G_p$ is tuned nonmonotonically, as observed in Fig. 3. These observations suggest that in region II, the change of $C_p$ is not driven by a change in $A_{\text{eff}}$. Rather, we hypothesize that the interface is fully conducting and that quantum-capacitive effects drive the change of $C_p$ in region II.

As Eqs. (3) and (4) describe, a positive and significantly small $C_q$ reduces the measured $C_p$. This applies typically to capacitors with low-dimensional conductors, which have a low DOS and therefore a low $dn/d\mu$ [46]. The LaAlO$_3$/SrTiO$_3$ interface is a low-dimensional conductor, so we expect our device to have a non-negligible $C_q$. In region I, however, the effect of the reduced $A_{\text{eff}}$ obscures this contribution. In region III, $C_q$ is either very constant at some certain value, or $dn/d\mu$ is so large that $C_q^{-1}$ becomes negligible.

Before we address the transition between regions II and III, we test our hypothesis by estimating the shift in the chemical potential $\mu$ within region II. We describe this analysis in the supplemental material [58], which yields a shift in $\mu$ of about 1 meV within this narrow range. This value agrees well with tunnel-spectroscopic measurements [70] and with Schrödinger-Poisson modeling [52].

Those measurements as well as that modeling revealed a peculiar feature of $\mu$ as a function of $V_B$. It increases monotonically for low $V_B$, but remains (almost) constant for high $V_B$. Such behavior explains our observation that $C_q$ is constant in region III, because a constant $\mu$ implies an infinite $dn/d\mu$ and therefore a negligible $C_q^{-1}$. This behavior was ascribed [52,70] to previous observations that the total DOS—and therefore $dn/d\mu$—increases dramatically once additional electronic bands become occupied as a result of increasing $n_{2D}$ [20]. This process is an example of a Lifshitz transition—we will use this term to refer to it below. The additional occupied bands lie a few tens of meV higher in energy, which is the result of both inversion-symmetry breaking [73] and the interplay of out-of-plane electrostatic confinement with orbital orientation [74]. The Lifshitz transition takes place at a nominal $n_{2D}$ of about $2 \times 10^{13} \text{ cm}^{-2}$ [20,21].

The phase separation identified in the previous sections also affects the Lifshitz transition. It is not a collective phenomenon happening simultaneously across the entire sample, but rather it occurs in a patchy manner like the MIT. Traversing region II from the border with region I to that with region III, the total area covered by patches in which the high-DOS bands are occupied increases gradually. Hence, the average $dn/d\mu$ increases gradually as well; accordingly, $C_q$ of the total device decreases gradually in region II, as observed in Fig. 2(b).

IV. SUPERCONDUCTING DOME

We now turn to the effect of the phase separation on superconductivity. In the following, we study this effect by measuring the superconducting transition as a function of temperature while varying the gate voltages, as shown in Fig. 4. These measurements yield two-dimensional maps of the onset temperature $T_c$ and the zero-resistance temperature $T_{c,0}$ as a function of $V_B$ and $V_T$ (Fig. 5). Comparing these maps to those in Fig. 2 allows us to directly study correlations between the EPS and the superconducting phase.

A. Single-gate tuning

Figures 4(a) and 4(b) show the sheet resistance $R_{\text{sheet}}$ measured as a function of temperature $T$ for varying $V_B$ and $V_T$. We refrain from extracting a resistivity $\rho_{xx}$ from our measurements, because this would imply that a single $q_{\rho_{xx}}$ value applies homogeneously to the entire device.

From these $R(T)$ measurements, we extract the temperatures marking the boundaries of the transition: the onset
FIG. 5. Tuning the superconducting critical temperatures by a combined application of backgate voltage \( V_B \) and topgate voltage \( V_T \).

(a) Tuning of the zero-resistance temperature \( T_{c,0} \). The main panel on the bottom left shows \( T_{c,0} \) on a color scale—given on the top right—as a function of both gate voltages. In the white-shaded area, the resistance was nonzero always for \( T \geq 20 \) mK. The top panel shows \( T_{c,0} \) as a function of \( V_B \) for various fixed values of \( V_T \). These curves represent horizontal line cuts across the main panel between between the orange (\( V_T = 0.1 \) V), blue (\( V_T = 0.3 \) V), and dark red (\( V_T = 0.5 \) V) triangles. The panel on the right-hand side shows \( T_{c,0} \) as a function of \( V_T \) for various fixed values of \( V_B \). These curves represent vertical line cuts across the main panel, between the olive (\( V_B = -100 \) V), violet (\( V_B = 0 \) V), and gray (\( V_B = +100 \) V) triangles. The red shading represents the magnitude of the dc gate leakage current. Lines connecting data points are guides to the eye. (b) Same as (a), mapping the onset temperature \( T_{c,\text{onset}} \) as a function of both gate voltages. In the white areas of the main panel, no superconducting onset could be detected in the measurements.

temperature \( T_{c,\text{onset}} \) and the zero-resistance temperature \( T_{c,0} \). We define \( T_{c,0} \) as the maximum temperature at which \( R_{\text{sheet}} = 0 \), or \( R_{\text{sheet}} < 10^{-1} \) \( \Omega \) in practice. \( T_{c,\text{onset}} \) marks the deviation from metallic \( R(T) \) behavior. We define it as the maximum temperature at which \( R(T) \) satisfies three conditions: \( R(T) \geq 0 \), \( dR/dT > 0 \), and \( d^2R/dT^2 \geq 0 \). Roughly speaking, it represents the temperature at which the \( R(T) \) curve starts “bending downwards” during cooling. Between \( T_{c,\text{onset}} \) and \( T_{c,0} \), the transition is complex with multiple steps. The steps suggest that \( T_c \) is also distributed as a discrete set of preferred values. Finally, we note that we do not observe a \( T \)-independent \( R_{\text{sheet}} \) below the superconducting transition in any of our devices. Such behavior would indicate an “anomalous-metal” state [75,76], an intriguing possible result of EPS.

Figures 4(c) and 4(d) show \( T_{c,\text{onset}} \) and \( T_{c,0} \) as a function of either \( V_B \) or \( V_T \). The effect of an applied topgate voltage appears to be relatively straightforward: Increasing \( V_T \) raises \( T_{c,\text{onset}} \) and \( T_{c,0} \) simultaneously at the same rate, except at high and at negative \( V_T \). There, both critical temperatures are suppressed by emerging gate leakage currents [13,75], blocking the observation of a superconducting dome with a clear maximum of \( T_{c,0} \) [15,77].

The effect of an applied backgate voltage is more complex. \( T_{c,0} \) follows a dome-shaped trajectory as a function of \( V_B \), as regularly observed previously [12,14,40,75,78]. The top of this dome lies somewhere between 20 and 40 V. In contrast, \( T_{c,\text{onset}} \) remains constant for negative \( V_B \) and decreases monotonically with positive \( V_B \). Very similar behavior was observed for the superconducting gap \( \Delta \) and critical field \( H_c \) measured as a function of \( V_B \) by tunnel spectroscopy [14,70,79,80].

In those experiments, \( T_{c,0} \) also fell with more negative \( V_B \), where \( \Delta \) and \( H_c \) kept increasing or remained constant. The correspondence between tuning \( \Delta \) and tuning \( T_{c,\text{onset}} \) suggests that these parameters are correlated.

We note that in the raw data underlying Fig. 4(a), \( R_{\text{sheet}} \) was negative at low \( T \) for \( V_B \leq -120 \) V. This negative resistance implies that one of the voltage contacts is pinched off from the region of interest, despite our effort to prevent this problem in the device design. In analyzing these data, we found that the apparent negative resistance in case the sample was superconducting—evidenced by \( V(I) \) measurements—was always \(-775 \) \( \Omega \). This value represents the combination of various electronic elements in the setup and/or in the device, which we could not resolve confidently. However, the singularity of this value allows us to correct the data by a fixed offset of \( 775 \) mK. This correction is justified by the smooth evolution of the curves in Fig. 4(a) with \( V_B \), with the slight exception of the high-temperature data for \( V_B = -120 \) V.

B. Dual-gate tuning

Figure 5 shows maps of \( T_{c,0} \) and \( T_{c,\text{onset}} \) as a function of both \( V_B \) and \( V_T \). For \( T_{c,0} \), we observe a superconducting dome around a maximum value of \( \sim 160 \) mK at \( V_B = 0 \) V and \( V_T \approx 0.3 \) V. Away from the optimum, global superconductivity is suppressed gradually in all directions. This gradual decrease is cut off abruptly by emergent topgate leakage currents on the bottom and top edges of the diagram. The gradual decrease
of $T_{c,0}$ away from the optimum is faster for positive $V_B$ than for negative $V_B$. For negative $V_B$, the topgate voltage at which $T_{c,0}$ is maximized is constant at about 0.3 V. This optimum shifts towards lower $V_T$ once $V_B$ turns positive. Accordingly, $T_{c,0}$ reduces to 0 for high $V_T$ and $V_B$.

From the same $R(T)$ measurements, we extracted $T_{c,\text{onset}}$ as a function of both gate voltages. Figure 5(b) shows the resulting map, which differs from the map of $T_{c,0}$. We focus on the left-hand side of the diagram, where $V_B < 0$. There, $T_{c,\text{onset}}$ remains constant as a function of $V_B$, like in Fig. 4(c). It appears to saturate at about 370 mK in the top left, before falling again at higher values of $V_T$ due to gate leakage currents. Hence, we conclude that $T_{c,\text{onset}}$ monotonically increases with $V_T$ in this regime, while remaining unaffected by $V_B$.

In region 1 of the capacitance-voltage phase diagram, $T_{c,\text{onset}}$ is tuned differently than $T_{c,0}$. This discrepancy is best observed by comparing curves in the top panels and the olive curves in the right-hand panels of Figs. 5(a) and 5(b). It implies that $\Delta$ and $T_{c,0}$ are tuned differently, which we ascribe to a heterogeneous superconducting state. If $\Delta$ varies in the plane of the superconductor, phase coherence across the sample is gradually lost and $T_{c,0}$ reduced [81]. Measurements of the kinetic inductance in this regime support this scenario [40].

V. DISCUSSION

The main result of our work is the experimental quantification of the carrier-density variation associated with the EPS occurring at the LaAlO$_3$/SrTiO$_3$ interface. We estimate this variation to be about $4 \times 10^{13}$ cm$^{-2}$. We argue that spatial variations of the electrostatic potential on the order of tens of meV are the main driving force for the huge EPS found. As a result, $T_c$ is heterogeneous on the order of the nominal $T_c$.

These magnitudes exceed the anticipated magnitude of variation caused by tetragonal domains in SrTiO$_3$ or by the boundaries between these domains [30,32]. Although these variations are expected to exist, domains and their walls cannot account for the full lateral variation observed here. The absence of capacitance enhancement anywhere in Fig. 2 shows that NEC also has at most a limited influence.

Hence, we consider charged defects as the most likely candidate driving the observed behavior. In SrTiO$_3$, local fixed charges are screened very ineffectively: because of the extremely high low-temperature permittivity [49,50], the Thomas-Fermi screening length is large [54]. Indeed, scanning-probe measurements suggest that the lateral extension of patches is at least of the order of 0.1–10 $\mu$m [25,30,32]. The patterns of peaks and dips observed in Fig. 2(b) imply a discrete energy spectrum associated with these defects. Given the total span of the potential distribution of a few tens of meV, the spacing in energy within this spectrum is of the order of 1 meV.

Charged defects located on the metal-oxide planes give rise to such a discrete spectrum [44]. Because these defects are confined to the lattice planes, their out-of-plane distribution is discrete. The original work [44] considered defects in the LaAlO$_3$ and suggested energy differences of several tens of meV with lateral extensions of a few nm. Applying the same framework to defects in SrTiO$_3$ at cryogenic temperatures requires using $\epsilon_r \sim 10^4$; doing so yields sub-meV level spacing and lateral extensions of the order of 1 $\mu$m. The spectrum is complicated further by the fact that the charge of each defect is not necessarily equal. Charged defects in SrTiO$_3$ may consist of negatively charged Sr (or Ti) vacancies, or of positively charged O vacancies [42]. Moreover, these defects can cluster in various configurations [82], yielding subtle differences in their resulting dipole moments. Our observation that the capacitance spectrum varies among devices supports the notion that the EPS is caused by charged defects, because the defect structure is different in each device.

Charged defects can migrate efficiently along domain walls in complex oxides, even at low temperatures [83]. This migration is an important aspect of the irreversible response to the initial application of a backgate voltage [60,61]. Hence, the gate-training process performed before measurement may affect or even create the lateral variations in the potential causing the EPS. Therefore, we measured $C_p$, $G_p$, and $R_{\text{sheet}}$ during the training process. The results, shown in the supplemental material [58], reveal that the electrostatic potential landscape indeed changes slightly during training. They also show that the lateral variations are present before training and that the irreversible response is mainly due to trapping of mobile charges, in line with previous observations [59–61].

Our results support the understanding that controlling the formation of (charged) defects is at the heart of oxide electronics. Due to the large number of elements involved and the volatility of oxygen, the electrochemical balance of oxide films is complex [42]. Appropriate deposition and postdeposition processing conditions are required to effectively mitigate EPS. For example, capping the LaAlO$_3$ by an infinite-layer cuprate enhances the oxygen uptake through the catalytic activity of the cap [84]. This capping boosts the carrier mobility by about an order of magnitude [84] and smooths the surface potential as a function of lateral position [85]. Alternatively, imposing many defects induces a transition to bulk conductivity, raising mobility [2] and suppressing the lateral variation in $T_c$ [32]. However, samples with a significant bulk conductivity are of limited use for field-effect studies. A different type of postdeposition processing is charge writing by conductive-tip atomic-force microscopy [86]. This writing exerts locally huge electrostatic forces that mitigate defects and even align the SrTiO$_3$ domains [87]. To date, such devices are the only examples of 2DESs in complex oxides with mean free paths of tens of micrometers [88].

VI. CONCLUSION

We have investigated the electronic phase separation at the archetypal LaAlO$_3$/SrTiO$_3$ interface by measuring the capacitance between the interface and a topgate electrode as a function of applied topgate and backgate voltage. These measurements revealed three different regions of tuning, separated by boundaries that correspond roughly to contours of constant nominal carrier density. At the highest nominal carrier density, we found that the capacitance is completely independent of gate voltage. Here, the LaAlO$_3$/SrTiO$_3$ interface behaves like a three-dimensional electron system with a very high density of states. Lowering the nominal carrier density below a threshold value resulted in a slight
capacitance reduction, which we attributed to a positive electronic compressibility.

At the lowest nominal carrier density, we found that the capacitance and also the tunnel conductance are reduced strongly by the gate voltages. We attributed this behavior to a reduction of the effective device area through a strong variation of the carrier density in the plane normally, but according to a discrete set of preferred values. We attributed this behavior to the presence of (clusters of) charged defects located at different discrete distances from the interface.

As a result of the phase separation, the electronic properties of the LaAlO3/SrTiO3 interface have to be considered as strongly heterogeneous. We studied the superconducting dome as an example—our device geometry allowed us to measure the full superconducting dome as a function of both gate voltages for the first time in the same device. These measurements revealed a large discrepancy between the onset temperature and the zero-resistance temperature, especially in the region in which insulating patches emerge. The stepwise $R(T)$ curves imply that $T_c$ is also distributed as a discrete set of preferred values.

Our results highlight the need to mitigate electronic phase separation as a result of in-plane potential variations in oxide 2DESs. All successful strategies reported tune the density of charged defects. Doing so will enable fundamental studies to reliably establish correlations between different physical properties and to reach appropriate conclusions about their possible connections. Moreover, controlling phase separation is essential for the exploitation of oxide 2DESs in future electronic devices. It need not necessarily be mitigated: controlled modulation may yield new physical systems in which an order parameter is laterally modulated in a controlled manner.

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