Wafer-scale nanostructure formation inside vertical nano-pores

J.W. Berenschot, X. Sun, H. Le The, R.M. Tiggelaar, M.J. de Boer, J.C.T. Eijkel, J.G.E Gardeniers, N.R. Tas

MESA+ Institute for Nanotechnology
University of Twente
Enschede, The Netherlands
email: j.w.berenschot@utwente.nl

E. Sarajlic

SmartTip B.V.
Enschede, The Netherlands

***Abstract*— We propose a wafer-scale technique for nanostructure formation *inside* vertically oriented, through-membrane nano-pores. It uses 50 nm monocrystalline silicon pillars as a mold, embedded in a silicon nitride membrane formed in an innovative step. The proposed technique paves the way towards advanced functionalization of parallel oriented nano-pores for actuation, sensing, filtering/trapping purposes.**

***Keywords*— Nano-pores; membrane; corner lithography; anisotropic etching; conformal deposition**

I. INTRODUCTION

The realization of large-area membranes containing pores of different composition and functionality, is based on a number of key top-down micro- & nanofabrication techniques which have a long history. The first key technology is the transfer of a lithographic pattern – composed of lines or dots – into bulk silicon by means of directional plasma or electrochemical etching, resulting in respectively silicon ridges [1-4] or pillars [5-9]. The second technique comprises complete and conformal refilling of the spacing between adjacent ridges or pillars with thin film dielectric material (SiRN or SiO_2) [1-4, 7-9] or isotopic ^{10}boron (^{10}B) [5,6]. The depth of the etched pattern defines the thickness of dielectric plugs that can be, for example, used as robust elements for RF-MEMS [2,4]. The spacing between the etched silicon structures defines the thickness of the conformal coating that needs to be deposited to completely fill the gaps between neighboring structures. Whereas spacings based on standard UV-lithography are typically at least 1 micron wide (implying that relatively thick dielectric films are required for filling of the spacing), use of nanolithographic techniques such as Displacement Talbot Lithography [10,11] allows the use of conformal layer thicknesses of only a few hundred nanometers for complete refilling of vertical gaps. The last 15 years, these key techniques in combination with optional removal of the underlying bulk silicon have been used for the realization of various applications. In case of non-removal of bulk-Si fabricated structures can be integrated in RF devices [2, 4], in thermal neutron detectors [5, 6], or used for the fabrication of arrays of silicon field nano-emitters [8]. Removal of the silicon underneath the conformally coated and refilled structure yields suspended layers, which can be applied as thermal barrier [3] or as extraordinary optical transmission (EOT) membrane [9]. In more detail, for the fabrication of their EOT membranes Walavalkar et al. [9] realized silicon nanopillars using dedicated ICP-RIE. These nanopillars were fully converted into SiO_2 prior to their embedment in metal and into a suspended membrane. Upon modification of the applied (deep) reactive ion etch settings, the silicon nanopillars can have vertical or sculptured sidewalls [12-14], where the latter allows for the formation of quantum dots [13]. While in previous work Si pillars were converted into glass, in our contribution non-sculptured silicon nanopillars in combination conformal deposition steps, corner lithography [15-16] and sacrificial etch steps are applied to realize SiRN-based membranes containing massive arrays of parallel, hollow nanopores with embedded nano-cages.

II. EXPERIMENTAL

The manufacturing method that we have followed is outlined in fig. 1 (membrane formation) and fig. 2 (nanostructure formation). Arrays of silicon nano-pillars are formed in a <100>-silicon wafer by Displacement Talbot Lithography (DTL) [10, 11] combined with ICP-RIE. A high density dual source ICP/CCP plasma apparatus (PlasmaPro Estrelas 100, Oxford Instruments) was used to etch the pillar array based on a SF_6 - C_4F_8 chemistry [14]. In this process the sidewalls are continuously passivated by C_4F_8 polymer creating pillars with smooth sidewalls. The shaping is primarily achieved by tuning etch-passivation gas ratio and verticality by adjusting the bias power to control the polymer removal rate at the etch front. Parameters of the process are: ICP 800 watt, CCP 38 Watt, a pressure of 22 mTorr, 50 sccm C_4F_8 flow, 25 sccm SF_6 flow, and an electrode temperature of °0 C. The pillars have a positive slope of 88.8°, a diameter of 100 nm and height of 440 nm. The process has an etch rate of 125 nm/min, a selectivity of 5.5 and wafer scale uniformity of ~0.2% for a 100mm wafer. This process is followed by a dry oxidation step at 950 ºC to form a 50 nm thick SiO_2 layer. After stripping this oxide in BHF, the diameter of the pillars reduced from around 100 nm to around 50 nm, fig 1a. The membrane structural material is LPCVD silicon nitride (SiN) which is coated conformally across the substrate at a thickness of at least d_1 (half the perpendicular pitch between the pillars), filling up the space between the pillars (distances w_1 and w_2),

and thus creating a SiN membrane thicker than the flat deposited layer thickness. In the current experiment a layer thickness of 200nm was deposited, fig 1b. The SiN was patterned on the backside using RIE, followed by anisotropic etching of silicon to form about 25 µm thick silicon membranes with surface areas of about 0.1 mm^2 each (25% TMAH at 85 ºC , etchrate of Si(100) is 0.66 µm/min). In-pore nano-cages are formed in the following steps. First, the silicon nitride membrane is locally thinned using a poly-silicon mask and isotropic etching in 85% H_3PO_4 at 180 ºC (etchrate of SiN is 3.5nm/min) to expose the silicon pillars, fig 1c. Next, the top of the pillars is anisotropically etched (25% TMAH solution, 70ºC, 2 min) to create the mold for corner lithography [15, 16], fig 2a. As the angle of the ribs of the pyramidal mold is about 110º, the subsequent corner lithography process would be rather critical, leaving only a few nanometer material (t_1 in fig. 3) in the ribs. We have therefore applied oxidation sharpening of the mold (13 nm wet thermal silicon oxide grown at 800 ºC) to locally increase the sharpness of the corner. The resulting silicon nitride nanowires will have an increased thickness t_2 (fig. 3), which is estimated to be around 10 nm for a deposited silicon nitride layer thickness of 16 nm and an isotropic over-etch factor of 1.05. After oxidation sharpening, the mold is coated by a 17 nm stoichiometric silicon nitride layer (Si_3N_4) deposited by LPCVD, fig 2b. This layer is isotropically thinned in in 85% H_3PO_4 , at 140 ºC to create the nano-cages. The etchrate of Si_3N_4 is 3.5 nm/min and was determined by etching a dummy wafer and measure the thickness by ellipsometry. The etching time was approx. a factor 1.05 of the time needed to remove the flat 17 nm layer, fig. 2c. In-pore nanostructures are released from the backside by removing the remaining silicon membrane and the sacrificial pillars in 25%TMAH at 70 ºC solution, fig 2d. The etchrate of Si(100) is 0.33 µm/min. Dicing was used to create STEM compatible substrates. Dicing foil (Nitto SWT 10) was applied on both sides of the wafer. Aligning and dicing is done at the backside. The size of each sample is 2.0 mm x 2.6 mm. After removing the dicing foil, samples are cleaned in 100% HNO3 followed by a timed 1% HF etching to remove the 13 nm sharpening layer from the backside of the nanowire features. The etchrate of SiO_2 is 4.5 nm /min and is predetermined using a dummy wafer.

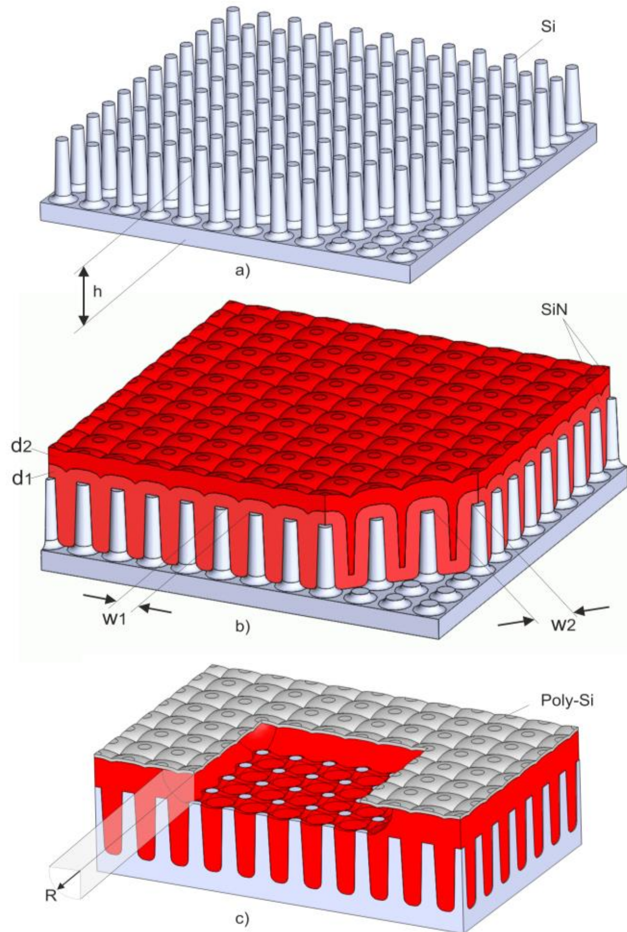

Fig. 1. First steps in "smart"-pore membrane fabrication: a) Sacrificial pillar formation, b) Conformal deposition of silicon nitride, c) Deposition, patterning of polysilicon mask followed local thinning of the silicon nitride to expose the sacrificial pillars.

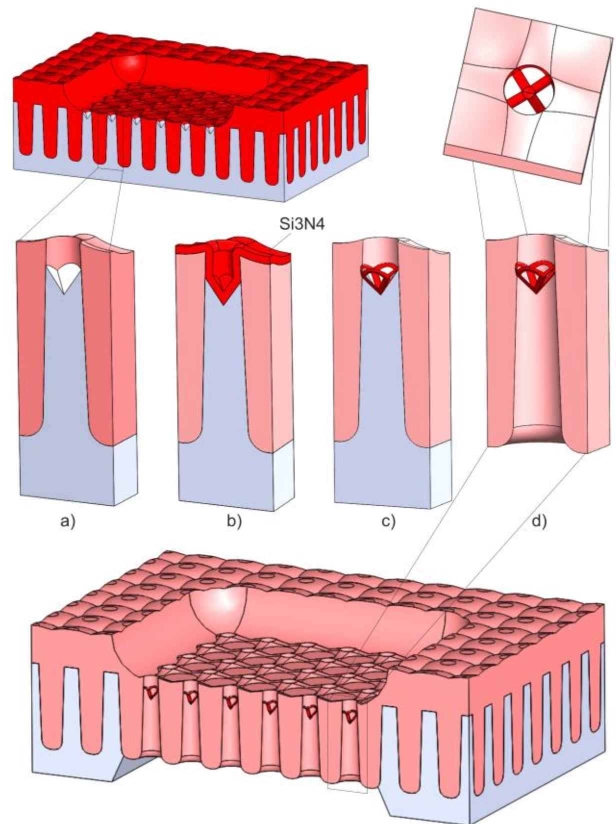

Fig. 2. In-pore feature formation by corner lithography: a) Anisotropic etching of the silicon to form pyramidal nano-pits, b) Oxidation sharpening of concave corners, followed by conformal deposition of a thin (17 nm) silicon nitride layer, c) Isotropic thinning of the silicon nitride and d) TMAH etching to remove the sacrificial silicon pillars, yielding nano-cages.

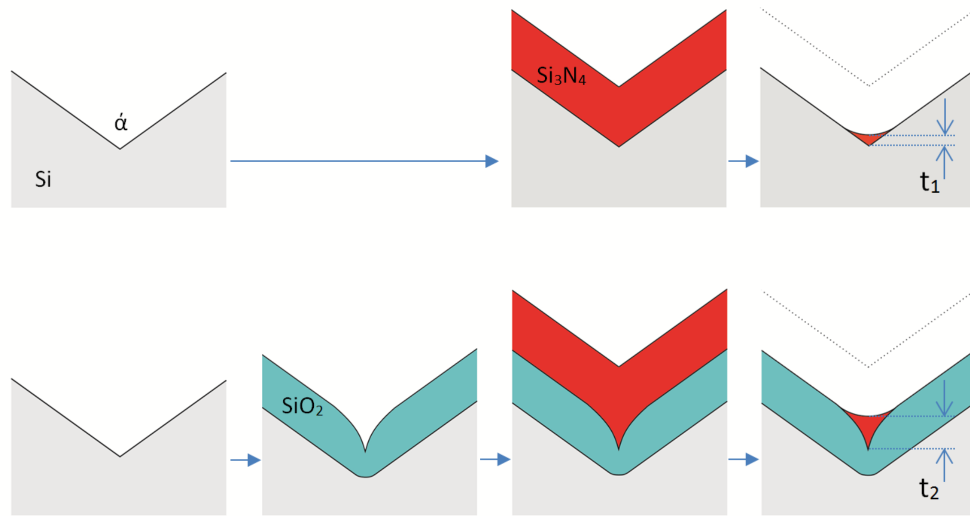

Fig. 3. Illustration of the nanowire formation by corner lithography in the ribs of the pyramidal mold (angle α = 110º), with (bottom) and without (top) oxidation sharpening of the corner. When using oxidation sharpening the remaining silicon nitride thickness $t_2 > t_1$.

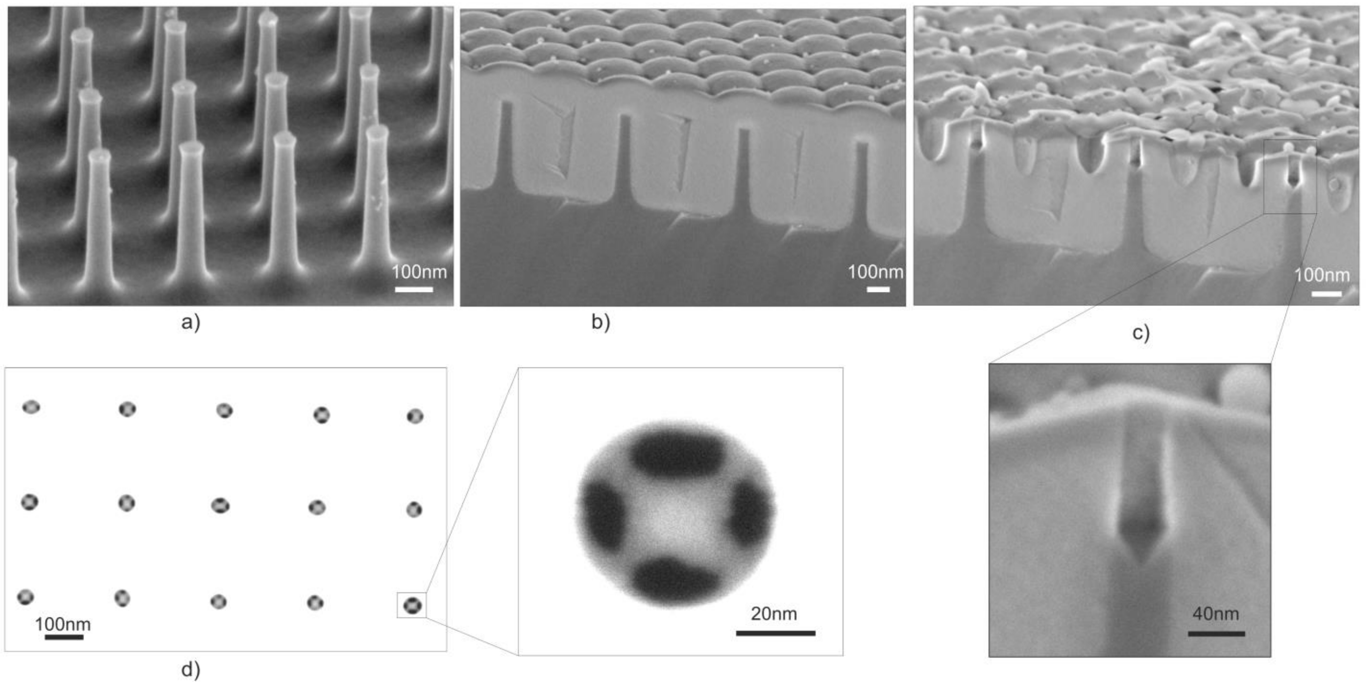

Fig. 4. Fabrication results. a) Silicon pillar array after RIE and oxidation thinning; b) Pillars embedded in silicon nitride; c) After accessing and shaping the pillars; d) Top-view (STEM) after nano-cage formation and silicon removal.

III. RESULTS AND DISCUSSION

Fig. 4 illustrates some key fabrication results. An array of 400 nm tall, slightly tapered silicon pillars after RIE and oxidation thinning is shown in fig. 4a. After embedding them in silicon nitride, the cross section of fig. 4b results. Note that the deposited silicon nitride thickness was between d_1 and d_2, resulting in shallow cavities diagonally between the pillars. Fig. 4c shows the cross section after shaping the silicon mold material. Tiny pyramidal pits are formed in the top of the pillars. After corner lithography and removal of the silicon pillar material, through-membrane pores have been formed containing nano-cages (best visible in the STEM top-view, fig. 4d). Note that the pore diameter is around 40 nm, and the nanowires forming the cages are around 10 nm in diameter. A crucial step, which we have investigated separately and more in detail, is the sacrificial etching of the silicon. Note that after a pyramidal pit is formed, the etching slows down because the receding pit is bound by slow etching {111}-crystal planes. Fig. 5 shows a cross section in which the 400 nm tall pores have just been opened. As can be deduced from the etch depth (400 nm) vs. etch time (510 s), the average axial etch rate is about 0.8 nm /s. This is slightly higher than the known etch rate of silicon (<111>-direction) in the solution used (0.42 nm / s), multiplied by the geometry factor 1 / sin (35.3º) related to the orientation of the pore with respect to the silicon crystal.

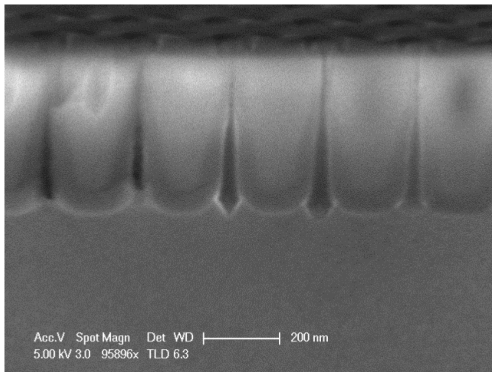

Fig. 5. Cross-section of about 400 nm tall pores, which were fully etched in 510 s in 25 wt% TMAH solution at 70 °C. This is indicative for an average axial etch rate of 0.8 nm / s.

IV. CONCLUSIONS

We have successfully fabricated a robust and free-standing silicon nitride membrane by filling the space between vertically oriented silicon nano-pillars of around 400 nm in height. These pillars were subsequently used as a mold and sacrificial material to make through-pores in the membrane containing nanowire pyramid structures. In future, this device will be tested for nano-particle trapping. The proposed technology is a first step towards "smart-pore" fabrication where functional components are integrated in pores of sub-100 nm diameter.

ACKNOWLEDGMENT

The authors would like to thank Mark Smithers, MESA+ NanoLab, for his help in making the SEM and STEM images.

REFERENCES

[1] G. Barillaro et al., "A thick silicon dioxide fabrication process based on electrochemical trenching of silicon," *Sensors and Actuators A* 107 (2003) p. 279

[2] L. Fernandez et al., "Fabrication of thick silicon nitride blocks for integration of RF devices," *Electronics Lett.* , 41 3, (2005) p. 124

[3] C. Zhang et al., "Fabrication of thick silicon dioxide layers using DRIE, oxidation and trench refill," *Proc. 15th IEEE Int. MEMS Conf.*, (2002) p. 160

[4] J. Miao et al., "Fabrication of thick SiO2 block with dry-released underneath cavity in silicon for RF MEMS," *Electronics Lett.* , 41 11, (2005) p. 662

[5] N. Deo et al., "Conformal filling of silicon micropillar platform with ^{10}boron," *J. Vac. Sci. Technol.* B 26, (2008) p. 1309.

[6] L.F. Voss et al., "Analysis of strain in dielectric coated three dimensional Si micropillar arrays," *J. Vac. Sci. Technol. B* 31, (2013) 060602.

[7] S. A. Guerrera et al., "Self-aligned, gated field emitter arrays with integrated high-aspect-ratio current limiters*," Vacuum Nanoelectronics Conference (IVNC)*, 26th International (2013), 6624726

[8] S.A. Guerrera et al., "Nanofabrication of arrays of silicon field emitters with vertical silicon nanowire current limiters and self-aligned gates", *Nanotechnology*, 27 (2016), 295302

[9] S. S. Walavalkar et al., "Scalable method for the fabrication and testing of glass-filled,three-dimensionally sculpted extraordinary transmission apertures," *Nano lett.* 14 (2014), p.311

[10] H. Solak et al., "Displacement Talbot Lithography: A new method for high-resolution patterning of large areas," *Optics Express* 19 (2011), p. 10686

[11] H. Le The et al.,"Shrinkage control of photoresist for large-area fabrication of sub-30 nm periodic nanocolumns," *Adv. Mater. Technol.*, 12 (2017), 1600238

[12] S. S. Walavalkar et al., "Three-dimensional etching of silicon for the Fabrication of low-dimensional and suspended devices," *Nanoscale,* 5 (2013), p. 927

[13] S. S. Walavalkar et al., "Size tunable visible and near-infrared photoluminescence from vertically etched silicon quantum dots," *Applied physics Lett.* 98 (2011), 153114

[14] K. Korwin-Mikke et al.," Precision 3-D Nanomachining of Silicon Nanowires," *42nd International Conference onMicro and Nano Engineering*, (2016), p. 118

[15] E. Sarajlic et al., "Fabrication of 3D Nanowire Frames by Conventional Micromachining Technology," *Proc. Transducers 2005*, p. 27

[16] E.J.W. Berenschot et al., "3D Nanofabrication of Fluidic Components by Corner Lithography," *Small* 8 (2012), p. 3823