A SELF-ALIGNED WAFER-SCALE GATE-ALL-AROUND APERTURE DEFINITION METHOD FOR SILICON NANOSTRUCTURES

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ABSTRACT
A novel fabrication technique is developed to deliver self-aligned gate structures on vertically aligned periodic silicon nanocones with gate aperture radii of 65±3 nm and a surface density of 1.6 billion structures cm⁻² across the 100 mm diameter substrate scale. The silicon nanocones were obtained by a combination of ion beam etching and thermal oxidation whereas the gate structures were obtained by a combination of ion beam etching planarization and selective wet chemical etching.

KEYWORDS
Planarization, low energy ion beam etching, cold field emitters, self-aligned fabrication.

INTRODUCTION
Cold field emission (CFE) relies on the existence of strong electric fields near conducting surfaces. Characteristic for CFE is the relatively small electron energy spread, making CFE useful for obtaining bright and coherent electron beams. The present research focuses on the application of new emitter materials, emitter design, and fundamental theories for understanding CFE. Improving the current-voltage behavior of a CFE device is commonly achieved by optimized single emitter design, increased height over footprint ratio (also known as aspect ratio (AR) and/or optimized distance between emitters in a field emitter array (FEA) to increase the local electric field. Another way of increasing the local electric field is by decreasing the cathode-anode distance. However, the latter will also constrain the volume that is exposed to the electron beams. The application of a perforated electrical gate structure then proves beneficial, introducing an electrical potential close to the cathode, ideally collecting only a small part of the total CFE current. An additional benefit is that a gated FEA suffers less from the repulsion phenomena due to neighboring emitters. Existing and well-established techniques for gated FEA fabrication rely on chemical mechanical polishing (CMP), [1], Spindt-type fabrication by molding into anisotropic etched silicon, [2], or Spindt-type lift-off-based fabrication, [3]. Spindt-type fabrication processes typically yield a trade-off between the ability to obtain high AR structures and the surface density of emitting sites. CMP of micro-and nanostructured surfaces, like in the gated field emitter application, is done to planarize textured surfaces, removing offset surfaces and exposing buried materials which can then be contected, coated or etched. CMP-based fabrication on 3D structured surfaces is not trivial. For instance, differences in physical material characteristics and pattern-density can induce wafer-scale and pattern-scale height inhomogeneities such as erosion of mask or device materials and dishing. Furthermore, CMP-based fabrication lacks end-point detection, [4]. In this work, a novel fabrication technique for obtaining silicon nanocones with a self-aligned electrical gate structure is presented. Rotating angle timed ion beam etching (rat-IBE) in combination with thermal-oxidative sharpening yield solid silicon nanocones with a silicon dioxide shell. The nanocones are coated with electrically insulating, conducting, and capping layers. Subsequent use of rat-IBE for planarization of the capping layer and selective isotropic wet chemical etching of the conductive and insulating films forms an aperture. The aperture radii are controlled by the rat-IBE time and thickness of the conformal dielectric stack.

Figure 1: Cross-sectional SEM images of a) silicon nanowires, b) silicon nanocones after rat-IBE pre-shaping, c) after thermal oxidative sharpening, and LPCVD of Si₃N₄, d) and stripping of Si₃N₄ and t-SiO₂ in 85% H₃PO₄ and 1% HF, respectively. Measurements on the silicon nanocone heights were conducted via cross-sectional SEM images at different locations over a 100 mm diameter silicon substrate. The scale bars represent 100 nm. e) The nanocone height measurements are plotted as a function of the radial distance from the center of the substrate with N=14 measurements for each 95% Confidence interval.
RESULTS AND DISCUSSION

Silicon nanocone fabrication

A 100 mm diameter c-Si (100) substrate was fabricated into a substrate containing several mm² sized square periodic arrays of silicon nanowires with 250 nm pitch. Continuous-mode inductively coupled plasma reactive ion etching (CM-ICP RIE) of c-Si was conducted under a hybrid mask, yielding silicon nanowire arrays with a smooth sidewall (Figure 1a). Timing of the rat-IBE allows reducing the diameter of the top of the pre-shaped nanocone to a set value. This is important, as the next step was to sharpen the pre-shaped silicon nanocone by converting the core of c-Si into thermally grown silicon dioxide (t-SiO₂). For set temperature and environmental conditions, the self-limited diameter of the c-Si core of the cylindrical convex silicon nanostructure after oxidation was controlled by the diameter of the structure before oxidation. More importantly, the stress in the t-SiO₂ film at the apex of the silicon nanocone reduced the growth rate to such a significant extent that the top of the nanocone barely reduced in height (Figure 1b-d). After oxidation, the nanocones were subsequently coated with 13 nm Si₃N₄ (Figure 1c). Sharp silicon nanocone structures were obtained by etching the Si₃N₄ and t-SiO₂ in 85% H₃PO₄ and 1% HF, respectively (Figure 1d). After stripping, height measurements of the silicon nanocones at the cross-section of cleaved samples were conducted at various locations. Measurements show the obtention of c-Si nanocones with height variations <5 nm between neighboring tips, and <80 nm (15%) across a 100 mm silicon substrate (Figure 1e).

Self-aligned gate fabrication

For self-aligned gate fabrication, both polycrystalline silicon (poly-Si) and amorphous silicon (a-Si) LPCVD deposited layers were characterized. This way, the self-aligned fabrication performance is characterized both on rough and smooth films. Either a 35 nm poly-Si or a 50 nm a-Si layer was deposited conformally over the Si₃N₄ (Figure 2a). Subsequently, a 130 nm LPCVD SiO₂ capping layer was deposited conformally over the a-Si or poly-Si and annealed (Figure 2b). Planarization of the SiO₂ films was initiated by rat-IBE, in which Ar⁺ ions impede on the silicon surface giving a physical sputtering of the SiO₂. Rotating the substrate with an angular velocity, ω, around its central axis reduced self-shadowing effects. An oblique ion incidence angle, θ, prevented redeposition, as schematically presented in (Figure 2g). A secondary ion mass spectroscope was used to measure the mass ratios of sputtered materials in-situ. Changes in the ratios of measured silicon and oxygen content indicated that etching of a different material occurred, e.g. when etching through the SiO₂ reaching the a-Si layer. The angular dependence of the etch-rate was characterized by variable angle spectroscopic ellipsometry measurements on non-structured (flat) dummy substrates (Figure 2f). Choosing θ to be 45° facilitated the maximum etch-rate at the top of the curved SiO₂ surface. A rat-IBE step etched the SiO₂ capping layer, revealing the underlying a-Si or poly-Si film (Figure 2c). Also, at this point, the gate aperture was defined, which will be enlarged during the wet-chemical etching of the silicon gate material. Over-etching the SiO₂ capping layer yielded a larger aperture as the film retracted along with the a-Si or poly-Si films curvature. The SiO₂ and poly-Si in Figure 2c) were rat-IBE over-etched.
beneath the silicon gate material while the poly-Si film was present of only a thin layer of (native) silicon dioxide. Therefore, prior to OPD etching, the substrates were submerged in 1% HF for 1 minute to remove any (native) silicon dioxide present. In fact, this etching step also widened the SiO₂ capping aperture. Smaller apertures may be obtained by choosing a capping material that shows selectivity towards both OPD and HF. The a-Si substrate was etched in OPD for 09:30 (mm:ss), including 1-minute over-etching, to reveal the Si₃N₄ film beneath the silicon gate material while the poly-Si film was etched for 7 minutes (Figure 2d). Observations of the resulting gate apertures by top-view SEM images showed well-defined holes in the case of a-Si derived structures, whereas the poly-Si apertures showed significant line edge roughness. Cleaving and subsequent SEM imaging at the cross-section revealed the conformally coated silicon nanocones and opened a-Si apertures (Figure 2e). In the case of the a-Si apertures, the structures were sufficiently defined to allow automated measurements of the gate aperture radii at various locations on the substrate. Line edge roughness present and low contrast prevented automated measurements on poly-Si apertures.

**Gate aperture homogeneity analysis**

Top-view SEM images of the opened a-Si apertures (Figure 3a) were processed in Matlab i.e. binarization of the grey-scale image and application of a circle fitting algorithm to extract the aperture radii (Figure 3b). Together with metadata provided by the SEM, a confidence interval for the gate aperture radii was determined for different positions on the substrate surface (Figure 3c). Automated measurements show gate aperture radii of 65±3 nm. The apparent differences and variance of the nanocone heights across the substrate did not influence the gate aperture radii, as is evident from comparing of Figures 1e) and 3c). The increased variance for the heights is absent in the radii. This shows that individual gate apertures were self-aligned. Combining the determined rat-IBE and wet-chemical etching resulted in good control over the feature sizes. Furthermore, etching selectivity facilitated the use of only a single thin capping layer as a self-aligned hard mask. A thicker layer may increase the planarity of the rat-IBE step. The method performed well on the curved surfaces visualized by cross-sectional and top-view SEM images in Figure 4. It is observed that the t-SiO₂+Si₃N₄ insulating layer stack controlled the minimum distance between the c-Si tip and the a-Si film. The obtained homogeneity of the gate aperture radii at the wafer-scale demonstrates that the rat-IBE method leads to good conformality. This indicates that this method can be used complementary to CMP where height inhomogeneities of a polishing step on surfaces with a varying pattern-density and material compositions are a known issue. However, performance on rougher films is sub-optimal. An approach to optimize this might be similar to CMP where overfilling is used. Moreover, using rat-IBE in combination with secondary ion mass spectroscopy circumvents problems as end-point detection, planarization alignment, debris, and other contamination. Compared to Spindt-type fabrication this method allows the combination of high aspect-ratio structures with small gate apertures. Compared to the lift-off based Spindt-type fabrication the method shows relatively smooth tips. Mold-based Spindt-type fabrication also yields smooth tips but still suffers from the trade-off between surface density and AR. A possible future direction might be the combination of the method presented here and mold-based Spindt fabrication.

**CONCLUSION**

A self-aligned gate aperture definition method was proposed that utilized rotating angle timed ion beam etching and timed selective wet-chemical etching of conformally coated silicon nanocone arrays with intrinsic wafer-scale height inhomogeneities. Wafer-scale height inhomogeneities up to 80 nm did not propagate into the gate aperture radii, where the measured radii were 65 ± 3 nm. The homogeneity of the gate aperture radii through the rat-IBE method shows the added benefit over CMP, where optimization of a polishing step for surfaces with varying pattern density and material compositions is a known issue. The benefit over Spindt-type fabrication lies in the combination of small gate apertures and relatively high aspect ratio structures with smooth and sharp c-Si tips.

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Figure 3: An example of top-view SEM images of a-Si films used for measuring the gate aperture radii at various substrate locations, a), using an automated Matlab script, b). The scale bars represent 100 nm. The measurement results in c) show the measured mean radius of the gate aperture as a function of the radial distance from the center of the substrate with N>60 for each 95% Confidence interval.
METHODS

rat-IBE of silicon nanowires

The rat-IBE cycle of the silicon nanowires, the substrate was rotated with a rotational speed of 5 rpm and kept at $\theta = 45^\circ$. A 200V DC bias was applied to the acceleration grid while the substrate was kept at 204V DC relative to ground. A 300W power was supplied to the RF plasma generator fed with a 5 sccm argon flow. The pressure in the process chamber was maintained at 0.17 mTorr and also fed with a 5 sccm argon flow. The measured current through the substrate was 3 mA while the neutralizer current was set at 50 mA.

Thermal oxidation of silicon

Before oxidation, the etched substrates were cleaned by submerging in RCA-2 etchant (consisting of hydrochloric acid, hydrogen peroxide, and demineralized water in a (1:1:5)-ratio) for 15 minutes whilst the solution was kept at a minimum of 70°C. Next, the substrates were submerged 1 min in a 1% HF solution, QDR, and cleaned by two cycles in an ozone-steam bath, followed by another 1 min submersion in 1% HF, QDR and spin-drying. Oxidation of silicon was done in a tube. The substrates entered the furnace at 700 °C after which the system pumped to vacuum conditions. The temperature was then ramped to 900°C in ~20 minutes. The oxidation cycle was conducted under a constant oxygen flow of 2000 sccm for 01:10:00 (hh:mm:ss).

Stoichiometric silicon nitride deposition

Si$_3$N$_4$ was deposited in a tube furnace using LPCVD at 800°C employing 22 sccm dichlorosilane and 66 sccm ammonia gas flow.

Amorphous or polysilicon deposition

The a-Si layer was deposited in a tube furnace from a 50 sccm silane flow at 550 °C and 250 mTorr pressure for 25:00 (mm:ss), whilst a 35 nm poly-Si was obtained by deposition at 595 °C for 06:10 (mm:ss).

Silicon dioxide deposition

A 130 nm LPCVD SiO$_2$ capping layer was deposited in 12:50 (mm:ss) at 725 °C, 200 mTorr pressure, 40 sccm tetraethyl orthosilicate flow, and 30 sccm N$_2$ flow. Additionally, the substrates were annealed for 3h at 800 °C in an N$_2$ atmosphere.

rat-IBE of the silicon dioxide capping layer

During the rat-IBE cycle of the SiO$_2$ capping, the substrate was rotated with a rotational speed of 10 rpm all other settings were similar to rat-IBE of silicon nanowires. The etching was conducted for 14 minutes.

Measurement procedure

After etching, the substrate was cleaved and SEM images were recorded at the cross-section. Height measurements were conducted on several samples located at different positions over the 100mm diameter substrate. The height was extracted using ImageJ software by drawing line segments and determining the length in pixels, where scaling was applied based on the metadata provided by the SEM to convert to the physical length.

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Figure 4: Cross-sectional, a) and top-view SEM images, b) and c), of the gated silicon nanocone structure after stripping of Si$_3$N$_4$ and t-SiO$_2$. In a) the different materials are indicated together with the tip location. The scale bars represent 100 nm.