The Search for Resilience Weak Spots in Automotive Mixed-Signal Circuits

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Abstract— **This paper presents the search for and resulting effects of resilience weak spots in a commercial Local Interconnect Network (LIN) transceiver. Industrial reliability simulations based on aging of devices have been used to locate these weak spots. The objective is to improve the resilience of the circuit during its design and validation phase after determination of the weak spots. In the case of our target chip, this complete cycle was successfully completed. Finally a new simulation principle is being proposed in order to automate the search for weak spots to speed-up and strengthen this search. It enables at an early design stage to take appropriate counter measures to improve resilience.**

Keywords- resilience, reliability simulation, Design for Reliability, PBTI, automotive, analogue, mixed-signal, automated generation

I. INTRODUCTION

Automotive circuits share the design trend of shrinking manufacturing process dimensions. Shrinking has the advantage to reduce the size and cost of a circuit but it may also have negative impacts on especially reliability [1, 2]. For instance, the voltage threshold (V_{th}) drift due to Negative Bias Temperature Instability (NBTI) increases [3]. As automotive critical applications often operate in harsh environments, guaranteeing the reliability [4] and robustness [5, 6] of automotive circuits is crucial. The automotive sector is a perfect vehicle for study of this subject, as large chip volumes are involved, very strict cost budgets maintained, severe impact of lacking dependability on brand names can occur (e.g. Toyota), and huge financial claims expected in the case of fatal accidents (e.g. in the US). Concerning robustness, designers and test engineers normally ensure that the circuit works in the ranges of user settings given by the specifications. Concerning reliability, designers and test engineers will also ensure that the circuit will operate correctly for a given time in a given environment (described in the mission profile [7]). But there is now also an increased need to improve the *resilience* of analogue and/or mixed-signal (MS) safety-critical circuits.

Resilience is a widely addressed topic in network and computer engineering domains [8]. Reference [8] gives definitions of the *resilience* of a ubiquitous system (large, networked, evolving systems constituting complex information infrastructures):

> "the persistence of the avoidance of failures that are unacceptably frequent or severe, when facing changes"

The *dependability* of a system is its ability to manage failures. A dependable system is usually identified as a fault-tolerant one. Actually it includes several attributes [6, 9, and 10] which are subsequently Reliability, Availability, Maintainability and Safety. The latter is of special importance in the automotive sector [11].

The main difference between dependability and resilience is that we can distinguish between resilience and the other concepts by the fact that the resilience of the system is characterized by its ability to manage a wide range of *unexpected* defects while reliability or maintainability are defined according to a limited number of *expected* defects.

The resilience of a circuit is often defined by its ability to cope with stress and catastrophe. A 100% resilient circuit remains functional during and after external stress even in the case of internal degradation or malfunctioning. Resilience differs from reliability and robustness by including *rare* events and disturbances. Our definition is hence:

> "the resilience of a circuit is its ability to cope with stress and catastrophe due to unexpected but realistic usage conditions".

A *weak spot* has been defined as a location in the netlist of the system where an aging effect, irrespective of its origin, will cause the system to fail under certain conditions. These origins can be NBTI, Positive Bias Temperature Instability (PBTI), Hot Carrier Injection (HCI), Time Dependent Dielectric Breakdown (TDDB) or electron migration (EM) etc. [1]. The conditions can be power-supply or data / control variations in value and time. Resilience weak spots search is a complement to the work done to ensure robustness and reliability. This search for resilience weak spots is between reliability/robustness and HALT experiments (Highly Accelerated Lifetime Test). Indeed like for reliability and robustness, simulation is used to stress the circuit and like HALT, the objective is to stress the circuit to identify the weakest part of the circuit in order to strengthen the design. Little work has been carried out until now in the area of resilient car ICs. Our investigation for the search of resilience weak spots using reliability simulations is presented in the section II. To generalize this approach, we introduce in the third section a new simulation principle in order to automate and speed-up this weak spot search.

II. INVESTIGATION OF THE SEARCH FOR RESILIENCE WEAK SPOTS

The Target Circuit

The target circuit we used to search for resilience weak spots is a Local Interconnect Network (LIN) transceiver referred here as LIN IP (Intellectual Property). It was manufactured in the 140nm CMOS ABCD9 process of NXP. The LIN transceiver is a component which is widely used in the automotive industry. A LIN transceiver consists of a receiver (RX) and a transmitter (TX) [12-14]. Figure 1a

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shows the global set-up while Figure 1b presents a more detailed part of the transmitter.

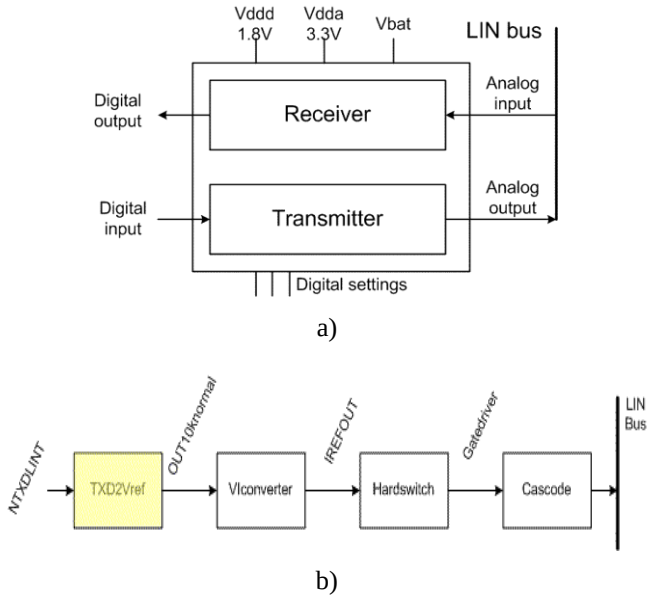

Figure 1: a) simple block diagram of the LIN-IP
b) detailed part of the transmitter (TX)

The receiver adapts signal levels from the analogue bus to levels expected by the digital controller. The transmitter converts the logic-bit signal received from the controller into a signal that is sent onto the analogue LIN bus (Figure 1b).

The design and test of the LIN transceiver are critical activities. For safety reasons the IC manufacturer targets for 100% test coverage and zero customer return (6-sigma) despite test escape or reliability failure being a circuit for automotive applications. Hence, standard design rules are to be followed to minimize the risk of different aging mechanisms. However, this only deals with the *expected* environmental situations, and not the case of resilience (*unexpected* environmental situations). In addition, in a modern car dozens of LIN buses are used to monitor the car environment or control dynamic behaviours [15] and more than 50 million cars are produced every year. As a consequence several hundred millions of LIN transceivers are produced every year. Finally it is important to search for resilience weak spots because the LIN-bus protocol corrects errors with the help of several techniques [15, 16], but it is only useful for transient faults (non-permanent, caused by environment) and not for permanent faults that can be the consequence of resilience weak spots.

A Reliability Simulator for the Search of Resilience Weak Spots

The reliability simulator PRESTO [17] has been used to look for resilience weak spots in the LIN IP. Parallel experiments carried out with Cadence's RelXpert simulator showed similar results in terms of accuracy. PRESTO is a proprietary software tool developed by NXP. It updates the regular netlist with *aged* device parameters. Aging is translated from stress to device parameters using a transient simulation and models of reliability failure mechanisms that have been characterized previously for individual transistors. The latter is the result of using a large number of industrial measurements.

In order to define usage conditions that induce resilience failures, many reliability simulations have been carried out for particular extreme settings and beyond specification usage that have been added to the mission profile [7]. This approach is coherent if one considers that the automotive environment is a harsh one. For instance circuits are normally characterized for temperatures up to 150°C, but an engine can probably go up to 185°C. It is noted that temperature is a main contributor to reliability failure mechanisms. As an example, Figure 2 shows the electrical simulation of the LIN IP Transmitter before and after aging.

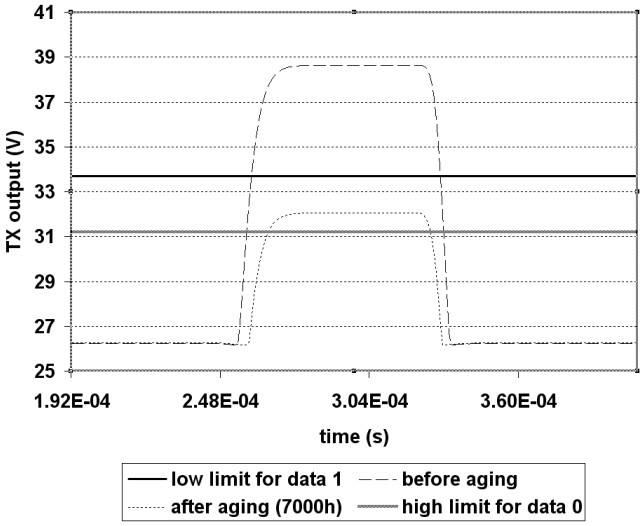

Figure 2: TX output response of a new and an extremely aged device

According to the LIN standard [18], there are limits to the levels of the analogue data "one" and "zero" being transmitted. These limits are shown in Figure 2 by two straight horizontal lines. It means that a transmitted "zero" should be below the full grey line to be correctly interpreted by remote receivers. And inversely a transmitted "one" should be higher than the full black line to be correctly interpreted by remote receivers. One can observe that after aging the circuit does not provide a sufficient high level for data "one" to be correctly interpreted by a remote receiver. This can cause the notorious "malicious inputs" for other chips connected to the bus. This behaviour is due to a particular aging configuration. The circuit has been powered down and the digital input is continuously stimulated by a constant voltage of 1.79V during 7000 hours at 175°C.

Figure 3 presents the weak part of the circuit, the TXD2Vref part (Figure 1b). The MP1 transistor has been affected by aging due to Positive Bias Temperature Instability (PBTI). Its V_{th} has shifted inducing a shift of its voltage source (*Vs*). The conditions required to induce the aging responsible for the resilience failure are particular. The circuit should be powered down first but it is still stimulated at the digital input of TX using a 1.79V DC signal, at 175°C. Without knowing this special aging condition, one can not observe such resilience failure. Fortunately this case can be easily avoided by using a switch just after the TX_digital_input line, controlled by the power supply. In the case the circuit is powered down, the digital input is isolated, thus avoiding voltage stressing. As a result of this simple *modification* of the original design, the resilience of the circuit has been increased.

This study has demonstrated the interest in looking for resilience weak spots. Circuits for critical applications such as automotive are designed to be very reliable and robust, usually following strict design rules. *Despite* that, a resilience weak spot has been found and a potential critical

usage condition has been avoided. Furthermore, the search of resilience weak spots has also an interest for non-critical application circuits. Usually reliability and robustness guidelines are less strictly followed for such applications and as a consequence there are potentially more resilience weak spots, and more critical usage conditions that can induce unexpected failures.

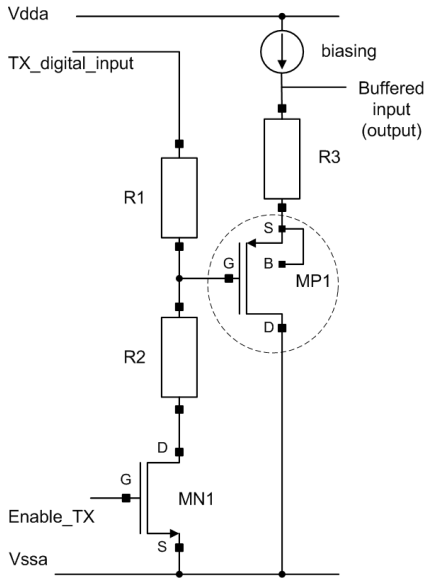

Figure 3: a resilience weak spot (MP1) due to aging

The search approach described in this section starts from usage conditions and subsequently to defects. This has two drawbacks. At first the number of different usage conditions is enormous because it is related to the number of inputs, including power supplies. As a consequence all usage conditions can not be simulated and as the circuit is basically reliable there was a need to run a lot of simulations which is extremely time-consuming. As a second drawback, this search can not ensure 100% coverage of resilience weak spots.

III. AUTOMATION OF RESILIENCE WEAK-SPOTS SEARCH

Basic principle

Considering the previous approach and its drawbacks, another approach should be used. We propose to use an ATPG-like (Automated Test Pattern Generation) approach. An ATPG-like approach means one that goes from defect to usage conditions. The basic principle is described thereafter.

The mathematical equation used during reliability simulation for computation of aging due to the PBTI mechanism is given by Equation (1). The stress is evaluated during a regular electrical simulation. Then it is extrapolated to the targeted age:

$$\Delta V_{fb} = \left(\frac{T_{age}}{T_{sim}} . \int_0^{T_{sim}} f(t) dt \right)^m \quad \text{(Eq. 1)}$$

where V_{fb} [V] denotes the flat-band voltage, a parameter of the transistor linked to the voltage threshold V_{th}. The targeted age is T_{age} [s], T_{sim} [s] is the electrical simulation time, and m [-] is a time-dependency exponent for permanent damage. The function of stress measurement over time is represented by $f(t)$, and given by Equations (2) and (3):

$$f(t) = |c(t)|^{\frac{1}{m}} \quad \text{(Eq. 2)}$$

$$c(t) = A . \exp\left(- \frac{E \cdot Q}{k.temp} \right) . p(t) \quad \text{(Eq. 3)}$$

Here E [eV] denotes the activation energy for permanent damage, Q [C] is the electron charge constant, k [J/K] the Boltzmann constant and temp [K] the temperature. A [V] is the scale factor for permanent damage. Finally $p(t)$ [V] is the function related to the stressor:

$$p(t) = \begin{cases} V_{GS}(t) & for\ V_{GS}(t) \geq 0 \\ 0 & for\ V_{GS}(t) < 0 \end{cases} \quad \text{(Eq. 4)}$$

$p(t)$ is a voltage equal to V_{GS} for positive V_{GS} or equal to zero for negative V_{GS}. This voltage is to the power n [1/V] being the oxide voltage factor for permanent damage. E, A, m and n are parameters characterized for a transistor for each technology. They can be measured or calculated.

In case of a positive DC stressing voltage, the aging model can be simplified to Equation (5).

$$\Delta V_{fb} = T_{age}^m . |c(t)| \quad \text{(Eq. 5)}$$

To summarize, as presented by Equation (6), the PTBI-related V_{fb} drift is a function of age, the temperature and the stressing voltage [19].

$$\Delta V_{fb} = g(T_{age}, V_{GS}(t), temp) \quad \text{(Eq. 6)}$$

Our initial idea comes from the observation of Equation (6). Indeed, as presented by Equation (7), for a given age, temperature and expected V_{fb} drift one should be able to compute the stressing voltage. As a consequence, the computed stressor, the temperature and the age will provide a usage condition that induces a failure due to a V_{fb} drift.

$$V_{GS}(t) = h(\Delta V_{fb}, T_{age}, temp) \quad \text{(Eq. 7)}$$

Considering a general case of stressing voltage, Equation (8), resulting from Equation (7), presents the integration over the electrical simulation time of the V_{GS} to the power m over n. The right-hand part is composed of known parameters (A, E, Q, k), the targeted voltage drift (ΔV_{fb}) and two parameters to be defined ($temp$, T_{age}). The variables $temp$ and T_{age} are defined according to the mission profile and can be set over the mission profile to find a resilience failure.

$$\int_0^{T_{sim}} V_{GS}^{n/m}(t) dt = \frac{T_{sim}}{T_{age}} . \left(\frac{\Delta V_{fb}}{A . \exp\left(- \frac{E \cdot Q}{k.temp} \right)} \right)^{\frac{1}{m}} \quad \text{(Eq. 8)}$$

In case that V_{GS}(t) is expected to be a digital signal with a 50% duty cycle, its amplitude V_{GS} is given by Equation (9).

$$V_{GS} = \left(\frac{2^m . \Delta V_{fb}}{T_{age}^m . A . \exp\left(-\frac{E \cdot Q}{k.temp} \right)} \right)^{\frac{1}{n}} \quad \text{(Eq. 9)}$$

Considering our study case in section II, for a constant stressing voltage, the inversed equation obtained from Equation (5) can be formulated by Equation (10).

$$V_{GS} = \left(\frac{\Delta V_{fb}}{T_{age}^m . A . \exp\left(-\frac{E \cdot Q}{k.temp} \right)} \right)^{\frac{1}{n}} \quad \text{(Eq. 10)}$$

By applying Equation (10) to the MP1 transistor (Figure 3), for a 250mV drift of V_{fb}, at a temperature of 175°C and for an age of 7000 hours, one obtains a constant V_{GS} stressing voltage gate of 1.79V. These values are the stressing conditions of the transistor that induce the resilience failure. In order to find the usage conditions that induce such resilience failure, the stressing conditions of the transistor should be backward propagated to the primary inputs.

According to Figure 3, for the V_{GS} of transistor MP1 to be equal to 1.79V, the biasing should be off; in other words the power supply should be off. Then V_S and V_G of MP1 are respectively equal to zero and 1.79V. As the Enable_TX command is provided by another block that is also powered down because of Vdda equal to zero, the value of this command signal is zero. As a consequence there is no current in the branch and the TX_digital_input value is equal to the V_G of MP1, being 1.79V. The usage conditions that induce the unwanted aging of the MP1 transistor are given in TABLE **1**.

TABLE 1: THE CRITICAL AGING CONDITIONS

TX_digital_input	1.79 V
Vdda	0 V
Temperature	175°C
Duration	7000 hours

Following this practical example, we have introduced the idea to set a resilience defect, in this example V_{fb} drift of a transistor, in order to compute the aging condition that causes this defect. Of course also other relevant effects of different aging mechanisms can be used. The interest in this approach is the possibility to automate this search. The principle of the search automation is introduced in the next sub-section.

Automation of search

The automation of resilience weak-spot search is mandatory for two reasons. First, setting reliability simulations "by-hand" does not provide an exhaustive search of weak spots. In addition, this by-hand approach is extremely time-consuming. As a matter of fact circuits for automotive applications are already designed to be robust and reliable and there is a need to perform a lot of simulations to find a relatively small number of weak spots. As a consequence, an automated approach is introduced that should be an innovative solution for resilience weak-spots search. In order to enhance the explanation, a practical circuit vehicle is provided to show steps in parallel of theoretical explanations.

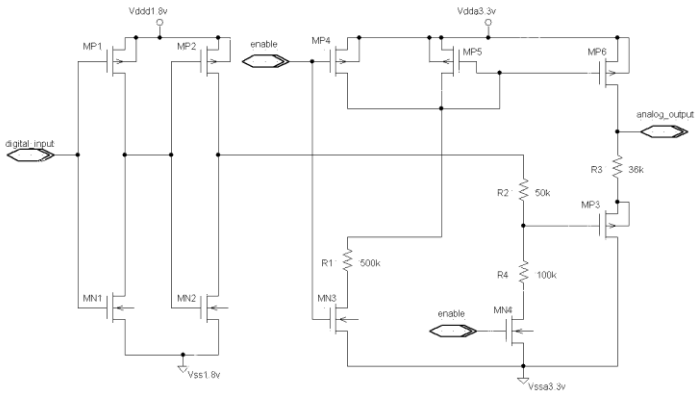

Figure 4: the mixed-signal input stage

The circuit used as practical example is presented in Figure 4. This is a mixed-signal (MS) input stage. At the left side, there are two inverters in series (MP1, MN1, MP2, MN2), used to speed-up the digital input signal transitions. Then three resistors (R2, R3, and R4) and a PMOS transistor (MP3) are used to shift and adapt the amplitude of the signal from the range 0 - 1.8V to the range 0.8 - 2V. The signal is adapted in amplitude for later signal processing. The remaining components (MP4/5/6, MN3, and R1) are parts of the biasing circuit of the analogue part of the circuit.

Three consecutive steps are required for our new approach. There are described in the following sub-sections.

Critical V_{fb} drifts

For each PMOS transistor of the netlist, a maximum V_{fb} drift is applied. The circuit is electrically simulated subsequently in order to test it and evaluate the impact of the V_{fb} drift on the circuit performances. If the V_{fb} drift induces a failure, then the transistor is considered as critical. Additional electrical simulations are carried-out using a dichotomy-based variation of V_{th} in order to define the lowest V_{fb} drift that induces a failure for critical transistors.

This first step finally provides a list of critical transistors with the lowest V_{fb} drift that induce a failure.

Considering the practical example (Figure 4), six electrical simulations have been carried out. For each of the simulations, one of the six PMOS transistors (MP1-6) has been affected by a maximum V_{fb} drift of 250mV. To simplify the example, only one V_{fb} drift of each transistor has been applied. The results are shown in TABLE **2**.

TABLE 2: RESULTS OF THE CRITICAL V_{FB} SHIFTS (FIRST STEP)

Affected transistor	*Impact on function*	*Critical V_{fb} drift*
MP1	Less than 0.1% variation of the duty cycle of the digital signal	No
MP2	Less than 0.1% variation of the duty cycle of the digital signal	No

MP3	Output signal over shifted of 200mV (Figure 5)	Yes
MP4	No impact	No
MP5	No impact	No
MP6	Strong delay on transition time of output signal and output signal shifted down by 400mV (Figure 5)	Yes

Figure 5 presents the output signal for a regular electrical simulation and for electrical simulations with MP3 and MP6 transistors affected by 250mV V_{fb} drift.

As a conclusion of this first step applied to the practical example, two PMOS transistors (MP3 and MP6) are considered as critical because the drift of their V_{fb} induces a significant variation in the function of the circuit which can be considered as a failure.

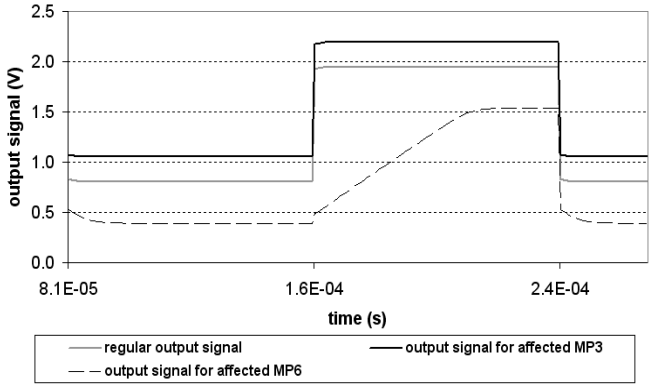

Figure 5: the regular output signal versus the output signal for affected transistor MP3 or MP6

Critical usage conditions

The second step consists in applying the inversed reliability model to the critical transistors for the previously defined V_{fb} drift in order to find the electrical conditions that induce these defects. Equation (8) provides the inverse reliability model for a particular case: a constant stressing V_{GS}. As the aging due to PBTI is related to the stressing voltage amplitude, a worst case can be considered by setting the stressing voltage as DC.

The inverse reliability model has been applied to the MP3 and MP6 transistors of the MS input stage. According to Equation (10), in order to minimize the value of the stressing voltage, the age and the temperature are set respectively to 10000 hours and 175°C. The aging duration and temperature have been arbitrarily chosen in this example. In case of an automated approach, we could have several values in order to provide several stressor values. In addition, these values could have been defined according to realistic values over the mission profile. Only one value of the aging duration and temperature are defined, in order to simplify the example. The results are given in TABLE **3**.

Next, the stressor and transistor-level voltage settings are being propagated backwards to the primary input to clearly define the usage conditions. It is similar to the structural ATPG backward propagation. The list of critical transistors is completed with the usage conditions corresponding to the corresponding V_{fb} drift. Those usage conditions are going to be sorted as *realistic* or *not realistic* for the next step. By realistic is meant a usage condition that is exceeding the mission profile and specifications but is still possible in reality.

TABLE 3: INVERSE RELIABILITY MODEL COMPUTATION FOR TRANSISTORS MP3 / 6

Transistor	Stressing V_{GS} (V)
MP3	1.74
MP6	1.74

Considering the example, the explanations on backward propagation are:

- With regard to MP6, this transistor is used as current source for MP3 biasing, and then V_{GS} is constantly equal to -800mV or 0V. As a consequence the stressing voltage of 1.74V can never be effective on MP6. Hence there is not any usage condition that can induce a critical aging of MP6.
- With regard to transistor MP3, in order to be able to have its V_{GS} equal to 1.78V, the biasing should be off. Then V_S is equal to zero and V_G to 1.78V. There are three possibilities to switch off the biasing: set the enable control signal to zero or switch off the Vdda3.3V power supply or both simultaneously.
  - In the first case, enable=1 and Vdda3.3v=0V, V_S is equal to 0 and V_G is equal to 1.74V. As the enable command is equal to one, transistor MN4 is conductive and according to the resistor values of R2 and R4, V_G of MP2 (V_G_MP2) should be equal to 2.62V. But V_G_MP2 is the output of the inverter powered by 1.8V. The only solution to observe the signal V_G_MP2 equal to 2.62V is to power the inverters by 2.62V. Finally in order to obtain this value of V_G_MP2, the digital input should be equal to 1.8V.
  - In the second case, enable=0 and Vdda3.3V=3.3V, like for the first case, V_G _MP3 is equal to 1.74. In this situation MN4 is opened and hence there is no current in the branch. As a consequence V_G_MP2 is also equal to 1.74V. In order to propagate this value back to the digital input, the two inverters should be powered to 1.8V and the digital input equal to 1.8V.
  - In the third case, enable=0 and Vdda3.3v=0V, the backward propagation of the stressor is the same as in the second case.

The summary of critical usage conditions inducing a critical V_{fb} drift of MP3 is provided in TABLE **4**.

TABLE 4: CRITICAL USAGE CONDITIONS

Digital input (V)	Vddd1.8 V (V)	Vdda3.3V (V)	Enable command	Age (h)	Temp (°C)
1.8	2.62	0	1	10000	175
1.8	1.8	3.3	0	10000	175
1.8	1.8	0	0	10000	175

Reliability simulation for global impact and validation

The realistic usage conditions corresponding to the V_{fb} drift of the critical transistors are used to run additional reliability simulations. These reliability simulations are used to validate the impact of the usage conditions on the targeted transistor and to evaluate the impact on the whole circuit. Note that the aging parameters of *all other* transistors are also taken into account.

Finally, reliability simulations for verification have been carried out with respect to the practical example under the critical usage conditions as previously defined. The circuit has been aging as expected and the failure was indeed observed at the output.

IV. CONCLUSIONS

The objective of this paper is to increase the quality of ICs by looking for weak spots to improve the resilience of circuits for automotive applications. A resilience weak spot can be found by carrying out reliability simulations over the specifications (time and temperature). As automotive application circuits are designed to be strongly reliable and robust, the search for weak spots under extreme conditions requires setting many reliability simulations and consequently it is extremely time-consuming. Therefore the idea was introduced of an ATPG-like simulation approach to accelerate this process while covering the entire product.

The basic principle of our automated search of resilience weak spots is based on the inversed model of PBTI. The inversed model of PBTI has been introduced, but it is obvious that a maximum number of reliability failure mechanisms should be considered in order to increase the efficiency of the resilience weak spot search. A similar inversed model can be obtained for NBTI [20, 21] and HCI [22].

The time consumption is obviously a critical parameter of the weak spot search. At first it appears clearly that our new approach is interesting because it reduces the number of reliability simulations to the critical settings previously defined. In case of very large scale integrated circuits, the complexity of backward propagation could be reduced by developing algorithms as has been done for ATPG in the past.

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