Fast Temperature Cycling Stress-Induced and Electromigration-Induced Interlayer Dielectric Cracking Failure in Multilevel Interconnection

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Abstract— **There is an increasing reliability concern of thermal stress-induced and electromigration-induced failures in multilevel interconnections in recent years. This paper reports our investigations of thin film cracking of a multilevel interconnect due to fast temperature cycling and electromigration stresses. The fast temperature cycling tests have been performed in three temperature cycle ranges. The failure times are represented well by a Weibull distribution. The distributions are relatively well behaved with generally similar slope (shape factor). The failure mechanism is well fitted by the Coffin-Manson equation indicating a uniform acceleration. The observation of cracking in the interlayer dielectric due to fast temperature cycling stress from failure analysis agrees well with the failure mechanism modeling and the calculated Coffin-Manson exponent. Electromigration experiments have shown that devices failed due to extrusion-shorts without increasing of resistance of metal line. The failure times are represented better by the Weibull distribution than by the lognormal distribution (normally used for electromigration data). A simulation of stress build-up in metal line using an electromigration simulator confirmed that the cracking of interlayer dielectric is the weakest spot and most likely to cause electromigration failure**.

Keywords— **Thermal cycling; Cracking; ILD;**

I. INTRODUCTION

With increasing power dissipation and decreasing chip size, thermal-mechanical and electrical current stresses-induced failures in multilevel interconnections are more likely to become a reliability problem. Temperature cycling was found to be one of the main factors that create stress cracking in thin films due to the large thermal mismatch among metallic and dielectric materials and the silicon substrate. Predictions of thermal cycling failure rates for integrated circuit (IC) have been widely discussed so far, because the temperature cycling test is extensively used in microelectronic industry to qualify new products [1]. Recent publications have addressed the issue of failures of interconnect systems due to temperature cycling [2-6]. It has been shown that temperature cycling can crack the metal films as well as interlayer dielectrics resulting in device failures. In order to use this understanding in reliability improvement of interconnect systems, the failure mechanism must be understood well enough to create a good failure rate model. However, a very fast thermal transients experiment to mimic temperature cycling in operational conditions cannot be carried out using an environmental chamber. The test condition in the environmental chamber is far from the real operation of IC's working at very high frequency, and possibly masks the failure mechanism more relevant to the field application and may actually prevent detection of failure mechanisms likely to occur in application environments. When the reliability problem of an interconnect system is concerned, the electromigration problem cannot be neglected. Even though the replacement of aluminum with copper will decrease the electromigration problem because copper has higher resistance to electromigration, one persistent problem remains, namely cracking of interlayer dielectric produced as result of stress build-up by electromigration. In this paper, we discuss two main aspects. First the thin film cracking induced by fast temperature cycling is treated; experimental technique, reliability testing, failure analysis, and a model to explain thin film cracking due to temperature cycling.

Second the thin film cracking induced by electromigration is dealt with experimentally and numerically using an electromigration simulator.

II. EXPERIMENTAL TECHNIQUE

To carry out the fast temperature cycling and electromigration experiments, the test chip was designed, including a number of important features. There is a very large n^+-Si resistor (about 4 Ω) just below the die surface where a very long meandering metal level 1 (M1) is located, the total length and width are 4000µm and 3.5µm, respectively. The n^+-Si resistor can be used to generate a high temperature transient. The temperature can be measured with an integrated diode as temperature sensor in the middle of the resistor. Extrusion monitors in M1, between the meandering line, and in metal level 2 (M2), a large plate above the whole structure, allow detection of short circuits due to extrusion. A part of the very long meandering M1 resistor (about 12Ω) can be used for electromigration testing. The top view of the test chip is shown in Figure 1. The test chips were processed in a standard two level metallization technology at a bipolar fab and it is encapsulated in a 17 pins power package. A special set-up is developed for the fast temperature cycling that can be used for reliability testing, and a simple scheme to generate and to monitor during temperature cycling is also shown in Figure 1. Details about the calibration and reliability test system can be found elsewhere [7,8]. The electromigration experiments are done using commercial electromigration testing equipment (DESTIN)[9].

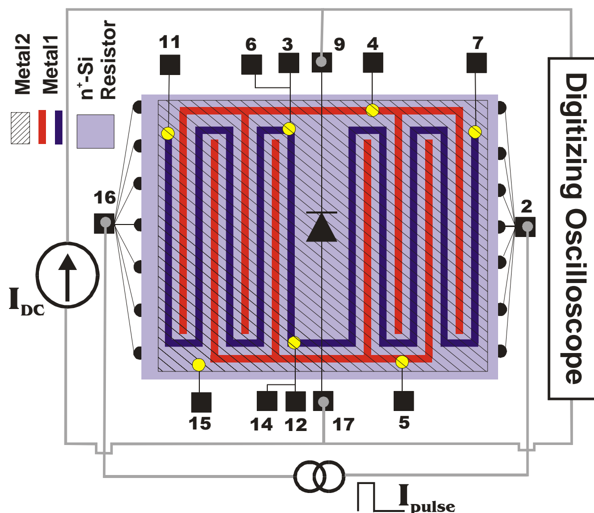

Fig. 1. Top view of test structure with hooking-up scheme to generate and to monitor the fast temperature cycling.

III. RESULT AND DISCUSSION

A. *Fast temperature cycling induced thin film cracking*

1) Reliability tests with fast temperature cycling

The reliability tests with fast temperature cycling have been carried out with three temperature cycle conditions.

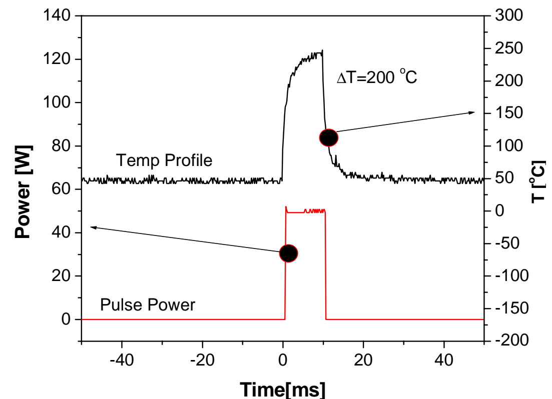

Fig. 2. Temperature cycling profile in case of temperature range of 200 °C, only one cycle shown.

The temperatures of conditions A, B, and C were cycled between 46 and 266 °C, 46 and 246 °C, and 46 and 226 °C, respectively. The temperature cycle frequency and duty cycle have been kept the same values of 10Hz and 10% for the three conditions. One example of the temperature cycle profile, which has been measured during the fast temperature cycling test with the condition B, is shown in Figure 2. During temperature cycling, an electrical current of 0.015MA/cm^2 was passed through the metal line to detect extrusion short-circuits. This current should not impose any electromigration-induced damage on the metal line.

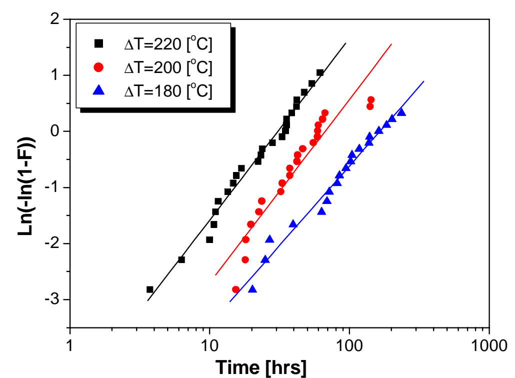

Fig. 3. Weibull failure probability plot for fast temperature cycling with temperature ranges of 220, 200, and 180°C.

A sample size of 24 devices was subjected to each condition and the device was considered to have failed

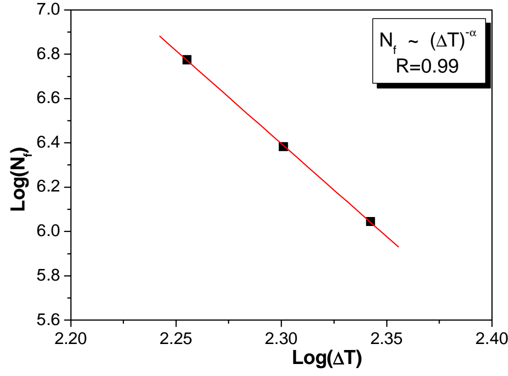

Fig. 4. Coffin-Manson plot for three temperature ranges.

Table 1
Results of median time to failure and shape factor

Conditions	A	B	C
	(ΔT=220°C)	(ΔT=200°C)	(ΔT=180°C)
T_{50}[hours]	30.8	66.9	165.2
β	1.4	1.4	1.2

when a significant voltage had appeared on any one of extrusion monitors. The failure time data are analyzed assuming a Weibull distribution, because the Weibull distributions are applicable in case where the weakest link, or the first of many flaws, propagates to failure. We observed that the failure mode is extrusion short-circuits, which suddenly happens during lifetime tests indicating a weakest link like the failure mode. Therefore, failure times would be better fitted by the Weibull distribution than by the lognormal one. By using a least square method of fitting Weibull distribution to time-to-failure data as shown in Figure 3, the median time to failure, t_{50} and the shape factor, β were extracted from the three stress conditions as summarized in Table 1. The distributions are relatively well behaved with similar shape factor, which suggests that the failure mechanism is the same for the three conditions.

It is noted that the temperature cycling failure mechanisms fit a power law relation [1], also known as the Coffin-Manson equation as follows:

$$N_f=C_0[\Delta T-\Delta T_0]^{-q} \quad (1)$$

Where N_f is the number of cycles to failure, C_o is a material-dependent constant, ΔT is the temperature cycling range, ΔT_0 is portion of the temperature cycling range in the elastic region, and q is the Coffin-Manson exponent determined experimentally.

It is noted that if the elastic range (ΔT_0) is much smaller than temperature cycle range (ΔT), it maybe dropped without any error being introduced (valid for most practical situation). Thus,

$$N_f=C_0(\Delta T)^{-q} \quad (2)$$

Because there was the same failure mechanism for all three conditions in our case, the Coffin-Manson exponent could be determined by using a least square method of fitting N_f and ΔT to equation (2), the results are shown in Figure 4. We found out the Coffin-Manson exponent q to be 8.4. The data in a recent publication [1] suggested that the Coffin-Mason exponent values in 2-4 range for metal-related mechanisms and 7-9 for brittle-related mechanisms. Therefore, from the Coffin-Manson exponent value found in our cases that we conclude that the failure mechanism is cracking of interlayer dielectric (ILD) causing the extrusion short-circuits.

2) Failure analysis

The SEM verifications on the surfaces of M1 have been done with fresh and failed devices (see Figure 5), the M1 surfaces of stressed devices showed many cracking places. The cross-section, which has been made by chemical polishing and viewed by SEM showed the cracking of ILD and extrusion between M1 and M2 (see Figure 6). This failure analysis confirmed again the observation from the Coffin-Mason model.

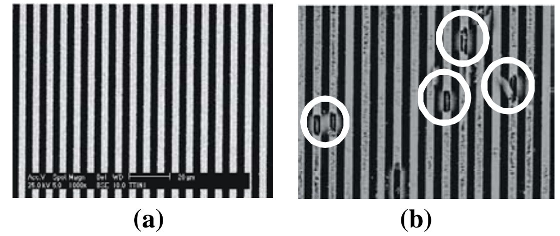

Fig. 5. The SEM verification of surface of metal level 1, (a) fresh devices, (b) more than 100 h stress at ΔT=220 °C.

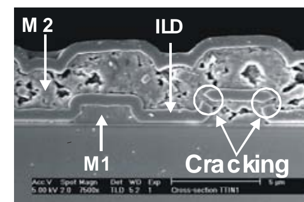

Fig. 6. SEM photo of cross-section showing the cracking of the interlayer dielectric due to the temperature cycling stress.

3) Failure mechanism modeling

From the results of lifetime test and failure analysis, we can summarize the observations that due to the temperature cycling, the ILD crack and aluminum can penetrate through the cracking places causing the extrusion short-circuit failures. Here, we applied a mode

suggested by Huang [10] to explain our experimental observations.

The packaging substrate has a larger thermal expansion coefficient than silicon chip. Upon cooling from bonding temperature, the substrate will contract more than the chip, but the boding prevents sliding between the substrate and the chip. As a result, shear stresses will develop on the chip surface, concentrated at the chip corner, pointing to the chip center [10] as shown Figure 7. More detail about the calculation of the shear stresses can be found elsewhere [11]. The shear stresses, however, were limited by the yield strength of the polymer (package), which is in the range 50-100 MPa. In our case, the yield strength of aluminum exceeds 100MPa, and the fracture strength of SiN is on the order of GPa [12]. Therefore, this low shear stress level cannot crack the high strength SiN film. Why does cracking occur after temperature cycling? The large difference in thermal expansion coefficients between the aluminum and silica causes metal films to deform plastically during temperature cycling. As illustrated in Figure 7, the shear stresses due to the packaging, which do not change the direction due to a lower temperature cycling than the boding temperature direct the aluminum pad to deform incrementally in the same direction. The aluminum gains a small amount of plastic deformation in each cycle. After many cycles, the accumulated deformation can be very large. This incremental deformation causes a distortion of the overlaying SiN toward the direction of the shear stresses that can build up a high level stress in overlaying SiN. As the stress can exceeds the fracture strength of SiN, and caused the cracking. During subsequent temperature cycle stress, overlaying SiN can be crawled as shown in Figure 8.

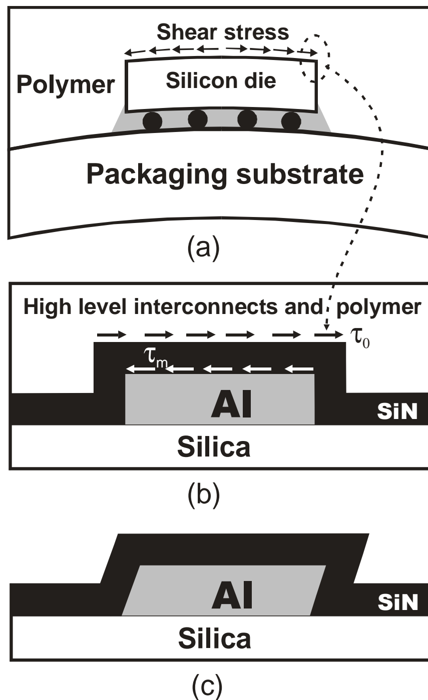

Fig. 7. The idealized model for thin film cracking due to plastic deformation after temperature cycling.

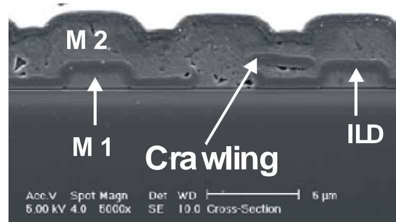

Fig. 8. SEM photo of cross-section showing the crawling of interlayer dielectric due to the subsequent temperature cycling stress.

B. Electromigration induced thin film cracking

1) Reliability tests with electromigration

Table 2
Stress conditions of electromigration tests

Conditions	E1	E2	E3	E4
J [MA/cm^2]	1.5	1.5	2.5	2.5
Ambient temp [^{o}C]	125	150	125	150

The electromigration lifetime tests were carried out with stress conditions, are shown in Table 2. A sample size of 16 devices was subjected to each condition. The electromigration tests involved continuously monitored the resistance of each test line and the voltages of three extrusion guards. The electromigration tests were carried out exceeding 3000 hours and we found out that there was not any increase of resistance of any metal line with these 4 stress conditions. Maybe these stress conditions were not accelerated enough. However, we observed that there are 16 and 10 devices failed due to the extrusion-short with stress conditions of E3 and E4, respectively. The times to failure were estimated using the extrusion short-circuit as the failure criteria (like the fast temperature cycling tests), not using a given percent of relative resistance change as failure criteria like usually using for electromigration failure. Therefore, the failure times were both plotted by lognormal distribution (normally used to analyze the electromigration data) and Weibull distribution for comparison as respectively shown in Figure 9a and 9b. In the Weibull plot, Figure 9b, the lines are very nearly parallel which means they can each be represented by the same distribution parameter The distribution parameter, β, is found to have

value of approximately 2.0. This implies that there is the same failure mechanism in this test. In lognormal plot, the lines are less parallel which lead one to conclude that the failure distribution due to extrusion short circuits in electromigration tests can better be represented by the Weibull distributions. For the lower current density cases (1.5MA/cm^2) for both temperatures, there is no device failed until 3000 hours stress. This suggested that an electrical current stress plays a more important role in the cracking of ILD caused extrusion fail than temperature ambient. It may be explained by the fact that the stresses are locally built-up in metal lines and these stresses can exceed the fracture strength of ILD and cause the cracking. However, the most dangerous location is the anode where there is a blocking boundary

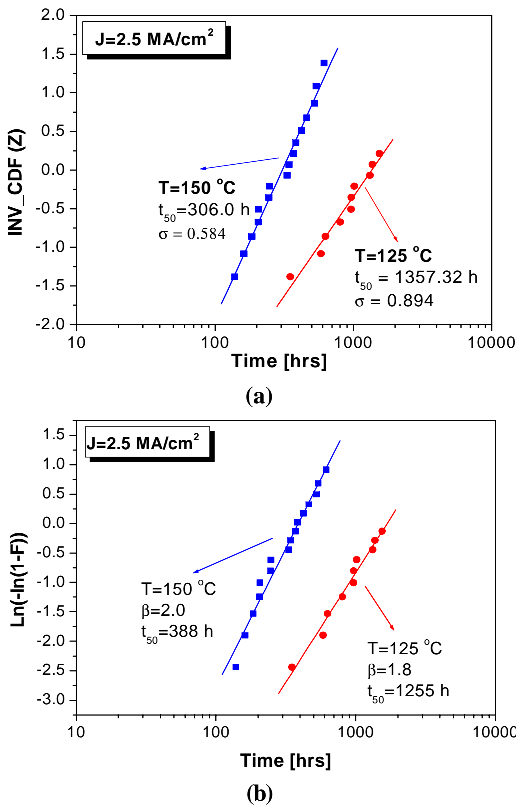

Fig. 9. Lognormal, (a) and Weibull, (b) failure probability plots for electromigration with current stress of 2.5MA/cm^2 and temperatures of 150°C and 125°C.

and an accumulation of metal atoms moved away from the metal line.

2) Electromigration simulation to verify a no cracking condition

Recently, Suo [13]has established a no-cracking condition for small objects that is

$$\beta P_{\max} \sqrt{W} < K_c \qquad [3]$$

Where, P_{max} is maximum hydrostatic pressure in the metal line, β is a geometric factor, W, is dimension characteristic of the interconnect cross-section, chosen to be the linewidth. K_c is the fracture resistance of layer overlaying metal line.

To verify the condition in our case, we have carried out an electromigration simulation with the same condition as E4 of the experiment. The mechanical stress distribution in the metal line after 3000 hours of current stress is shown in Figure 10. We observed that the maximum of compressive stress built up at anode and it reached up to 1GPa (see Figure 11). To verify the condition with the simulated stress, we have taken values β=0.5 and K_c=0.5MPa.m$^{1/2}$ from literature [13]. The linewidth of the metal line, W, is 3.5µm. The calculated

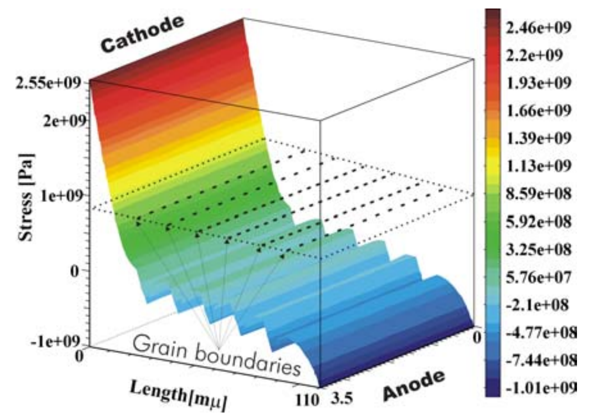

Fig. 10. The simulation of stress build-up in a metal line after 3000 hours of current stress and temperature of 2.5MA/cm^2 and 150°C, respectively.

value of $\beta P_{max} W^{1/2}$ for our samples is about 0.9 MPa.m$^{1/2}$. It shows that the no cracking condition is exceeded, which means the overlaying SiN can be cracked by electromigration stress with the condition E4.

IV. DDITIONAL OBSERVATIONS

Although the thrust of this work has been on fracture of the constraining dielectric, there are significant other implications for new generation of copper interconnections in low permittivity interlayer dielectric currently under development. First, the replacement of Al with Cu suggests that the time taken to buildup a particular stress in line is significantly longer due to the copper's higher resistance to electromigration. However, it is pertinent to mention that the fracture toughness of interfaces with low-K dielectric reported to date that are also lower that the conventional dielectrics [12] so that the cracking of the low-K dielectric due to the

electromigration stress is significantly shorter. Second, and potentially far more important is that the new low-K dielectrics are considerably more compliant that either PECVD SiO_2 or SiN_x. Consequently, they are less able to constrain the distortion of interconnects in respond to temperature cycling or thermal shock of plastic packages.

V. CONCLUSION

A fast temperature cycling method has been presented that can be used for reliability testing and studying the failure mechanisms of interconnect systems of power IC's. The shape factors of Weibull failure time distribution plots for three temperature ranges (ΔT) are comparable, which suggests the same failure mechanism. The exponent, q, in the power law expression was found to have a value of 8.4 which is consistent with a brittle fracture, as was confirmed by failure analysis showing cracking of interlayer dielectric after temperature cycling. Not only temperature cycling, but also current stresses can cause cracking of interlayer dielectrics. Simulation of stress build-up due to electromigration confirmed occurrence of mechanical stresses exceeding the yield strength of the interlayer dielectric.

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REFERENCES

[1] EIA/JEP122:"Failure mechanism and model for silicon semiconductor devices", EIA/JEDEC Pub. Dec. 2001.

[2] Cory AR. Improved reliability prediction through reduced-stress temperature cycling. Proc. of the 38th Annual Intl. Rel. Phys. Symp. 2000:231-235.

[3] Dunn CF and McPherson JW. Temperature cycling acceleration factors in VLSI application. Proc. of the 28th Annual Intl. Rel. Phys. Symp. 1990:252-258.

[4] Blish RC and Vaney PR. Failure rate model for thin film cracking in plastic ICs. Proc. of the 29th Annual Intl. Rel. Phys. Symp. 1991:22-29.

[5] Blish RC. Temperature cycling and thermal shock failure rate modeling. Proc. of the 35th Annual Intl. Rel. Phys. Symp. 1997:110-117.

[6] Zelenka RL. A reliability model for interlayer dielectric cracking during temperature cycling. Proc. of the 29th Annual Intl. Rel. Phys. Symp. 1991:30-34.

[7] Nguyen VH, Salm C, Vroemen J, Voets J, Krabbenborg B, Bisschop J, Mouthaan AJ, and Kuper FG. Fast thermal cycling stress and degradation in multiplayer interconnect. Proc. of the 4th Annual Workshop on Semiconductors for Future Electronics, 2001:136-141.

[8] Nguyen VH, Salm C, Vroemen J, Voets J, Krabbenborg B, Bisschop J, Mouthaan AJ, and Kuper FG. Test chip for detecting thin film cracking induced by fast temperature cycling in multilevel interconnect. To be published in Proceedings of the 9th Intl. Symp. on the Physical and Failure Analysis of Integrated Circuits, 2002.

[9] DESTIN User Manual for Electromigration-Stressmigration-Interconnection.

[10] Huang M, Suo Z, and Ma Q. Metal film crawling in interconnect structures cause by cyclic temperatures. Acta mater, 2001:3039-3049.

[11] Ohring M. Reliability and failure of electronic materials and devices. Academic Press Ltd, UK, 1998:411-471.

[12] Moore TM, Hartfield CD, Anthony JM, Ahlburn BT, Ho PS, and Miller MR. Mechanical characterization of low-K dielectric materials. Proc. of the 15th Annual Intl. Conference on Characterization and Metrology for ULSI Technology, 2000:431-438.

[13] Suo Z. Stable state of interconnects under temperature change and electric current. Acta Mater.1998:3725-3731.