

Selectivity Versus Noise Trade-Offs in Resistively Driven Passive Switched-Capacitor Infinite Impulse Response Low-Pass Filters

Roel Plompen¹, Graduate Student Member, IEEE, Jeroen Ponte¹, Graduate Student Member, IEEE, Stef van Zanten¹, Graduate Student Member, IEEE, Eric A. M. Klumperink¹, Fellow, IEEE, and Bram Nauta¹, Fellow, IEEE

Abstract—In this article, we derive a practical limit on the maximum achievable selectivity of three commonly used Passive Switched-Capacitor (PSC) Infinite-Impulse Response (IIR) low-pass filter (LPF) topologies driven from a resistive source. We show that filter topology selection and component dimensioning aimed to improve the selectivity of these filters will necessarily degrade the Noise Figure (NF), revealing a selectivity versus NF trade-off. We subsequently capture this in selectivity versus NF graphs. These graphs quantify the limitations on achievable selectivity and NF for each topology given the number of filter poles, and graphically provide guidance in navigating the trade-off between them. The three considered topologies mainly differ in how the sampling capacitor resets, inverts, or holds its voltage between clock periods. We capture the handling of the sampling capacitor as a new design parameter. We derive a singular model to encompass the entire design space consisting of the three topologies, filter order (number of history/integration capacitors), clock frequency, and component dimensions. The model comprises an adjoint network with a state-space description and is used to analyze the filter transfer function (to quantify selectivity), input- and output-referred noise, and NF.

Index Terms—Adjoint network, analysis, charge rotating, design strategy, infinite impulse response (IIR), low noise, low-pass filter, selectivity, state space, switched capacitor, passive.

I. INTRODUCTION

THE growing number of radio spectrum users has increased demand for interferer robust radio architectures. Integrated filters [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15] are tasked with attenuating interfering signals before they reach sensitive circuits. The challenge in designing these filters is maximizing filter selectivity (i.e., approximate an ideal ‘brick wall’ filter as closely as possible) while ensuring sufficiently high linearity and low noise to avoid corrupting the desired in-band signals. This functionality can be implemented with e.g. the use of active

Received 22 August 2024; revised 28 December 2024; accepted 14 January 2025. This was supported in part by European Research Council (ERC) under European Union’s Horizon 2020 Research and Innovation Programme under Grant 834389 and in part by the Nationaal Groeifonds 6G Future Network Services. This article was recommended by Associate Editor J. Goes. (Corresponding author: Roel Plompen.)

The authors are with the IC Design Group, University of Twente, 7522 NB Enschede, The Netherlands (e-mail: r.plompen@utwente.nl).

Digital Object Identifier 10.1109/TCSI.2025.3531706

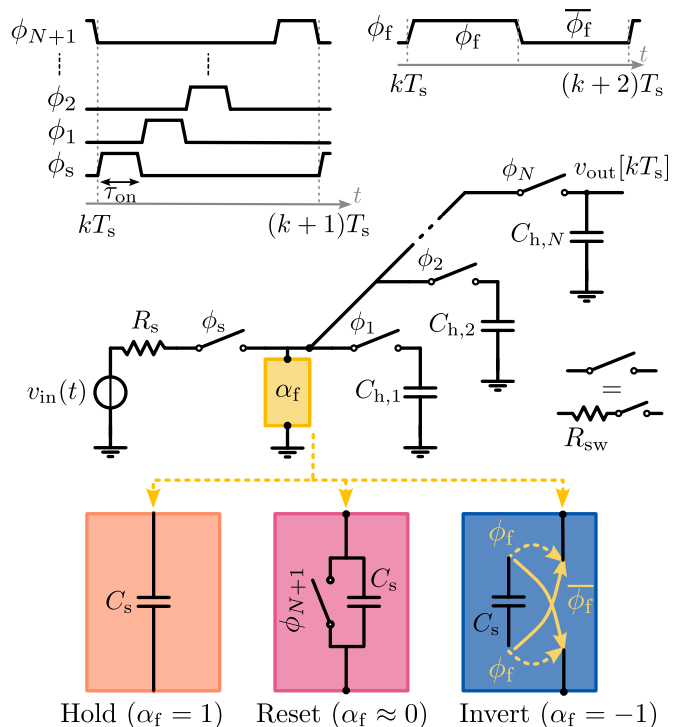


Fig. 1. Generalized N^{th} -order PSC-IIR LPF driven from a source resistance R_s . The box with α_f models three different ways of handling the sampling capacitor C_s , namely hold, reset, and invert. When $\alpha_f = 0$, $R_s = 0$, the implemented filter represents the “voltage-sampling mode” from [1], or the RF pre-filter from [2] for $R_s = 50\Omega$. For $\alpha_f = -1$, the topology is similar to [3].

linear amplification as done in Op-amp RC, Gm-C, and (super) source follower filters [6], [7], [11], [13], using a (fully) Passive Switched-Capacitor (PSC) Infinite Impulse Response (IIR) filter [1], [2], [3], or a combination of linear amplification followed by a PSC-IIR filter [8], [9], [14].

Implementing high-performance linear amplifiers in modern deep-nanoscale CMOS is increasingly challenging [16]. In [17], the author proposes an alternative “No Gain” approach, altogether avoiding the use of active linear amplifiers and instead relying only on passive components and (CMOS) switches. In shrinking technology nodes with more dense metals, capacitors occupy less area, and CMOS switches

exhibit reduced parasitic capacitance for a given on-resistance, making deep-nanoscale CMOS favorable for a “no gain” approach. The authors of [1], [3], and [15] point to the transconductance cell preceding a highly linear PSC-IIR Low-Pass Filter (LPF) as the chief overall linearity bottleneck for the structure, therefore, omitting it would benefit overall linearity. Thus, (fully) PSC-IIR LPFs seem attractive candidates for modern deep-nanoscale CMOS, and this filter category will be the focus of this article. In following this “No Gain” approach to make PSC-IIR LPFs that do not contain active linear amplification, the resulting switched-capacitor filters are driven directly from a resistive source impedance. This has considerable implications on the attainable filter selectivity and Noise Figure (NF).

Recent examples of PSC-IIR LPFs in literature [1], [2], [3], aimed to either improve selectivity or NF over a simple Switched-Capacitor (R)C [18], all use a sampling capacitor (C_s) that samples an input signal, and charge-share the sampling capacitor with integration/history capacitor(s) (C_h) sequentially one after the other. The main difference between them lies in the treatment of the sampling capacitor C_s after charge-sharing with the last C_h , before acquiring a new input sample (i.e., during ϕ_{N+1}). C_s can either be reset, flipped (inverted), or left unchanged (hold). See colored ‘ α_f ’ boxes in Fig. 1. We capture the permutation in circuit topology as a new design parameter: “feedback factor” α_f . Using α_f , we present a single model capable of analyzing all three topologies simultaneously, including the effects associated with resistive source impedance that are inevitably present in a (fully) PSC-IIR LPF. This enables computation and an apples-to-apples comparison of their key performance metrics, such as filter selectivity and NF. We will show how the combination of finite source resistance, feedback factor α_f , and component sizing, places a lower limit on the achievable NF for a given filter selectivity, while sampling capacitor C_s directly controls the trade-off between them.

To illustrate the significance of these limits and the present trade-off, we illustrate how α_f and the presence of a (50 Ω) source impedance affect filter performance. In Fig 2, we show five transfer characteristics made with three different PSC-IIR LPF topologies (α_f). All filters contain four filter poles and are designed for the same -3 dB bandwidth. In this article, we will show that the topology denoted with $\alpha_f = -1$ (Invert), which is based on [3], yields the best filter selectivity (lowest transition bandwidth) due to the presence of complex poles. However, it *cannot* have an NF less than 4.9dB when driven directly from a finite source impedance. We will show that to reach a lower NF of 4dB, the filter topology has to be changed to the ‘Reset’ ($\alpha_f \approx 0$) topology, which is based on [1], [2]. We will show that from a selectivity vs. NF perspective, there is an optimum design that has the lowest attainable NF of around 4dB and always has the (all real-pole) selectivity (filter shape) as shown in Fig 2.¹ In certain applications, the in-band losses for $\alpha_f \in \{0, -1\}$ can

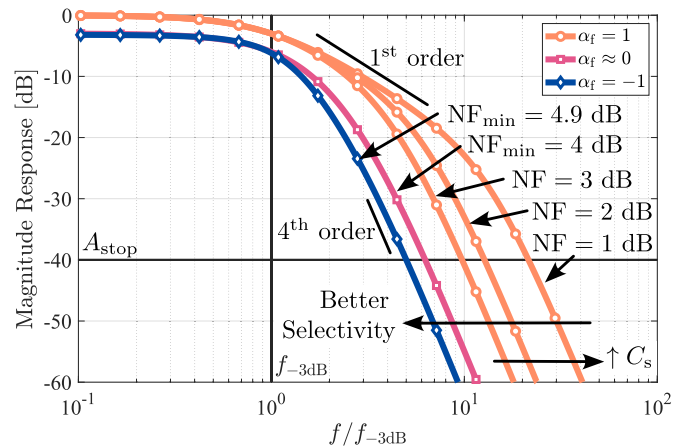


Fig. 2. Transfer functions and annotated NF of five PSC-IIR LPF implementations made using three filter topologies (different α_f). See the generalized network in Fig 1. All filters have the same filter order and -3 dB bandwidth (by adjusting C_h). For $\alpha_f = 1$, C_s is increased to reduce NF, for $\alpha_f \in \{0, -1\}$ changing C_s does not improve NF.

be used for input matching purposes (e.g. as done in [2]).² Reducing NF further necessitates changing the topology to $\alpha_f = 1$ (Hold), which inadvertently decreases selectivity as this topology has a low-frequency pole that causes an initial first-order frequency response before additional filter poles come into effect. With $\alpha_f = 1$, it is possible to reduce NF further than shown in Fig 2, at the expense of selectivity, by changing the size of the sampling capacitor. For $\alpha_f = 1$, the NF is improved by increasing C_s . For $\alpha_f \in \{0, -1\}$, there is a specific value for C_s (given f_s , R_s , N) that minimizes NF (indicated with NF_{\min} in Fig 2). As we will show in Section III, for $\alpha_f \approx 0$, deviating from the optimum C_s only degrades NF without a change in selectivity (shape of the TF in Fig 2). If $\alpha_f = -1$, a marginal selectivity improvement is possible for smaller C_s , at a degraded NF.

Filter designers often work towards a specific required selectivity (e.g., a transition bandwidth until a stop-band attenuation, A_{stop} in Fig 2, is reached) and/or a specific noise requirement. We will capture the selectivity (transition bandwidth) as a single value and plot it versus the NF for different combinations of α_f , number of history capacitors C_h (filter poles), and sample capacitor size. This enables designers of PSC-IIR LPFs to use our model and resulting selectivity vs. NF graphs to translate their selectivity and NF requirements directly into one of the three topologies while simultaneously extracting the required number of history capacitors and sample capacitor size.

The generalized circuit (Fig 1), including α_f , contains eight degrees of freedom. Exhaustively analyzing the design space with this many degrees of freedom using Linear Periodic Time Variant (LPTV) simulation tools, such as Spectre X, poses significant challenges, including possible user intervention in changing network topology (both α_f and number of C_h), monitoring of the simulation accuracy/validity, especially for noise simulations around extreme cases, and simulation duration.

¹We assume a fixed number of filter poles here. We discuss the effect of changing the number of filter poles on this result in Section III-E.

²As this introduces additional limitations, we will not include input matching as a requirement going forward.

Instead, we propose an accurate mathematical model that can easily be used to evaluate the performance of a large amount of implementations quickly without user intervention. The periodic and sampled nature of the generalized PSC-IIR LPF forms the basis of the analysis. We formulate a discrete-time state-space description of the periodicity of the adjoint network [19] of the generalized filter to find the filter transfer function (TF), similar as in [20]. We extend the analysis in [20] by computing the input and output referred noise density over frequency, which we use in evaluating the NF of the PSC-IIR filter. The model also yields expressions for the (complex) pole locations as functions of the network parameters (Spectre X currently does not offer pole and zero locations as functions of circuit component parameters). The resulting Pole-Zero plots provide insight into how filter poles move differently to changes in component values depending on α_f . Though mathematically more involved than [21], our approach will yield accurate results up to the Nyquist frequency, places less stringent assumptions on the ratio of C_h to C_s , incorporates effects of a finite source and sample switch impedance for both TF and NF, and relies on less simplifications for calculating noise behavior. These aspects are crucial to allow us to explore the broad design space, including extreme cases, encompassed by the circuit in Fig 1.

The remainder of this article is organized as follows. In Section II, we will derive a model to analyze the generalized filter in Fig 1. In Section III we will explore the design space encompassed by Fig 1, and discuss the design trade-offs. Appendix A outlines a procedure to use the presented selectivity vs. NF graphs to synthesize a PSC-IIR LPF.

II. ANALYSIS OF THE GENERALIZED PASSIVE SWITCHED-CAPACITOR IIR FILTER

In this section, we analyze the generalized PSC-IIR LPF (Fig 1) to find its (input to output) TF, Input- and Output-Referred Noise (IRN and ORN, respectively), and the NF. For the TF analysis, we make use of a similar adjoint network-based analysis method with a state-space description as in [20], extend it to include noise behavior, and apply it to the circuit in Fig 1.

The generalized circuit (Fig 1) has eight degrees of freedom (design parameters): the sampling capacitor (C_s), each history capacitance ($C_{h,x} = C_h$, $x \in [1, 2 \dots N]$), the number of history capacitors (N), the clock frequency ($f_s = 1/T_s$),³ the on-time of a single clock sub-phase [$\tau_{on} = 1/(f_s(N+2))$], the source and switch impedances (R_s and R_{sw} , respectively), and our feedback factor (α_f). Every clock period of T_s starts with sampling $v_{in}(t)$ through its finite source-impedance R_s , followed by charge sharing of sampling capacitor C_s with the first history capacitor $C_{h,1}$, sharing C_s with $C_{h,2}$ etc. until C_s shares with $C_{h,N}$. What happens during the last clock phase, ϕ_{N+1} , depends on the choice of α_f :

- 1) ($\alpha_f \approx 0$) **Reset** the sampling capacitor by a reset switch to ground, as in [1] and [2].

- 2) ($\alpha_f = -1$) **Invert** (flip) the sampling capacitor between clock periods, as shown in [3] and [21].
- 3) ($\alpha_f = 1$) **Hold**. Do nothing and leave the sampling capacitor unchanged before the next sample. Bozorg et al. [9] proposes a bandpass filter around a charge-sharing filter topology, where the sampling capacitor is neither inverted nor reset.

We impose two assumptions on the network parameters. First, we assume that the switch resistance is sufficiently small, such that the voltages on C_s and C_h settle to a stable voltage within τ_{on} (thus $R_{sw}(C_s||C_h) \ll \tau_{on}$). This allows us to use charge-balance equations to model interactions between the sampling and history capacitors and allows for simplifications regarding sampled noise later. Second, we assume all clock signals are non-overlapping and have near-instantaneous rising and falling edges. This reduces the complexity of the calculations, as effects associated with finite rise-and-fall times can be omitted. Additionally, this will allow for simplifications when introducing interleaving/pipelining in Section II-E.5.

A. Deriving the Adjoint Network of the Generalized Filter

We convert the LPTV circuit from Fig 1 into an adjoint network and use reciprocity to derive the equivalent TF of the original network. The equivalent TF, $H_{eq}(f)$, is calculated by Fourier transforming the impulse response [$h_{eq}(t)$] of the adjoint network [22]. It should be noted that $H_{eq}(f)$ is the *equivalent* LTI transfer function, which when sampled at the output with periodicity T_s , gives the same samples as the original network (Fig 1) [22].

We now derive the adjoint network of Fig 1. Respecting the port impedances, the input voltage source is replaced with a short, while source impedance R_s remains. The output voltage is replaced by a current source which injects a delta-dirac current $i_{in}(t) = \delta(t)$. All passive components remain unaltered. The timing of the clocks operating the switches is reversed [22]. The resulting adjoint network is displayed in Fig 3.

By observing the resultant current $i_{out}(t)$ flowing through R_s , the location where in the original network $v_{in}(t)$ was injected, we find the impulse response of the adjoint network $h_{eq}(t)$. Using the periodic nature of the LPTV circuit and the fact that the input impulse only occurs at $t = 0$ and never after, a prototype recursive expression for the impulse response can be written as [20]:

$$i_{out}(t) = h_{eq}(t) = p(t) + \lambda h_{eq}(t - T_s) \quad (1)$$

in which $p(t)$ is the output current $i_{out}(t)$ during the first cycle of the clock from $t = 0^+$ until $t = T_s^+$, and λ describes how the impulse response is scaled from one clock period to the next.

We will use a Signal Flow Graph (SFG) to formulate a Discrete-Time State-Space (DTSS) description [20]. This offers two distinct advantages. First, the eigenvalues of the DTSS description yield information about the repetition of the output current and provide λ for (1). Second, the state vector $\mathbf{x}[kT_s^+]$ of the DTSS yields the voltages on *all* the capacitors in the network (v_{C_s} and $v_{C_{h,1 \dots N}}$). We will use these capacitor

³For the ‘invert’ implementation, $\alpha_f = -1$, output samples are produced at f_s rate, but two periods are needed to capture the inversion fully, see the timing waveform in Fig 1.

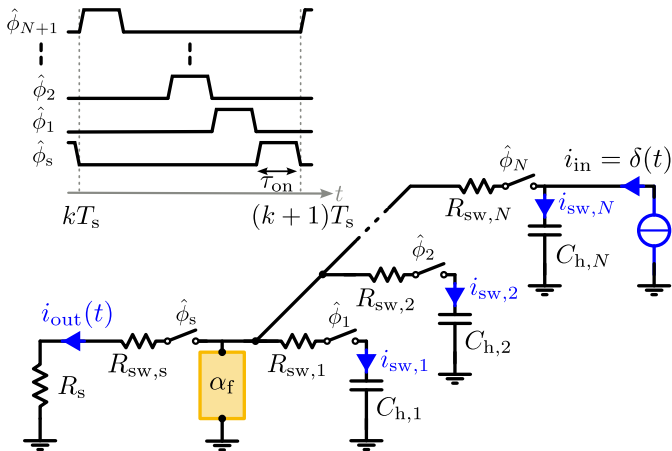


Fig. 3. Adjoint network of the generalized circuit from Fig. 1. Note that the switch timings in the α_f box need to be replaced by their time-reversed variants ($\hat{\phi}_{N+1}$), if present.

voltages to calculate $p(t)$ in (1), and later in Section II-E to find the currents flowing through switch on-resistances of the switches, which will be used to calculate noise contributions of individual components.

B. Formulating a Discrete Time State-Space Description Using a Signal Flow Graph

We will now describe how the state vector $\mathbf{x}[kT_s^+]$ is affected by input signals and how it evolves from one clock period ($t = kT_s^+$) to the next ($t = (k+1)T_s^+$). The DTSS is given by:

$$\mathbf{x}[(k+1)T_s^+] = \mathbf{A}\mathbf{x}[kT_s^+] + \mathbf{B}\delta[0]. \quad (3)$$

Here, \mathbf{A} is the $N+1$ row by $N+1$ column state matrix (sometimes referred to as evolution matrix), and \mathbf{B} the input vector of length $N+1$. Next, we construct \mathbf{B} and \mathbf{A} .

The \mathbf{B} vector computes $\mathbf{x}[0^+]$ from the delta impulse that has been injected at the output node on $t = 0$. As all switches are open, only the last history capacitor, $C_{h,N}$ is charged. This results in the \mathbf{B} vector shown in (2), as shown at the bottom of the page, located in the footnote of this page.⁴

To construct the \mathbf{A} matrix, we realize that each element of the \mathbf{A} matrix in the DTSS description represents the compounded effect of all the manipulations of the network states (capacitor voltages) that occur during a full clock period

⁴The '1' in \mathbf{B} stands for 1 Coulomb. Thus, $1/C_h$ is a voltage. From here, we no longer explicitly write $\mathbf{B}\delta[0]$, but just \mathbf{B} .

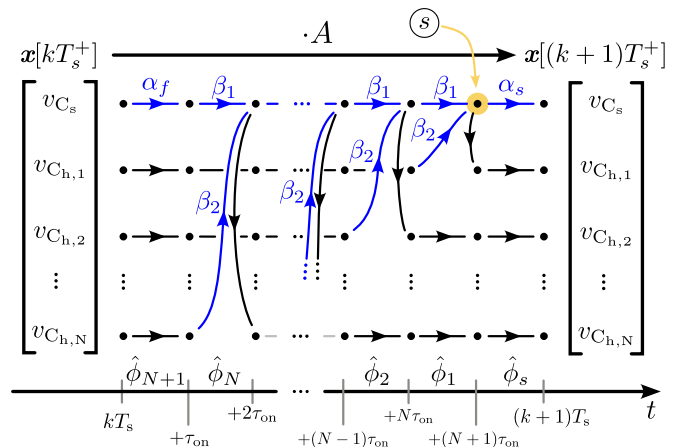


Fig. 4. Discrete-time signal flow graph of the adjoint network from Fig 3 from $t = 0$ till $t = T_s$. The thicker dots represent capacitor voltages as clock sub-phases change. (Black) arrows without quantities are unity. The circled s represents voltage on C_s just before the sample switch closes.

T_s , from a single capacitor voltage to all other capacitor voltages. To track these changes in capacitor voltages during the sub-phases of the clocks (when the sampling and charge-sharing switches are active), we will first construct an SFG as shown in Fig 4. In the SFG, the quantity associated with the transition arrow (β_1 , β_2 , α_f , α_s or '1') is multiplied by the capacitor voltage at the start of the sub-phase (thick dot at the base of an arrow) to find the network state at the next clock sub-phase (thick dot at the point of an arrow). By changing the value of α_f , the SFG in Fig 4 can represent all three topologies of Fig 1:

- Setting $\alpha_f = 1$ represents a topology in which C_s is neither reset nor inverted between clock cycles. Thus v_{C_s} holds its state from $t = kT_s^+$ to $t = kT_s^+ + \tau_{on}$, with $k \in [0, 1, \dots]$.
- Setting $\alpha_f \approx 0$ represents a topology in which C_s is reset between clock cycles. Thus v_{C_s} is reset to 0 V.
- Setting $\alpha_f = -1$ represents a topology in which C_s is inverted between clock cycles.⁵ Thus v_{C_s} is inverted to $-v_{C_s}$.

The arrows in the SFG with an associated (β_1 , β_2) quantity represent the elementary charge-sharing equations between C_s and $C_{h,x}$, and the discharge of C_s through the source

⁵This 'inversion' of C_s could be implemented by appropriately sharing the sampling capacitor in a differential implementation [23], or by using four switches surrounding C_s [21]. If the nodes connected to C_s are sufficiently low-ohmic, the signal-flow graph presented in Fig. 4. remains valid.

$$\mathbf{A} = \begin{bmatrix} a_{1,1} & \dots & a_{1,N+1} \\ \vdots & \ddots & \vdots \\ a_{N+1,1} & \dots & a_{N+1,N+1} \end{bmatrix} = \begin{bmatrix} \alpha_f \alpha_s \beta_1^N & \alpha_s \beta_2 \beta_1^0 & \alpha_s \beta_2 \beta_1^1 & \alpha_s \beta_2 \beta_1^2 & \dots & \alpha_s \beta_2 \beta_1^{N-1} \\ \alpha_f \beta_1^{N-0} & \beta_2 & \beta_2 \beta_1^1 & \beta_2 \beta_1^2 & \dots & \beta_2 \beta_1^{N-1} \\ \alpha_f \beta_1^{N-1} & 0 & \beta_2 & \beta_2 \beta_1^1 & \dots & \beta_2 \beta_1^{N-2} \\ \alpha_f \beta_1^{N-2} & 0 & 0 & \beta_2 & \dots & \beta_2 \beta_1^{N-3} \\ \vdots & \vdots & \vdots & \vdots & \ddots & \vdots \\ \alpha_f \beta_1^1 & 0 & 0 & 0 & \dots & \beta_2 \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} 0 \\ 0 \\ \vdots \\ 1/C_h \end{bmatrix} \quad (2)$$

impedance (α_s). They are:

$$[\beta_1 \ \beta_2] = \left[\frac{C_s}{C_s + C_h} \quad \frac{C_h}{C_s + C_h} \right] \quad (4a)$$

$$\alpha_s = \exp\left(\frac{-\tau_{on}}{(R_s + R_{sw})C_s}\right). \quad (4b)$$

Now that we have an SFG that captures all three topologies from Fig 1, we will use it to construct a generalized \mathbf{A} matrix. The \mathbf{A} matrix is constructed by tracing all combinations of paths from $\mathbf{x}[kT_s^+]$ to $\mathbf{x}[(k+1)T_s^+]$ in the SFG, i.e. from the left of Fig 4 to the right. As an example, let us find $a_{1,1}$, which describes how v_{C_s} evolves from $t = kT_s^+$ to $t = (k+1)T_s^+$. Starting on the left in Fig 4, at $v_{C_s}[kT_s^+]$, we follow the path that leads to $v_{C_s}[(k+1)T_s^+]$ on the right of the figure.⁶ In this case, the capacitor voltage is first affected by α_f , followed by N charge-sharing actions with history capacitors, and finally a partial discharge of C_s in the source described by α_s . This yields the compounded effects (by multiplication) captured in $a_{1,1}$ as $\alpha_f \alpha_s \beta_1^N$. Repeating the same procedure for all network states, we find the generalized \mathbf{A} matrix found in (2). Note that this is the last step in the derivation where N is a degree of freedom; once the state-space description is determined, N is fixed, as it determines the size of the matrix. Generating the state-space description using the generalized description of (2) is a straightforward procedure, and all consecutive steps from this point on can be fully automated for both symbolic and numeric approaches.

C. Eigendecomposition of the \mathbf{A} -Matrix

Similar to the case in [20], the \mathbf{A} -matrix in (2) is not diagonal due to charge sharing from the sampling capacitor to all the history capacitors. This complicates using our DTSS in solving the recursive equation in (1), as we cannot directly use \mathbf{A} for λ , i.e., to calculate the scaling of the impulse response from one T_s^+ to the next. To solve this, we follow the same two-step procedure outlined in [20]: First, we decompose the \mathbf{A} -matrix into its eigenvalue matrix (\mathbf{D}) and eigenvectors (\mathbf{V}). Second, we decompose the recursive equation of the impulse response (1) into multiple responses, in which the scaling from one clock period to the next (through λ_i) is described by the eigenvalues as found in the first step.

Let us perform eigendecomposition, yielding $\mathbf{A} = \mathbf{VDV}^{-1}$. The state vector $\mathbf{x}[kT_s^+]$ at any multiple of the clock k , can be found as:

$$\mathbf{x}[kT_s^+] = \mathbf{A}^k \cdot \mathbf{B} = (\mathbf{VDV}^{-1})^k \cdot \mathbf{B} = \mathbf{VD}^k \mathbf{V}^{-1} \cdot \mathbf{B}. \quad (5)$$

Written in this form, it becomes evident that the recursion of the network can be captured by applying the proper exponent to the eigenvalue matrix (\mathbf{D}^k). As \mathbf{D} is a diagonal matrix, \mathbf{D}^k is found by applying the exponent to the individual eigenvalues (λ_i) on the diagonal

elements $d_{i,i}$:

$$\mathbf{D}^k = \begin{bmatrix} \lambda_1^k & 0 & \dots & 0 \\ 0 & \lambda_2^k & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \lambda_{N+1}^k \end{bmatrix}. \quad (6)$$

The eigenvalues of the network represent the (filter) poles of the network directly. We will use this property when constructing pole-zero plots in Section III-A to illustrate how filter selectivity is affected by network parameters.

To use the eigenvalues found in (6) to solve (1), we can decompose $h_{eq}(t)$ into multiple responses as:

$$h_{eq}(t) = \sum_{i=1}^{i=N+1} h_{eq,i}(t) \quad (7a)$$

$$h_{eq,i}(t) = p_i(t) + \lambda_i h_{eq,i}(t - T_s). \quad (7b)$$

Each $h_{eq,i}(t)$ response is a recursive expression with one eigenvalue of the network.

D. Impulse Response and Transfer Function

Now that we have captured the recursion of (7) through the eigenvalues (λ_i) obtained from the DTSS, we need to construct an expression for $p_i(t)$ to finish (7b). We can interpret $p_i(t)$ as a contribution to $i_{out}(t)$ in the adjoint network (Fig 3), during the first clock-period from $t = 0^+$ until $t = T_s^+$. We will obtain $p_i(t)$ from the state vector $\mathbf{x}[kT_s^+]$ next.

The state vector $\mathbf{x}[kT_s^+]$ represents the capacitor voltages at exact integer multiples of the clock only and not during the sub-phases during which switches are active. Inspection of Fig 3 shows that during $\hat{\phi}_s$, current flows through R_s . Thus, it is not possible to use the state vector $\mathbf{x}[kT_s^+]$ directly to compute $i_{out}(t)$. Instead, we re-use the SFG of Fig 4 to find the voltage across C_s , as the sample switch closes at $t = kT_s + (N+1)\tau_{on}$. This follows the same procedure as used to construct \mathbf{A} by tracing all the paths from the state vector $\mathbf{x}[kT_s^+]$ on the left to node marked by ⑤ in Fig 4. We find the voltage across C_s before the discharge starts ($v_{C_s,d}[kT_s^+]$) to be:

$$\begin{aligned} v_{C_s,d}[kT_s^+] &= v_{C_s}[kT_s + (N+1)\tau_{on}] \\ &= [\alpha_f \beta_1^N \ \beta_2 \beta_1^0 \ \beta_2 \beta_1^1 \ \dots \ \beta_2 \beta_1^{N-1}] \mathbf{x}[kT_s^+]. \end{aligned} \quad (8)$$

We will re-write (8) such that the terms are grouped for each individual eigenvalue λ_i . This regrouping collects the eigenvalues (λ_i) with their accompanying contributions to $p_i(t)$. We denote the re-grouped terms as v_i :

$$v_{C_s,d}[kT_s^+] = \sum_{i=1}^{i=N+1} v_{C_s,d,i}[kT_s^+] = \sum_{i=1}^{i=N+1} \lambda_i^k v_i[kT_s^+] \quad (9)$$

where $v_i[kT_s^+]$ are a function of \mathbf{V} , \mathbf{B} , α_f , β_1 , and β_2 given by (5) and (8).

We are calculating partial contributions to $i_{out}(t)$ during the first clock period [$p_i(t)$], thus $k = 0$. This simplifies (9), as $\lambda_i^0 = 1$, and $v_{C_s,d,i}[0] = v_i[0]$. Using this (decomposed contribution to the) voltage across R_s' just after the sample

⁶In our network, we find that there is a single path leading from an element of the starting state ($\mathbf{x}[kT_s^+]$) to an element of the next state ($\mathbf{x}[(k+1)T_s^+]$). If there had been multiple, each path should have been followed individually and their contributions summed.

switch closed, we find the continuous time $i_{\text{out}}(t)$ to be an exponential discharge of C_s through R'_s during $\hat{\phi}_s$ as:

$$p_i(t) = \frac{v_i[0]}{R'_s} \left(e^{\frac{-t-(N+1)\tau_{\text{on}}}{R'_s C_s}} u(t - (N+1)\tau_{\text{on}}) - \alpha_s e^{\frac{-t-(N+2)\tau_{\text{on}}}{R'_s C_s}} u(t - (N+2)\tau_{\text{on}}) \right) \quad (10)$$

where $u(t)$ denotes the unit-step function used to start and stop the discharge of C_s through R'_s . We now transform $p_i(t)$ into the frequency domain. Using the addition, amplitude scaling, and time-shift properties of Fourier transforms, we find:

$$P_i(f) = \frac{v_i[0]}{R'_s} \left(\frac{R'_s C_s}{1 + j2\pi f R'_s C_s} e^{-j2\pi f (N+1)\tau_{\text{on}}} - \alpha_s \frac{R'_s C_s}{1 + j2\pi f R'_s C_s} e^{-j2\pi f (N+2)\tau_{\text{on}}} \right). \quad (11)$$

Now that we have an expression of the Fourier transform first period of the clock [currently decomposed in $P_i(f)$], and the eigenvalues (λ_i found in \mathbf{D}) describing the repetition, we can construct the transfer function by calculating the Fourier transform of (7b), substituting the result in (7a), and using the results of (11) and (6) yielding:

$$H_{\text{eq}}(f) = \sum_{i=1}^{i=N+1} \frac{P_i(f)}{1 - \lambda_i e^{-j2\pi f T_s}}. \quad (12)$$

We will show agreement between simulation and (12) in Section II-F. The zeros of the TF can be obtained from (12) by taking the summation over the fractions, and equating the resulting numerator to zero.

E. Noise Analysis

In this section, we will extend the model to calculate ORN and refer it back to IRN. To do so, we will calculate the contributions to the (total) ORN from all noise sources in the generalized circuit including the source resistance. First, we calculate the noise contributions from the charge-share switches $R_{\text{sw},q}$, where index q refers to the charge-share switch connected to the q^{th} history capacitor ($q \in \{1, 2, \dots, N\}$). Second, we will evaluate the noise contributions associated with the implementation of the reset action when $\alpha_f \approx 0$. Last, we account for the noise contributed by R_s and the sample switch resistance ($R_{\text{sw},s}$) during ϕ_s . After finding the contributions, we will combine them to find the ORN, use $H_{\text{eq}}(f)$ from (12) to find IRN, calculate NF, and address considerations regarding pipelining/interleaving to reduce NF.

1) *Noise Density Contribution From Charge-Sharing Switches:* The on-resistance of the charge-sharing switches is dimensioned such that the capacitor voltage has settled in less than τ_{on} . Therefore, a simplification proposed by [24] is valid. In this simplification, first the noise is sampled onto the series combination of the sample and history capacitor $C_{\text{eff}} = (C_s C_h)/(C_s + C_h)$, which gives the single-sided switched-capacitor sampled density of $S_{n,\text{sc}} = (2k_b T)/(f_s C_{\text{eff}})$ from

$f = 0$ to $f = f_s/2$. This sampled noise is subsequently transferred to the output as:

$$S_{n,\text{sw},q}(f) = S_{n,\text{sc}} |H_{\text{eq},\text{Rsw},q}(f)|^2. \quad (13)$$

In this, $H_{\text{eq},\text{Rsw},q}(f)$ is the transfer function from the current flowing through charge-share switch q to the network output, which we will now calculate.

After the application of the Dirac (delta) impulse current in the adjoint network (Fig 3), current will flow through all branches of the network over the course of a clock period T_s . In Section II-D, we observed the resulting current flowing through R_s in order to derive the transfer function from $v_{\text{in}}(t)$ to $v_{\text{out}}[kT_s^+]$ of the original network (Fig 1). Now, to find the TFs from all charge sharing switches to the sampled output $v_{\text{out}}[kT_s^+]$, we observe the current flowing through the respective switch impedances: $R_{\text{sw},q}$. We use the same approach as taken for calculating (12), and note that the eigenvalues of the network are system responses, and do *not* change for different combinations of input/output. Thus, the SFG (Fig 4), \mathbf{A} -matrix, \mathbf{B} -vector and resulting eigenvalues λ_i remain valid, and are re-used.

To calculate the TF from the noise sources to the output, we follow the same procedure described in Section II-D, following (8) through (12). Similar to the calculation of (8), we calculate the voltage across charge-sharing switch $R_{\text{sw},q}$ just before it closes. Using the state vector $\mathbf{x}[kT_s^+]$ and the SFG (Fig 4) we find:

$$\begin{aligned} v_{\text{Rsw},q}[kT_s^+ + (N+1-q)\tau_{\text{on}}] &= -v_{\text{Ch},q}[kT_s^+] \\ &+ \begin{bmatrix} \alpha_f \beta_1^{N-q} \\ \beta_2 u(0-q) \beta_1^{\frac{|0-q|+0-q}{2}} \\ \beta_2 u(1-q) \beta_1^{\frac{|1-q|1-q}{2}} \\ \vdots \\ \beta_2 u((N-3)-q) \beta_1^{\frac{|(N-3)-q|+(N-3)-q}{2}} \end{bmatrix}^T \mathbf{x}[kT_s^+] \end{aligned} \quad (14)$$

where $v_{\text{Ch},q}[kT_s^+]$ is the voltage of the history capacitor connected to switch q ; the q^{th} entry of the state vector found in (5), T denotes the matrix transpose, and $u(n)$ is the Heaviside step-function defined as:

$$u(n) = \begin{cases} 0, & n < 0 \\ 1, & n \geq 0. \end{cases} \quad (15)$$

Following the steps of (9) through (11), we find $P_{i,\text{Rsw},q}(f)$:

$$P_{i,\text{Rsw},q}(f) = \frac{v_{i,\text{Rsw},q}[0]}{R_{\text{sw}}} \frac{R_{\text{sw}} C_{\text{eff}}}{1 + j2\pi f R_{\text{sw}} C_{\text{eff}}} \cdot \left(e^{j2\pi f (N+1-q)\tau_{\text{on}}} - \alpha_d e^{j2\pi f (N+2-q)\tau_{\text{on}}} \right) \quad (16)$$

with $\alpha_d = e^{\frac{-\tau_{\text{on}}}{R_{\text{sw}} C_{\text{eff}}}}$, and $v_{i,\text{Rsw},q}[0]$ obtained by re-grouping terms as shown in (9). The summation outlined in (12) can be carried out with (16) and the λ_i system responses from (6) to find the TF $H_{\text{eq},\text{Rsw},q}(f)$. This TF is used to solve (13), yielding the output noise contributions $S_{n,\text{sw},q}(f)$ of all $R_{\text{sw},q}$. We verify the analytical results with simulation in Section II-F.

2) *Noise Density Contribution From the Reset Switch:* The reset switch is only present for the ‘reset’ ($\alpha_f \approx 0$) topology.⁷ Our prior assumption of $R_{\text{sw},\text{Rrst}}C_s \ll \tau_{\text{on}}$ also applies here. Thus, we use the same simplification as Section II-E.1. We note that the reset occurs right after the start of a new period kT_s^+ , thus (14) simplifies to $v_{\text{Rrst}}[kT_s^+] = [1 \ 0 \ \dots \ 0]\mathbf{x}[kT_s^+]$. Following the steps of (9) through (11), we find:

$$P_{i,\text{Rrst}}(f) = \frac{v_{i,\text{Rrst}}[0]}{R_{\text{sw}}} \frac{R_{\text{sw}}C_s}{1 + j2\pi f R_{\text{sw}}C_s} \cdot \left(e^{j2\pi f \tau_{\text{on}}} - \alpha_r e^{j2\pi f 2\tau_{\text{on}}} \right) \quad (17)$$

with $\alpha_r = e^{-\frac{\tau_{\text{on}}}{R_{\text{sw}}C_s}}$. We then find $H_{\text{eq},\text{Rrst}}(f)$ by substituting (17) into (12). The output noise contribution associated with the implementation of the reset switch is then found as follows:

$$S_{n,\text{Rrst},\text{out}}(f) = S_{n,\text{reset}} |H_{\text{eq},\text{Rrst}}(f)|^2 \quad (18)$$

where $S_{n,\text{reset}} = 2k_b T / (f_s C_s)$, following the same reasoning as in Section II-E.1.

3) *Noise Density Contribution of the Input Sampler:* We note that in our analysis in Section II-D, we did *not* impose restrictions on the time-constant of the input sampler $R'_s C_s$, ensuring that our analysis remains general. However, this means that we do not yet know in which regime the sampler operates. The input sampling could occur in Sample and Hold regime [24], [25] where $R'_s C_s \ll \tau_{\text{on}}$, Passive-Mixer regime [24], [25] where $R'_s C_s \gg \tau_{\text{on}}$ or somewhere in-between $R'_s C_s \approx \tau_{\text{on}}$ [25]. As such, we cannot use the same simplification as when calculating $S_{n,\text{sw},q}(f)$ in (13). Instead, we will calculate the noise contribution of the combination of the source resistance R_s and input sampling switch on-resistance $R_{\text{sw},s}$ by evaluating how the Double-Sided (D-S) noise Power Spectral Density (PSD) from R'_s , $S_{n,R_s'} = 2k_b TR'_s$, is filtered and folded to baseband via Harmonic Transfer Functions (HTFs). To do so, we first use $H_{\text{eq}}(f)$ from (12), which describes the TF from $v_{\text{in}}(t)$ to the sampled output $v_{\text{out}}[kT_s^+]$, capturing how $S_{n,R_s'}$ is filtered before frequency translation. The product of $H_{\text{eq}}(f)$ and $S_{n,R_s'}$ represents the filtered PSD before folding, as shown in Fig 5a. According to [25], $H_{\text{eq}}(f)$ consists of a summation of harmonic transfer functions $H_{\text{eq}}(f) = \sum_{l=-\infty}^{\infty} H_l(f)$. Consequently, the filtered PSD before folding already consists of the required HTFs once we account for frequency translation from (multiples of) the clock frequency, see Fig 5a. Then, the ORN contribution originating from the sampling of $v_{\text{in}}(t)$ through R'_s onto C_s , is found by summation of the frequency-translated and shaped noise PSD as:

$$S_{n,\text{samp}}(f) = \sum_{l=-\infty}^{\infty} |H_{\text{eq}}(f - lf_s)|^2 (2k_b TR'_s) \quad (19)$$

for $-f_s/2 < f < f_s/2$. $H_{\text{eq}}(f)$ is the same as obtained during (1) - (12). In (19), $S_{n,\text{samp}}(f)$ contains the noise from both the sample switch and R_s . Absorbing the noise contribution of R_s into the circuit noise calculation implicitly

⁷We do not prescribe how an implementation of $\alpha_f = -1$ could be made, and therefore do not account for its associated noise here.

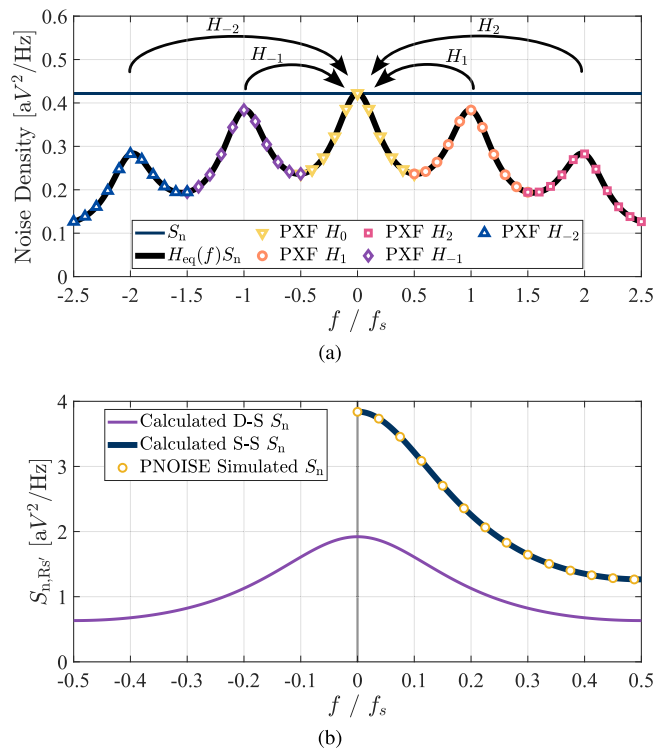


Fig. 5. (a) Illustration of the noise density calculation using $H_{\text{eq}}(f)$ from (12). This illustration shows the effect of the sampling of v_{in} through R_s for an implementation with $\alpha_f = 1$, $N = 0$, $C_s = 1.5\text{pF}$, $f_s = 2.5\text{GHz}$, $R_s = 50\Omega$, and $R_{\text{sw}} = 1\Omega$. 5 Nyquist zones are shown. Additionally, we show agreement with harmonic transfer functions obtained with Spectre PXF simulations (markers). The harmonic transfer functions have been normalized to $S_n(0)$. (b) Noise density of the sampler calculated using (19) as Double-Sided (D-S) and Single-Sided (S-S) PSD. The summation of (19) is carried out over 50 harmonics and verified versus Spectre simulations (circles).

samples its noise contribution onto C_s , and propagates it to the output. This will simplify the NF calculation in Section II-E.5. Fig 5b shows agreement between a Spectre (Sampled) noise simulation and the result obtained from (19).

4) *Total Input/Output Referred Noise:* After computing (13), (18), and (19), we can sum their powers to find the ORN and IRN:

$$S_{n,\text{kernel,ORN}}(f) = S_{n,\text{samp}}(f) + S_{n,\text{Rrst}}(f) + \sum_{q=1}^N S_{n,\text{sw},q}(f) \quad (20a)$$

$$S_{n,\text{kernel,IRN}}(f) = \frac{S_{n,\text{kernel,ORN}}(f)}{|H_{\text{eq}}(f)|^2} \quad (20b)$$

for $f = 0$ till $f = f_s/2$ and $H_{\text{eq}}(f)$ is the TF found from (1) - (12).

5) *Pipelining, Interleaving, and Conversion to NF:* In the derived model, we assumed that charge sharing between the sampling and history capacitors settles to a high degree within one switch on-time τ_{on} , thus $\tau_{\text{on}} \gg R_{\text{sw}}C_{\text{eff}}$. As pointed out in [1], [9], this could become challenging when τ_{on} becomes small to accommodate a high number of history capacitors N , especially at high clock frequencies f_s . The work in [1] proposes a pipelining solution using one sampling capacitor for each clock sub-phase T_s/τ_{on} . It similarly is also possible

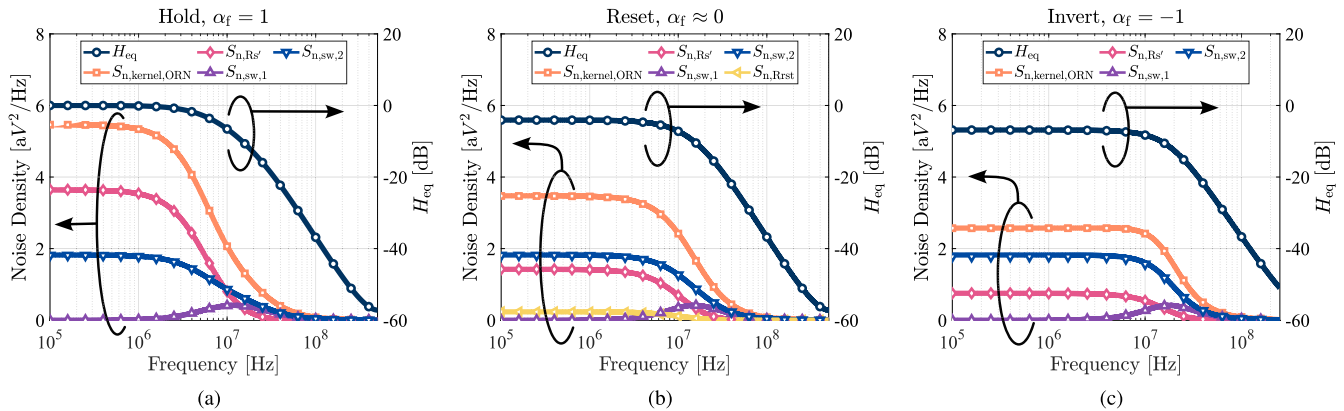


Fig. 6. Comparison between Spectre X simulations (data markers) and (13), (18), (19), (20a), (12) (solid lines), for (a) $\alpha_f = 1$, (b) $\alpha_f \approx 0$, and (c) $\alpha_f = -1$. The remaining network parameters are: $C_s = 5\text{pF}$, $C_h = 50\text{pF}$, $N = 2$, $R_s = 50\Omega$, $f_s = 1\text{GHz}$, and $R_{sw} = 1\Omega$ (all switches).

to time interleave several kernels (instances of Fig 1 consisting of C_s and all C_h) together.

The result of (20a) can be expanded to account for the noise improvement for a time-interleaved or pipelined structure. Provided that there is no mismatch between the kernels, no crosstalk between the kernels, and the clocks are non-overlapping, the noise performance is found by realizing that with M kernels, we add M^2 times correlated signal power, and M times uncorrelated noise power. This yields a net reduction in PSD (in V^2/Hz) of M [26]. As we have $N + 2$ available clock phases, this is the maximal degree of interleaving available, granting a noise PSD reduction of $N + 2$:

$$S_{n,\text{interleaved,IRN}} = \frac{S_{n,\text{kernel,IRN}}}{M} = \frac{S_{n,\text{kernel,IRN}}}{N + 2}. \quad (21)$$

$S_{n,\text{interleaved,IRN}}(f)$ is the total input-referred noise PSD including noise from R_s [see (19) and (20)], so NF can now be calculated by dividing the $S_{n,\text{interleaved,IRN}}(f)$ with only the source noise $S_{n,R_s}(f)$ (see e.g., [27, p. 50]), as:

$$\text{NF}(f) = 10 \log_{10} \left(\frac{S_{n,\text{interleaved,IRN}}(f)}{S_{n,R_s}(f)} \right). \quad (22)$$

F. Model Verification

Let us verify the analysis by computing (12), (20a) and comparing the calculation result to simulations with Spectre X. We do this for three PSC-IIR LPFs, one for each $\alpha_f \in \{1, 0, -1\}$. The results are shown in Fig 6, where the simulated markers and calculated (solid) lines overlap nearly perfectly, indicating excellent agreement between the simulation and the derived analytical model.

III. DESIGN SPACE EXPLORATION

In this section, we will use the model derived in Section II to provide insights into the trade-offs present in the design space of the PSC-IIR LPF represented in Fig 1. In Appendix A, we describe a brief implementation procedure which uses the results presented in this Section to design a filter with the topology presented in Fig 1 for a certain NF and selectivity.

We use a normalized design parameter $|Z_{\text{eq}}|/R_s$. Z_{eq} is the *equivalent switched-capacitor impedance* of the periodical

charge and subsequent discharge of C_s with the input or C_h capacitors, while accounting for interleaving/pipelining.⁸ Using $|Z_{\text{eq}}|/R_s$, we can evaluate the noise and selectivity characteristics irrespective of f_s , while simultaneously assuming noise minimization through interleaving/pipelining, and have the result normalized to R_s . $|Z_{\text{eq}}|/R_s$ is defined as:

$$\frac{|Z_{\text{eq}}|}{R_s} = \frac{1}{(N + 2)f_s C_s R_s}. \quad (23)$$

We will show that the ratio $|Z_{\text{eq}}|/R_s$ plays a crucial role in determining both the noise and selectivity of the circuit and that $|Z_{\text{eq}}|/R_s$ directly trades one for the other. We will first discuss the effect of $|Z_{\text{eq}}|/R_s$ on selectivity and noise individually, then we will explore the trade-off between them.

A. Selectivity Considerations

The Selectivity of the filter is mainly determined by $|Z_{\text{eq}}|/R_s$, the topology (denoted with α_f), and the number of history capacitors N . Because a complex-pole filter requires $N \geq 2$ and the closed-form expressions become long and difficult to interpret for $N > 2$, we will first treat an example with $N = 2$. In Section III-E, we will consider the effects of increasing N . We will look at absolute and normalized transfer functions (Fig 7), a Pole-Zero plot (Fig 8), and capture the selectivity as a single number to be used in Section III-D for evaluating selectivity vs NF.

To express the selectivity of the filter as a single number irrespective of its bandwidth, we will quantify the filter selectivity as the (Number of) *Normalized Transition Bandwidths* until A_{stop} (stopband) attenuation is reached (see diamond-shaped markers in Fig 7):

$$\text{NTBW}_{A_{\text{stop}}} = \frac{f_{A_{\text{stop}}}}{f_{-3\text{dB}}} - 1. \quad (24)$$

⁸The use of equivalent impedance Z_{eq} bears similarity to [1], [21], where key design aspects are captured in a SC resistor R_{eq} . The SC resistor approximation only holds if the nodes to which the sampler capacitor is connected may be approximated as a stable voltage. We explicitly will not do so, as such an assumption severely restricts the size of the sampling capacitor in the presence of a source impedance R_s , and the ratio $C_s:C_h$. Seen from the input of the circuit, Z_{eq} may appear capacitive if $R_s C_s \approx \tau_{\text{on}}$.

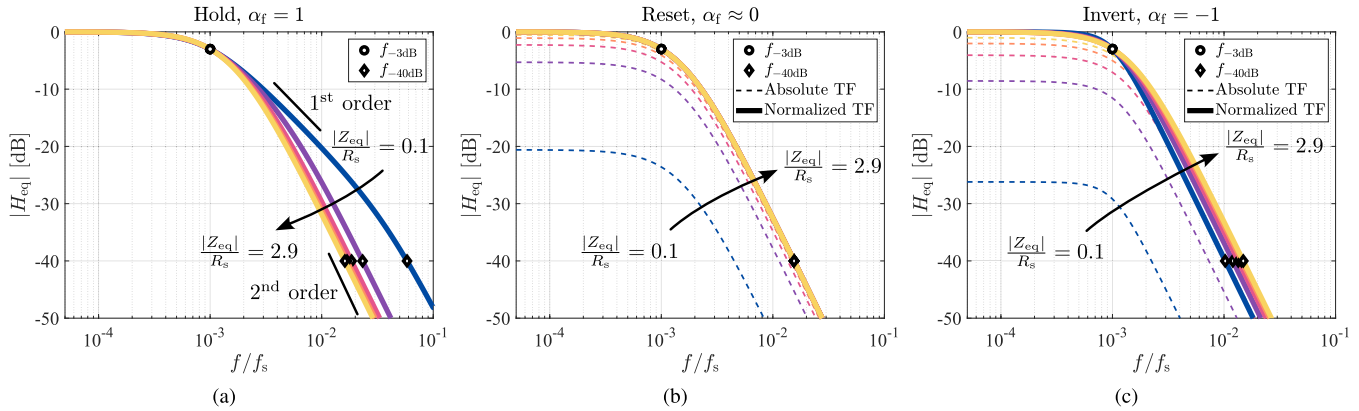


Fig. 7. Computed filter responses from (12) to illustrate how the transition band is affected by changing $|Z_{\text{eq}}|/R_s$, for (a) $\alpha_f = 1$, (b) $\alpha_f \approx 0$, and (c) $\alpha_f = -1$. The different lines within a plot represent different $|Z_{\text{eq}}|/R_s$, which run from 0.1 until 2.9 in steps of 0.7. To aid in comparing the normalized transition bandwidth (NTBW) in the presence of variable in-band attenuation, each transfer (dashed lines) has been normalized (solid lines) by its DC magnitude $|H_{\text{eq}}(0)|$. Note that in (a), for $\alpha_f = 1$, $H_{\text{eq}}(0) = 0\text{dB}$ irrespective of $|Z_{\text{eq}}|/R_s$. For all implementations $R_{\text{sw}} = 0.02R_s$ and $N = 2$, while C_h is adjusted to ensure a constant bandwidth of $f_{-3\text{dB}} = 0.001f_s$.

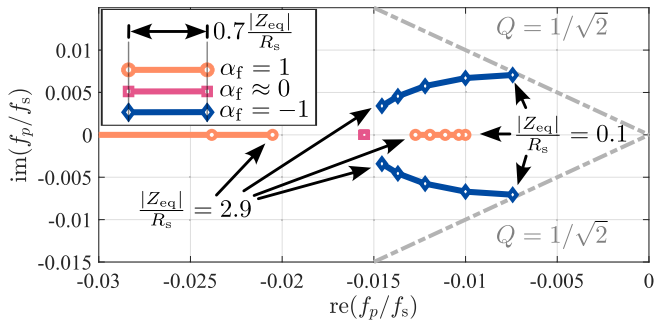


Fig. 8. Pole-Zero plot of the generalized filter implementations. $|Z_{\text{eq}}|/R_s$ is swept from 0.1 to 2.9 in steps of 0.7, and this coincides with the marker spacing. For all implementations, the filter bandwidth is kept equal at $0.01f_s$ by adjusting C_h . In the case of $\alpha_f \approx 0$, all poles stay at the same frequency and are unaffected by $|Z_{\text{eq}}|/R_s$. For $\alpha_f = 1$, the second pole continues shifting to higher frequencies after $|Z_{\text{eq}}|/R_s = 1.6$, at the left of the figure.

Here, A_{stop} is the desired stopband attenuation relative to the pass band, $f_{A_{\text{stop}}}$ the frequency at which A_{stop} is attained, and $f_{-3\text{dB}}$ the -3dB bandwidth. A *lower* value of $\text{NTBW}_{A_{\text{stop}}}$ means that the stopband attenuation is reached in a *narrower* transition band and is therefore indicative of a *more selective* filter. This section will use $A_{\text{stop}} = -40\text{dB}$, representing a practical filter stopband attenuation.

The selectivity of the filter is directly related to the pole locations, which we will find from the eigenvalue matrix \mathbf{D} in (6). The pole locations primarily change depending on α_f , C_h , and $|Z_{\text{eq}}|/R_s$. For the filter derived in Section II with $N = 2$, we find that the two poles are located (in the z -domain) at:

$$\lambda_{1,2} \approx \beta_2 \left(1 \pm \beta_1 \sqrt{\alpha_f \alpha_s (1 + C_s/C_h)} \right). \quad (25)$$

These poles can be approximated in the s -domain by using the bilinear transform:

$$f_{p,i} \approx \frac{2}{T_s} \frac{\lambda_i - 1}{\lambda_i + 1}. \quad (26)$$

The pole locations are used to construct the Pole-Zero plot in Fig 8. We will now discuss in detail how $|Z_{\text{eq}}|/R_s$ and α_f affect the selectivity using Fig 7 and Fig 8.

For $\alpha_f = 1$ (Hold), the poles remain purely real as predicted by (25). The rightmost pole in Fig 8 shifts to a lower frequency for decreasing $|Z_{\text{eq}}|$, and the leftmost pole to a higher frequency. This means that for $|Z_{\text{eq}}| \leq R_s$ (large C_s), the rightmost (low frequency) pole primarily determines the bandwidth of the resulting filter. The second pole (the leftmost pole in Fig 8) moves to a frequency much higher than the filter bandwidth (in Fig 8 it moves off screen for $|Z_{\text{eq}}|/R_s \leq 1.6$ with $f_{p2} > 3f_{-3\text{dB}}$). At frequencies between these two pole frequencies, the filter roll-off is only first-order, which is especially visible for $|Z_{\text{eq}}|/R_s = 0.1$ in Fig 7a. It could be concluded that from a selectivity point of view, $|Z_{\text{eq}}| > R_s$ should be larger than approximately 1.5, as in that case Fig 7a indicates almost no selectivity degradation. However, as will be discussed in Section III-B, the reduced selectivity for small $|Z_{\text{eq}}|/R_s$ comes with improved NF, which make designs with $|Z_{\text{eq}}|/R_s < 1$ a sensible design point in situations where achieving a low NF is prioritized over achieving a high frequency-selectivity.

if $\alpha_f \approx 0$ (Reset), inspection of (25) reveals that both poles are located at $\beta_2 = (C_h)/(C_h + C_s)$ (in z -domain), a result consistent with [1]. As the poles have the same expression regardless of $|Z_{\text{eq}}|$ (C_s), the selectivity remains unchanged when changing this design parameter. Therefore, all poles in the Pole-Zero plot (square data markers) and all normalized curves in Fig 7b overlap. The absolute transfer functions are affected by $|Z_{\text{eq}}|$, particularly showing considerable in-band losses for low $|Z_{\text{eq}}|/R_s$. We will discuss the implications of in-band (signal) losses in Section III-B.

When $\alpha_f = -1$ (Invert), the real part of both poles is equal, and the root in (25) becomes negative, resulting in a complex pole pair. The selectivity is improved slightly when lowering $|Z_{\text{eq}}|/R_s$ (larger C_s), mainly through the reduction of the droop at the band-edge, as the Q of the poles is increased (see Fig 8). It should be noted that, as pointed out in [21] and shown in Fig 8, the maximum quality factor Q for a 2-pole filter is

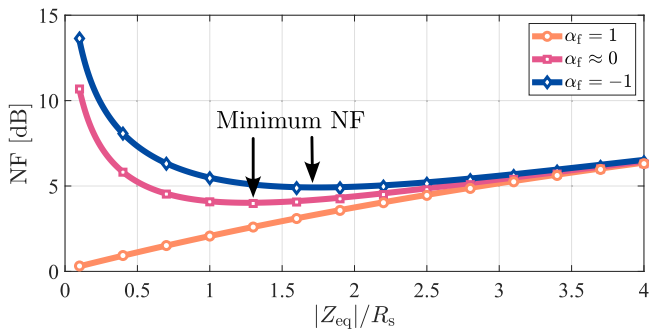


Fig. 9. In-band NF of the network vs $|Z_{\text{eq}}|/R_s$. The markers represent Spectre X sampled PNOISE simulations for (20b), and the solid lines represent the analytical model up to (22). The number of poles N does not affect this result. We assume that the filter is interleaved or pipelined $N + 2$ times to reach optimal noise performance. $R_{\text{sw}} = 0.02R_s$.

limited to $1/\sqrt{2}$. The improvement of selectivity by lowering $|Z_{\text{eq}}|/R_s$, comes at the expense of in-band losses in excess of those occurring for $\alpha_f \approx 0$, as shown by the absolute TFs in Fig 7c.

B. Noise Performance Considerations

In Section II-E, a method was described to calculate the NF of the generalized circuit. Fig 9 shows the NF of the filter versus $|Z_{\text{eq}}|/R_s$ for $\alpha_f \in \{1, 0, -1\}$. The NF is calculated using (22) for a single frequency well below the $f_{-3\text{dB}}$ of the filter.

The curves in Fig 9 can be used as a guide to minimize the NF of a filter with a given transfer function using (23). To understand how these curves (and thus the minimum NF for each α_f) are independent of R_s , we first note that the x-axis in Fig 9 is normalized to R_s as described in (23). Increasing (decreasing) R_s for a given N , f_s and $|Z_{\text{eq}}|/R_s$ requires a proportional increase (decrease) in C_s . To keep the filter response the same, C_h must change proportionally with C_s . As a result, the transfer functions of each of the noise contributions of the filter also remain constant. While an increase (decrease) in R_s proportionally increases (decreases) its input-referred voltage noise PSD in (19), the same is true for the noise contributions resulting from each charge sharing phase, as described by (13), and the reset phase, as described by (18). As such, a change in R_s results in an equal, proportional change in both the total input-referred noise PSD $S_{n,\text{interleaved,IRN}}(f)$ and the input-referred voltage noise PSD $S_{n,R_s}(f)$ contributed by R_s alone. Thereby, (22) is independent of R_s and the curves in Fig 9 hold for any R_s , as long as the mentioned assumptions in Section II are respected.

The definition of $|Z_{\text{eq}}|/R_s$ accounts for $N + 2$ interleaved/pipelined stages to minimize NF, as discussed in Section II-E.5. If less interleaved/pipelined stages are present, the NF degrades. We will discuss the results in Fig 9 by splitting up into 3 operating regions: $|Z_{\text{eq}}| \gg R_s$, $|Z_{\text{eq}}| \approx R_s$, and $|Z_{\text{eq}}| \ll R_s$. For these regions, we discuss how NF is degraded by (in-band) signal attenuation [$|H_{\text{eq}}|^2(f)$ in (20b)] and/or (sampled) noise contributions [$S_{n,\text{kernel,ORN}}$ in (20b)] in the filter.

When $|Z_{\text{eq}}| \ll R_s$, in-band signals are attenuated for the implementations with $\alpha_f \in \{0, -1\}$ (see Fig 7b and 7c), but

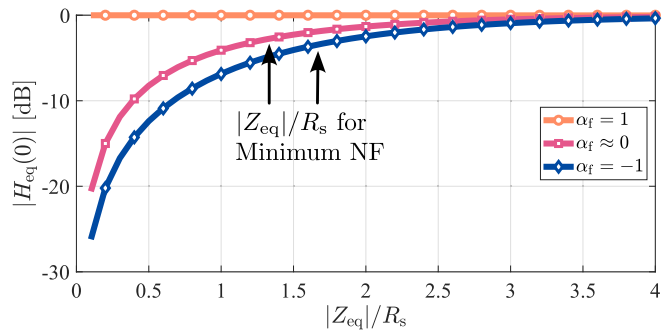


Fig. 10. In-band signal attenuation vs. $|Z_{\text{eq}}|/R_s = 0.1$ to $|Z_{\text{eq}}|/R_s = 4$. Markers are Spectre X, solid lines evaluate (12) for $f = 0$. The arrows indicate the design point that yields the lowest NF (Fig 9), resulting in a signal loss of 2.9 dB and 3.2 dB for $\alpha_f \approx 0$ and $\alpha_f = -1$, respectively. The number of poles N does not affect this result. $R_{\text{sw}} = 0.02R_s$.

experience negligible attenuation if $\alpha_f = 1$ (as shown in Fig 7a). The in-band attenuation of the filters can be found by evaluating (12) at $f \ll f_{-3\text{dB}}$, and is shown in Fig 10. Intuitively, this attenuation can be explained by considering the time-domain behavior when C_s samples $v_{\text{in}}(t)$ through R_s . The in-band loss of the filter is determined by how much v_{C_s} settles to v_{in} during the sample phase $\hat{\phi}_s$. For implementations with $\alpha_f \in \{0, -1\}$, the voltage on C_s at the start of the sample phase is either 0V (when $\alpha_f \approx 0$), or even $-v_{C_s}(t - T_s)$ when $\alpha_f = -1$. C_s gets subsequently charged to $v_{\text{in}}(t)$ through R_s . For lower values of $|Z_{\text{eq}}|$, C_s increases, and v_{C_s} cannot fully charge to v_{in} . This results in the increased in-band losses shown in Figs 7b and 7c. When no reset is present ($\alpha_f = 1$), all C_h capacitors will settle to the input voltage and in-band signals remain present on C_s after charge-sharing with all history capacitors. This results in little in-band attenuation during input sampling during the next clock period, as shown in Fig 7a. When $|Z_{\text{eq}}| \ll R_s$, it is this in-band loss for $\alpha_f \in \{0, -1\}$ that dominates the NF through $|H_{\text{eq}}(f)|^2$ in (20b), while these losses are negligible if $\alpha_f = 1$.

When $|Z_{\text{eq}}| \gg R_s$ the C_s capacitor is relatively small, and v_{C_s} can reasonably settle to v_{in} within τ_{on} . This results in negligible in-band signal attenuation for all α_f (as shown in Fig 7). As the sampling capacitor reduces in size with increasing $|Z_{\text{eq}}|$, the output noise density of the filter calculated with (20) increases. Since $|H_{\text{eq}}(f)|^2$ approaches 1 for all filters, the NF curves for $|Z_{\text{eq}}| \gg R_s$ converge to the same value at the right in Fig 9. As $|Z_{\text{eq}}|$ gets much bigger than R_s , the NF will keep increasing due to increasing contributions of sampled noise, while no additional signal is present. Thus, when $|Z_{\text{eq}}| \gg R_s$, the NF is dominated by sampled noise contributions ($S_{n,\text{kernel,ORN}}$) in (20b).

The case for $|Z_{\text{eq}}| \approx R_s$ is the point where the NF transitions from being degraded primarily by significant input signal losses for $\alpha_f \in \{0, -1\}$ (with only minor filter noise contribution), towards being primarily degraded by significant noise contributions (with negligible signal loss). An optimum between these two extremes exists that balances the two effects dominating the extremes. Fig 9 shows that for $\alpha_f \approx 0$ and $\alpha_f = -1$, the NF is minimized for $|Z_{\text{eq}}|/R_s \approx 1.3$ and $|Z_{\text{eq}}|/R_s \approx 1.7$, respectively. For implementations with $\alpha_f = 1$, no optimum exists, as there is negligible signal

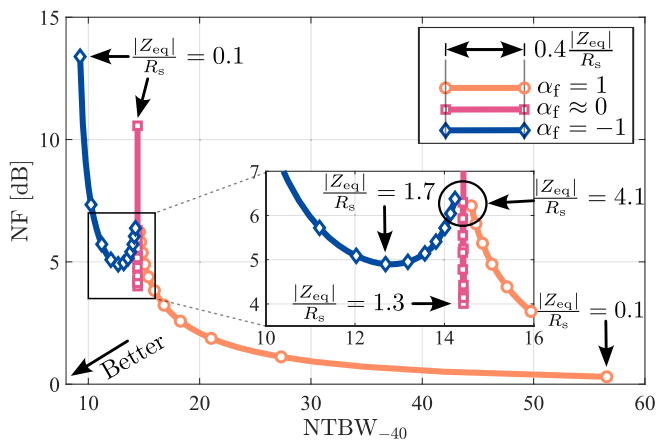


Fig. 11. Noise vs. selectivity (number of transition bandwidths) for $N = 2$. The different lines in the plot each represent their own feedback factor α_f . The distance between the drawn markers can be used to identify the design parameter $|Z_{eq}|/R_s$ by counting the elapsed markers since the start (end). $|Z_{eq}|/R_s$ runs from 0.1 to 4.1 in ten steps of 0.4. $R_{sw} = 0.02R_s$.

attenuation for $|Z_{eq}| \ll R_s$. Instead, filters with $\alpha_f = 1$ exhibit an NF that increases proportionally to the increase in ORN.

C. Implications of In-Band Signal Attenuation

We caution the reader of the implications caused by the in-band attenuation (Fig 10) occurring for implementations using $\alpha_f \in \{0, -1\}$ when considering the NF of the PSC-IIR filter in a system context. Not only is the NF of the standalone filter affected by the signal attenuation (Section III-B), but it may also impact the design considerations of the circuits following the filter. If, for instance, an amplifier is used to amplify the output of the filter, its IRN must be designed to keep the cascaded NF of the filter + amplifier at an acceptable level. If the input signal is attenuated by a factor due to the reset or C_s -inversion in the filter, the IRN of the cascaded baseband amplifier needs to be reduced to keep the cascaded NF equal. Thus, resetting or inverting C_s to improve filter selectivity may disproportionately degrade NF beyond that predicted by Fig 9 on a system level or result in considerable power consumption increase elsewhere in the system.

D. Noise-Versus-Selectivity Design Space

In Sections III-A and III-B, we showed that both Selectivity and Noise are affected by $|Z_{eq}|/R_s$ and α_f . This section will discuss how $|Z_{eq}|$ controls the trade-off between them. First, we illustrate the NF versus selectivity (as defined in (24) for $A_{stop} = -40$ dB) in Fig 11. Note that $|Z_{eq}|/R_s$ can be interpreted from the data markers in the figure and can be directly related to the TF and noise characteristics in Fig 7 and Fig 9, respectively. We relate Fig 11 to the results discussed in Sections III-A and III-B first.

When $\alpha_f = 1$, there is no distinct minimum NF, as illustrated in Fig 9. Thus, it is possible to reduce $|Z_{eq}|/R_s$ (increase C_s) to reduce the NF. However, the selectivity worsens as can be seen in Fig 7a and Fig 8, due to the presence of a bandwidth-limiting low-frequency pole for lower $|Z_{eq}|/R_s$, as discussed in Section III-A.

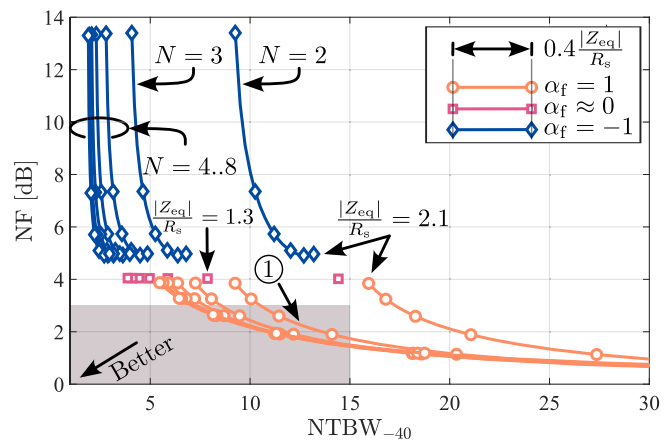


Fig. 12. Effect of increasing the number of C_h capacitors from $N = 2$ to $N = 8$. Not all line segments have their N annotated to minimize clutter, but $N = 2$ always starts right, and increases when moving left, up to $N = 8$. $|Z_{eq}|/R_s$ from 0.1 to 2 in steps of 0.4 for $\alpha_f \in \{1, -1\}$ and $|Z_{eq}|/R_s = 1.3$ for $\alpha_f = 0$ to minimize visual cluttering of the figure. $R_{sw} = 0.02R_s$. The shaded area and marked '1' are relevant for Appendix A.

When $\alpha_f \approx 0$, all poles of the filter are located at the same frequency (as shown in Fig 8). Thus, $|Z_{eq}|/R_s$ does not change the transition bandwidth, and selectivity (NTBW) is only dependent on the number of poles N . NF is affected by $|Z_{eq}|/R_s$ with a distinct minimum as illustrated in Fig 9. As NF is affected by $|Z_{eq}|/R_s$ and selectivity is not, the result is a vertical line in Fig 11. When optimizing the circuit for noise, it is sensible to pick the design point associated with the minimum NF: $|Z_{eq}|/R_s \approx 1.3$, as shown in Fig 9, unless demands on chip area, input matching, maximum f_s , or power-consumption dictate otherwise.

When $\alpha_f = -1$ there is an improvement of selectivity for reducing $|Z_{eq}|/R_s$. There is an observed minimum in the NF at $|Z_{eq}|/R_s \approx 1.7$ as shown in Fig 9. Lowering $|Z_{eq}|/R_s$ to improve selectivity is possible, but keep in mind that the NF of the filter worsens, and the in-band attenuation starts to increase considerably, while the selectivity begins to asymptote (Fig 8 and Fig 7c).

For $|Z_{eq}| \gg R_s$, the noise and selectivity performance become nearly independent of α_f , as shown by the point encircled around $|Z_{eq}|/R_s = 4.1$ in the inset in Fig 11. Fig 7 shows that selectivity is mostly unaffected by α_f , as for large $|Z_{eq}| \beta_1 \approx 0$, resulting in all filter poles residing at the same frequency as predicted by (25). Likewise, the NF of all α_f is roughly equal (right side in Fig 9), as the output referred noise caused by the small C_s dominates while input signals experience negligible attenuation (Fig 7). Together, this results in the convergence point at $|Z_{eq}|/R_s = 4.1$ in Fig 11. If $|Z_{eq}|/R_s > 4.1$, all three implementations will continue to degrade in NF as ORN increases with reducing C_s at negligible improvement of selectivity.

E. Increasing the Number of Poles

Fig 11 provides guidance in selecting which α_f topology to pick to implement a filter given a specific selectivity and/or NF, but only does so for $N = 2$. Increasing the number of history capacitors adds additional poles to the TF and thus may improve the selectivity. To investigate this, we used our

model to derive the selectivity for $N = [2, 3, \dots, 8]$, with the results shown in Fig 12. It can be seen that from $N = 2$ to $N = 3$, a considerable selectivity improvement is achieved for all α_f . After $N = 4$, the improvement in selectivity begins to asymptote. As indicated by the data-markers representing $|Z_{\text{eq}}|/R_s$, moving only horizontally for changing N in Fig 12 (thus keeping $|Z_{\text{eq}}|/R_s$ constant), an increase in N does not change the NF. In addition, in-band signal attenuation also does not change when increasing N . As discussed in Section III-B, the in-band attenuation is determined by the degree of settling of the voltage on C_s during τ_{on} , which change in equal proportions for increasing N , keeping the transfer from v_{in} to v_{C_s} constant.

It is worth highlighting that Fig 12 encompasses a considerable number of realizations of Fig 1. It therefore indicates the attainable selectivity (as defined in (24) with $A_{\text{stop}} = -40$). It also shows which topology (α_f) may be best suited to implement a combination of selectivity and NF, as the data-markers in Fig 12 represent which $|Z_{\text{eq}}|/R_s$ is used for this data-point. It is possible to find a full filter realization (with component values) using (23) and Fig 1 for individual points in the graph. This can considerably reduce the time spent on dimensioning and comparing different topologies. In Appendix A, we show an example that uses the results presented in Fig 12 to synthesize a filter from selectivity and NF specifications.

IV. CONCLUSION

This article investigated the selectivity and noise characteristics of three PSC-IIR LPFs driven directly from a source resistance. By assigning each topology a new design parameter ‘feedback factor’ α_f , a singular model was derived that can efficiently analyze the exhaustive design space. The ‘feedback factor’ α_f captures three possible techniques of handling the sampling capacitors between clock periods: resetting the sampling capacitor C_s ($\alpha_f \approx 0$), inverting C_s ($\alpha_f = -1$), or simply do nothing ($\alpha_f = 1$). The comprehensive model used an adjoint network with a state-space matrix to track the capacitor voltages during discrete clock intervals. We included noise analysis by evaluating noise folding from clock harmonics during sampling and charge-sharing and calculating their ORN contributions using their associated transfer functions. The analysis results remain valid irrespective of the operating region of the input sampler, which allowed us to evaluate the broad design space without loss of accuracy when the size of the sampling capacitor becomes large.

We have shown that the combination of finite source resistance, α_f , and component sizing place a lower limit on the achievable NF for a given filter selectivity and that we can control the trade-off between them through a (normalized) design parameter $|Z_{\text{eq}}|/R_s$. This relation was quantified by plotting the selectivity of a filter (number of transition bandwidths) versus the NF. The resulting selectivity versus NF graphs are used to find limits in attainable selectivity and NF, as well as to provide guidance in navigating the trade-off between them.

When driving a PSC-IIR LPF from a resistive source, there is a minimum in the NF that can be achieved when $\alpha_f \approx 0$ or $\alpha_f = -1$. The minimum NF for a resetting implementation

($\alpha_f \approx 0$) is approximately 4dB for $|Z_{\text{eq}}|/R_s \approx 1.3$, and $\text{NF} \approx 4.9\text{dB}$ at $|Z_{\text{eq}}|/R_s \approx 1.7$ when the sampling capacitor is inverted between clock periods ($\alpha_f = -1$). We showed that this limitation arises from signal losses in the input sampler when $|Z_{\text{eq}}| \ll R_s$, and considerable switched-capacitor noise contributions when $|Z_{\text{eq}}| \gg R_s$. When $\alpha_f \approx 0$, selectivity does not change upon changing $|Z_{\text{eq}}|/R_s$. The best selectivity for a fixed number of poles is achieved when inverting the sampling capacitor between clock periods. However, we caution the reader that signal losses will become considerable for small $|Z_{\text{eq}}|$ (big C_s when $\alpha_f \in \{0, -1\}$), and may affect the design of subsequent circuits. If the sampling capacitor is left un-altered between clock periods ($\alpha_f = 1$), the NF can theoretically be reduced to values well below the minima available when $\alpha_f \in \{0, -1\}$, but this is accompanied by a degradation in filter selectivity due to the presence of a low-frequency pole, causing an initial first-order roll-off even if a large number of C_h capacitors are present.

Assuming an appropriately interleaved or pipelined system, selectivity does improve upon adding more poles to any of the filters without necessarily degrading NF. However, in the limit towards an infinite number of poles, the selectivity of each of the three passive PSC-IIR filters described in this article reaches an upper limit (see Fig 12).

APPENDIX A

DESIGNING USING THE SELECTIVITY VS NF PLOT

In this appendix, we describe an example filter design with the following specifications: a NF less than 3dB, and a $\text{NTBW}_{-40\text{dB}}$ of at most 15. We target a 10MHz bandwidth and assume other relevant system parameters to be: $f_s = 1\text{GHz}$, $R_s = 50\Omega$.⁹ We will use Fig 12 to translate specifications into a network from Fig 1.

1) *Selectivity and NF Requirement:* The $\text{NTBW}_{-40\text{dB}} < 15$ and $\text{NF} < 3\text{dB}$ specifications together define the shaded area shown in Fig 12, in which all compatible designs lie. As can be seen, there are multiple possible implementations, in which case it is possible to prioritize certain aspects over the others: 1) minimize NF (pick lowest curve), 2) minimize the number of poles and consequently circuit complexity and area (pick lowest N), 3) pick a preferred α_f , if for instance droop is of concern.¹⁰ If there are no implementations in the shaded area constricting NF and selectivity, the filter is not implementable as a PSC-IIR filter following the generalized topology of Fig 1. For our example application, we will pick the design point indicated with ① in Fig 12.

2) *Determining Number of Poles, Feedback Factor, and Normalized Design Parameter:* We will now extract the network parameters for Fig 1 for the selected point ①. The α_f and N are determined by the line (segment) to which ① points. In our example application, we find $\alpha_f = 1$ and $N = 3$. Next, we extract the design parameter $|Z_{\text{eq}}|/R_s$ from the curve by

⁹Generally R_s will be a given, and f_s should be taken sufficiently high such that aliasing is not detrimental. In practice, this means that a continuous time pre-filter with sufficient alias suppression should be present somewhere before the sampling stage.

¹⁰In our example application, only $\alpha_f = 1$ is possible.

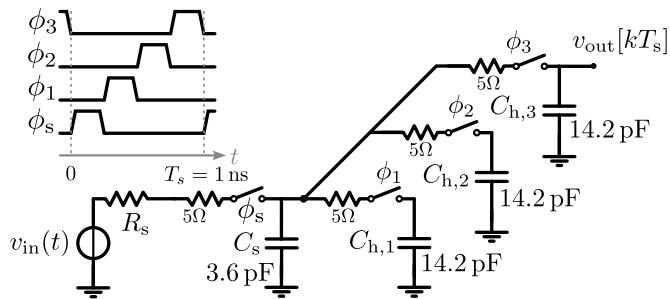


Fig. 13. Resulting filter design with component values.

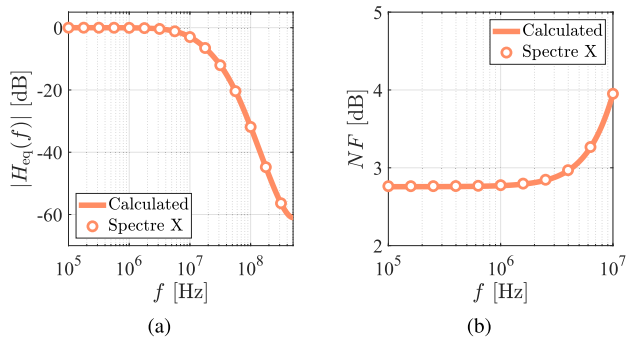


Fig. 14. Results from the design example. (a) TF as computed from (12) and with Spectre sampled PAC. (b) In-band NF as calculated in (22) and using Spectre PNOISE results for (20b).

checking the number of markers passed since the start (or end).¹¹ In the example case $|Z_{eq}|/R_s \approx 1.1$. From (23) we find $C_s \approx 3.6\text{pF}$ and using (21) with $N = 3$, we find that the filter should be pipelined/interleaved five times to reach the NF indicated by Fig 12.

If the selected α_f is 0 or -1 , and there, for instance, will be an amplifier following the filter under design, It is recommended to check the implications of the in-band attenuation on a system level. The in-band signal attenuation can be read from the graph in Fig 10.

3) *Setting the Bandwidth and Dimension the Switches:* For the charge-share switches, the primary consideration is to ensure that the capacitors' voltages can settle sufficiently during the on-time of a single clock sub-phase τ_{on} . For the sample switch, it is important to realize that it appears in series with R_s , and therefore could affect NF and/or transfer characteristics. A complete discussion on switch dimensioning is beyond the scope of this article, and therefore we pragmatically set $R_{sw} = 5\Omega$, i.e., 1/10th of R_s , making it of minor influence.

The bandwidth of the filter is mainly determined by α_f , $|Z_{eq}|$ and C_h . As $|Z_{eq}|$ was fixed in the previous step to determine NF, and α_f is also fixed, C_h needs to be adjusted to set the bandwidth. We do this by (numerically) solving (12) such that $f_{-3\text{dB}} = 10\text{MHz}$. We find $C_h \approx 14.2\text{pF}$.

The resulting filter topology with component values is shown in Fig 13. Fig 14 shows the TF from (12) and NF obtained using (22) of the resultant filter. The NF is slightly higher in Fig 14 than predicting with Fig 12, due to $R_{sw} = 5\Omega$.

¹¹In the case of $\alpha_f \approx 0$, $|Z_{eq}|/R_s$ will always be ≈ 1.3 .

In Fig 14, we see excellent agreement between the calculated and simulated results.

REFERENCES

- [1] M. Tohidian, I. Madadi, and R. B. Staszewski, "Analysis and design of a high-order discrete-time passive IIR low-pass filter," *IEEE J. Solid-State Circuits*, vol. 49, no. 11, pp. 2575–2587, Nov. 2014.
- [2] Y. Xu and P. R. Kinget, "A switched-capacitor RF front end with embedded programmable high-order filtering," *IEEE J. Solid-State Circuits*, vol. 51, no. 5, pp. 1154–1167, May 2016.
- [3] S. Z. Lüleç, D. A. Johns, and A. Liscidini, "A third-order integrated passive switched-capacitor filter obtained with a continuous-time design approach," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 10, pp. 3643–3652, Oct. 2019.
- [4] N. Barber, "Narrow band-pass filter using modulation," *Wireless Engineer*, vol. 24, no. 5, pp. 4–132, 1947.
- [5] M. Soer, E. Klumperink, Z. Ru, F. E. van Vliet, and B. Nauta, "A 0.2-to-2.0 GHz 65 nm CMOS receiver without LNA achieving $>11\text{dBm}$ IIP3 and $<6.5\text{ dB NF}$," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 222–223.
- [6] M. De Matteis, A. Pezzotta, S. D'Amico, and A. Baschiroto, "A 33 MHz 70 dB-SNR super-source-follower-based low-pass analog filter," *IEEE J. Solid-State Circuits*, vol. 50, no. 7, pp. 1516–1524, Jul. 2015.
- [7] S. D'Amico, M. Conta, and A. Baschiroto, "A 4.1-mW 10-MHz fourth-order source-follower-based continuous-time filter with 79-dB DR," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2713–2719, Dec. 2006.
- [8] Y. Xu, P. K. Venkatachala, Y. Hu, S. Leuenberger, G. C. Temes, and U.-K. Moon, "A charge-domain switched- G_m -C band-pass filter using interleaved semi-passive charge-sharing technique," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 2, pp. 600–610, Feb. 2020.
- [9] A. Bozorg and R. B. Staszewski, "A clock-phase reuse technique for discrete-time bandpass filters," *IEEE J. Solid-State Circuits*, vol. 57, no. 1, pp. 290–301, Jan. 2022.
- [10] S. Manetti and A. Liberatore, "Switched-capacitor lowpass filter without active components," *Electron. Lett.*, vol. 16, no. 23, pp. 883–885, Nov. 1980.
- [11] Y. Xu, H. Hu, J. Muhlestein, and U.-K. Moon, "A 77-dB-DR 0.65-mW 20-MHz 5th-order coupled source followers based low-pass filter," *IEEE J. Solid-State Circuits*, vol. 55, no. 10, pp. 2810–2818, Oct. 2020.
- [12] A. Bozorg and R. B. Staszewski, "A charge-sharing IIR filter with linear interpolation and high stopband rejection," *IEEE J. Solid State Circuits*, vol. 57, no. 7, pp. 2090–2101, Jul. 2022.
- [13] S. V. Thyagarajan, S. Pavan, and P. Sankar, "Active-RC filters using the gm-assisted OTA-RC technique," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1522–1533, Jul. 2011.
- [14] P. Payandehnia et al., "A 0.49–13.3 MHz tunable fourth-order LPF with complex poles achieving 28.7 dBm OIP3," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 8, pp. 2353–2364, Aug. 2018.
- [15] I. Madadi, M. Tohidian, and R. B. Staszewski, "Analysis and design of I/Q charge-sharing band-pass-filter for superheterodyne receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 8, pp. 2114–2121, Aug. 2015.
- [16] A.-J. Annema, "Analog circuit performance and process scaling," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 46, no. 6, pp. 711–725, Jun. 1999.
- [17] B. Nauta, "Racing down the slopes of Moore's law," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, vol. 67, Feb. 2024, pp. 16–23.
- [18] D. L. Fried, "Analog sample-data filters," *IEEE J. Solid-State Circuits*, vol. SSC-7, no. 4, pp. 302–304, Aug. 1972.
- [19] S. Pavan and E. Klumperink, "Analysis of the effect of source capacitance and inductance on N -path mixers and filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 5, pp. 1469–1480, May 2018.
- [20] E. Zijlma, S. van Zanten, R. Plompen, E. A. M. Klumperink, R. A. R. V. D. Zee, and B. Nauta, "Analysis and design of a low-loss 1–10 GHz capacitive stacking N -path filter/mixer," *IEEE J. Solid-State Circuits*, early access, Jul. 12, 2024, doi: 10.1109/JSSC.2024.3407241.
- [21] S. Z. Lulec, D. A. Johns, and A. Liscidini, "A simplified model for passive-switched-capacitor filters with complex poles," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 6, pp. 513–517, Jun. 2016.
- [22] S. Pavan and R. S. Rajan, "Interreciprocity in linear periodically time-varying networks with sampled outputs," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 61, no. 9, pp. 686–690, Sep. 2014.

- [23] S. Z. Lulec, D. A. Johns, and A. Liscidini, "A 150- μ W 3rd-order Butterworth passive-switched-capacitor filter with 92 dB SFDR," in *Proc. Symp. VLSI Circuits*, Jun. 2017, pp. 142–143.
- [24] T. Iizuka and A. A. Abidi, "FET-R-C circuits: A unified treatment—Part II: Extension to multi-paths, noise figure, and driving-point impedance," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 63, no. 9, pp. 1337–1348, Sep. 2016.
- [25] S. Pavan and E. Klumperink, "Simplified unified analysis of switched-RC passive mixers, samplers, and N -path filters using the adjoint network," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 10, pp. 2714–2725, Oct. 2017.
- [26] M. C. M. Soer, E. A. M. Klumperink, P.-T. de Boer, F. E. van Vliet, and B. Nauta, "Unified frequency-domain analysis of switched-series-RC passive mixers and samplers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 10, pp. 2618–2631, Oct. 2010.
- [27] B. Razavi, *RF Microelectronics*, vol. 2. New York, NY, USA: Prentice-Hall, 2012.



Roel Plompen (Graduate Student Member, IEEE) received the B.Sc. and M.Sc. degrees in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2016 and 2019, respectively, where he is currently pursuing the Ph.D. degree with the Bram Nauta's Integrated Circuit Design Group. His current research interests include radio frequency CMOS circuits and switched-capacitor filters.



Jeroen Ponte (Graduate Student Member, IEEE) was born in Harlingen, The Netherlands. He received the B.Sc. and M.Sc. (cum laude) degrees in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2018 and 2020, respectively, where he is currently pursuing the Ph.D. degree with the Integrated Circuit Design Group. His research interests include, but are not limited to, passive switched-capacitor filters, and analog-to-digital conversion, with a focus on noise-shaping architectures and radio frequency circuits.



Stef van Zanten (Graduate Student Member, IEEE) was born in Harderwijk, The Netherlands, in March 1996. He received the B.Sc. and M.Sc. degrees (cum laude) in electrical engineering from the University of Twente, Enschede, The Netherlands, in 2018 and 2020, respectively, where he is currently pursuing the Ph.D. degree with the Integrated Circuit Design Group.



Eric A. M. Klumperink (Fellow, IEEE) was born in Lichtenvoorde, The Netherlands, in April 1960. He received the B.Sc. degree from HTS, Enschede, in 1982. He worked in industry on digital hardware and software and then joined the University of Twente, Enschede, in 1984, shifting focus to analog CMOS circuit research. This resulted in several publications and his Ph.D. thesis "Transconductance-Based CMOS Circuits: Circuit Generation, Classification and Analysis," in which systematic circuit generation lead to the discovery of thermal noise cancelling in 1997. In 1998, he became a Professor with the IC-Design Laboratory, Twente, and shifted focus to RF CMOS circuits during a sabbatical in 2001 with Ruhr Universitaet Bochum, Germany. Since 2006, he has been an Associate Professor, teaching analog & RF IC electronics and guiding Ph.D. and M.Sc. projects in RF CMOS circuit design, with a focus on software defined radio, cognitive radio, and beamforming. He is currently the Project Leader of Horizon Europe SNS Project 6G-Reference (2024–2027). He also served as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS (2006–2007), IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART I: REGULAR PAPERS (2008–2009), and the IEEE JOURNAL OF SOLID-STATE CIRCUITS (2010–2014); and as a Technical Program Committees Member of ISSCC (2011–2016), RFIC Symposium (2011–2021), and ESSCIRC (2019–2023). He holds 16 patents, authored, or co-authored over 200 internationally refereed journals and conference papers and was recognized as more than 20 ISSCC paper contributor over (1954–2013). He was a co-recipient of the ISSCC 2002 and the ISSCC 2009 "Van Vessel Outstanding Paper Award," served as an IEEE SSC Distinguished Lecturer.



Bram Nauta (Fellow, IEEE) was born in Hengelo, The Netherlands. He received the M.Sc. degree (cum laude) in electrical engineering and the Ph.D. degree in analog CMOS filters for very high frequencies from the University of Twente, Enschede, The Netherlands, in 1987 and 1991, respectively.

In 1991, he joined the Mixed-Signal Circuits and Systems Department, Philips Research, Eindhoven, The Netherlands. In 1998, he returned to the University of Twente as a Full Professor heading the new IC Design Group. In 2014, he was nominated as a

Distinguished Professor and from 2016 to 2020, he was the Chair of the Electrical Engineering Department. In 2022, he co-founded "ChipTechTwente," a local ecosystem initiative with 50 semiconductor-related companies, partners, and knowledge institutions. His research interests include analog and radio frequency CMOS circuits.

Dr. Nauta is a member of the Royal Netherlands Academy of Arts and Sciences (KNAW). He was a co-recipient of the ISSCC 2002 and 2009 "Van Vessel Outstanding Paper Award," and in 2023, he received an ISSCC Author-Recognition Award for its first 70 years as a top 10 contributor in the conference's history. He served two terms as a Distinguished Lecturer of the IEEE Solid-State Circuits Society. In 2014, he received the "Simon Stevin Meester" Award (500 000 Euros), the Largest National Prize in The Netherlands for achievements in engineering sciences. In 2019, he received an European Research Council (ERC) Advanced Grant (2.5 Million Euros, personal grant). In 2023, he received the inaugural "Dutch Innovation Award" and the NWO Stevin Prize (1.5 Million Euros), the largest national science prize in The Netherlands for "Exceptional Success in Knowledge Exchange and Impact for Society." He served as the Editor-in-Chief (2007–2010) for the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC) and was the 2013 Program Chair of the International Solid-State Circuits Conference (ISSCC). He served as the President for the IEEE Solid-State Circuits Society (2018–2019). Also, he served as an Associate Editor for IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—PART II: EXPRESS BRIEFS (1997–1999) and of IEEE JOURNAL OF SOLID-STATE CIRCUITS (2001–2006). He was on the technical program committee of the Symposium on VLSI Circuits (2009–2013) and served on the steering committee and program committee (1999–2017) of European Solid-State Circuit Conference (ESSCIRC). He served on the program committee (2003–2013) and the Executive Committee (2007–2015) and since 2022 of the ISSCC, and in 2023, he joined the Program Committee of the Advances in Analog Circuit Design Workshop Series (AACD).