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A Reliability Model for Interlayer Dielectric Cracking During Fast Thermal Cycling

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ABSTRACT

Interlayer dielectric (ILD) cracking can result in short circuits of multilevel interconnects. This paper presents a reliability model for ILD cracking induced by fast thermal cycling (FTC) stress. FTC tests have been performed under different temperature ranges (ΔT) and minimum temperatures (T_{min}). The Weibull distributions of time to failure are relatively well behaved with a similar slope. The number of cycles to failure increases with increasing T_{min}, even though ΔT increases. The Coffin-Manson law is used to model the failure rate only for test results having the same T_{min}. The obtained exponent value is in the range of brittle material cracking mechanism, which is confirmed by failure analysis and modelling of the failure mechanism. An extended Coffin-Manson law is developed to model failure rates during FTC stresses.

INTRODUCTION

With increasing power dissipation and decreasing chip size, thermomechanical failure in multilevel interconnects are more likely to become a reliability problem [1]. Recent publications have addressed thermomechanical failure issues of interconnect systems due to thermal cycling. It has been shown that the thermal cycling can crack metal films [2,3] as well as interlayer dielectrics [4], resulting in device failures. In order to use this understanding in reliability improvement of interconnect systems, the failure mechanism must be understood well enough to create a good failure rate model. Thermal cycling using an environmental chamber is far from the real operating condition of ICs working at high operating frequencies. Such "slow" temperature cycling test could mask failure mechanisms more relevant to field applications and may actually prevent detection of failure mechanisms likely to occur in the field. The thermal cycling failure mechanism is known to fit the Coffin-Manson law [5] ($N_f \sim [\Delta T]^{-q}$). However, this model may not be sufficient to predict the failure rate of fast thermal cycling (FTC) stress. In this paper, a study on the FTC reliability of a standard two level metallization is presented. We will deal with reliability tests, failure analysis, and modelling of failure mechanism, respectively. After considering these issues, we propose a reliability model for the FTC stress.

EXPERIMENTAL DETAILS

A test chip as shown in Figure 1a is designed with 2 metal layers, integrating a large n^+-Si resistor (about 4Ω) just below the die surface and a p/n diode in the middle of the resistor to generate and monitor temperature swings, respectively. Metal 1 (M1) is a long meandering line resistor located on the die surface and considered as the stressed line. Between the meandering line additional tracks on the both sides to detect sideways short circuits are implemented. Metal 2 (M2) is a large plate over the whole structure to detect interlayer short circuits. The ILD and passivation layers are both Si_3N_4. The test chip is encapsulated in a standard 17 pin plastic package for power ICs.

Table I. The fast thermal cycling test conditions.

Conditions	A	B	C	D	E
T_{min}[°C]	46	46	46	65	65
ΔT[°C]	220	200	180	230	210
Duty Cycle[%]	10	10	10	20	20

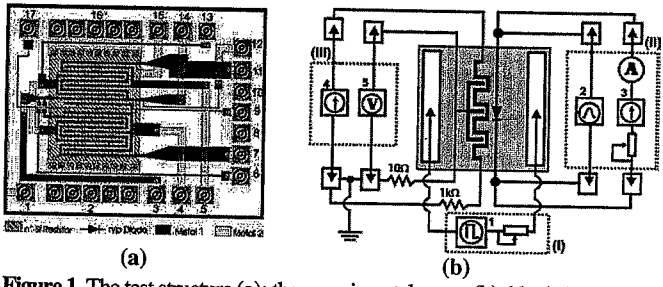


Figure 1. The test structure **(a)**; the experimental set up **(b)**; block (I) is the temperature generation scheme; block (II) is the temperature measurement scheme; block (III) is device failure detection scheme.

The scheme as shown in Figure 1b is employed for FTC tests, more details about the test method can be found in a previous paper [6]. The reliability test conditions as shown on Table I are used. The temperature cycling frequency is kept at 10Hz for all conditions. During FTC, a current of $0.1mA/\mu m^2$ is periodically passed through the metal line to detect short-circuits. This current should not impose any electromigration-induced damage on the metal line. A sample size of 24 devices is subjected to each condition. A device is considered to have failed when a significant voltage across the 10Ω resistor which is placed in series with the extrusion monitor is measured (see Figure 1b). The time to failure is taken as the time of the first short circuit.

RESULTS AND DISCUSSIONS

The results of time-to-failure data are analysed assuming a Weibull distribution, because the Weibull distributions are applicable in case of weakest link failures [1]. Weibull distribution plots of the time-to-failure data are shown in Figure 2a and 2b. The median time to failure (MTF) and the shape factor, β were extracted for all stress conditions and summarized in Table II. The distributions are relatively well behaved with similar shape factor, which implies that the failure mechanism is the same for all conditions. The number of cycles to failure N_f was plotted as a function of temperature range ΔT for three conditions A, B, and C. Using the Coffin-Manson equations, the exponent value has been found to be 8.4. Based on published data [5], this exponent value indicates that the failure mechanism is related to the fracture of brittle materials. SEM (Scanning Electron Microscope) verifications on the surfaces of M1 have been done with fresh and failed device as shown in Figure 3a and 3b, respectively. Only cracks are observed on the M1 surface of stressed devices. The cross-section, which has been made by chemical polishing and viewed by SEM, shows the cracking of ILD layer (see Figure 3c). These are consistent with the experimental estimation of the exponent value.

Table II. The reliability test results, MTF and slope, β.

Conditions	A	B	C	D	E
MTF[hrs]	30.8	66.9	165.2	65.8	193.7
β	1.4	1.4	1.2	1.3	1.0

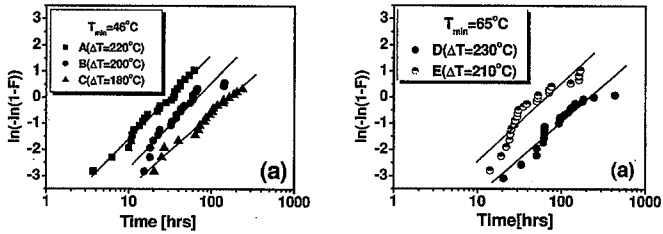
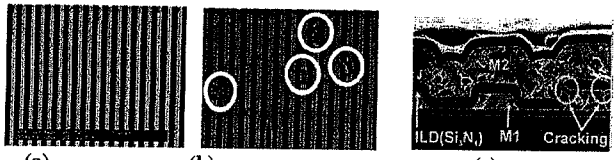


Figure 2. Weibull probability plot: (a) for conditions A, B, and C; (b) for conditions D and E.

The model to explain the failure mechanism is shown in Figure 4. It is briefly described as follows. The packaging substrate has a larger thermal expansion coefficient (TEC) than the silicon chip. Upon cooling down from the bonding temperature, the package substrate will contract more than the silicon chip, but the bonding prevents sliding between the substrate and the chip (see Figure 4a). Consequently, shear stresses will develop on the chip surface. The chip and the plastic package (polymer) are joined, so that the shear stresses are limited by the yield strength of the polymer. The result is that the shear stresses are imposed on the surfaces of the ILD (τ_o) and the metal layers (τ_m), respectively (see Figure 4b). Under the temperature cycling, the Al pad deforms plastically, resulting in relaxation of the shear stress τ_m. Therefore, the Al pad will not longer support the shear stress τ_o. This means τ_o is fully sustained by the ILD layer. Consequently, the stress magnitude σ_s in the ILD layer as calculated by (1) could build up to high levels, which may cause cracking of the ILD layer.

$$\sigma_s = (\tau_o - \tau_m)W/2t \quad (1)$$

Where, W and t are the width and the thickness of the metal pad, respectively. It can be seen that the failure mechanism is related to the shear stress from the packaging. This shear stress is generated due to the large difference in the TEC of silicon chip, package substrate, and moulding compound used in the assembly. Design, process, and materials all can be used to reduce this shear stress. For instance, during the package process, if the assembly materials have a TEC closely matched to that of silicon, the shear stress would significantly reduce [2]. This implies that the magnitude of shear stress, τ_o is strongly dependent on the temperature conditions and moulding compound temperature of plastic package. These features can affect the lifetimes of FTC tests. Interestingly, our test results showed that the lifetime does not always follow the Coffin-Manson equation. As shown in Figure 5a, the log-log plot of N_f as function of temperature range ΔT for cases of A, B, C, D, and E do not follow the same line. As can be seen in Table II, the lifetime of the FTC tests carried out at higher T_{min} and T_{max} have longer lifetimes, even although higher ΔTs are used. This can be explained due to the reduction of the mechanical stress from plastic packages after encapsulating when average temperature (acted as the ambient temperature) during FTC increased. This was extensively studied in [7]. The moulding



(a) (b) (c)

Figure 3. The failure analysis results: (a) and (b) showing the SEM image of M1 surfaces of fresh and stressed devices, respectively; (c) a cross-section showing cracking of ILD layer.

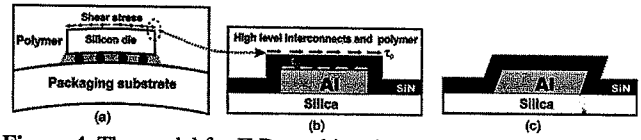


Figure 4. The model for ILD cracking due to plastic deformation after temperature cycling.

temperature also affects the mechanical stress of packaging as was reported by Usell [8]. In which, the strain on the silicon chip built up by the plastic package can be calculated by [8];

$$\varepsilon_c = \int_{T_{mold}}^{T_{amb}} \left[\left(\alpha_p(T) - \alpha_c \right) / \left(1 - E_c A_c / A_p E_p(T) \right) \right] dT \tag{2}$$

Where α, E, and A are the TEC, the effective modulus, and the effective cross-sectional area, respectively. The subscripts p and c are noted the plastic and the chip, respectively. ε_c is the in-plain train in chip. This model shows that the plastic strain after cooling from the moulding temperature (T_{mold}) to the ambient temperature (T_{amb}) is a function of the T_{mold}. With a FTC test, the peak temperature is reached in a short time and the heating is done locally. Therefore, the storage of the temperature on plastic package is small during the FTC, and the temperature dependence of α_p and E_p can be ignored. Then, the strain on the chip due to the plastic package during FTC can be approximated by

$$\varepsilon_c \propto \left(T_{avg} - T_{modl} \right) \tag{3}$$

Where, the T_{avg} is an average temperature during FTC, which is considered as the ambient temperature. The metal film is bonded to the silicon chip so that the strain of the metal film due to the plastic package has the same form (the absolute amplitude may be different).

$$\varepsilon_{Al}^{P} \propto \left(T_{avg} - T_{mold} \right) \tag{4}$$

During temperature cycling from T_{min} to T_{max}, the metal film (Al) deforms plastically due to the thermal mismatch. Assuming, TECs of aluminium and substrate are not very depending on temperature, and its in-plain strain can be expressed by (5)

$$\varepsilon_{Al}^{T} \propto \left(T_{max} - T_{min} \right) \tag{5}$$

This in-plain strain is constrained by the compressive stress from the plastic package. Therefore, the total strain is calculated by subtracting the strain from plastic package.

$$\Delta\varepsilon = \varepsilon_{Al}^{T} - \varepsilon_{Al}^{P} \tag{6}$$

When combining equations (4), (5), and (6), the number of cycle to failure can be expressed by

$$N_f \propto [\Delta\varepsilon]^{-q} \propto \left[C1(T_{max} - T_{min}) - C2(T_{avg} - T_{mold}) \right]^{-q} \tag{7}$$

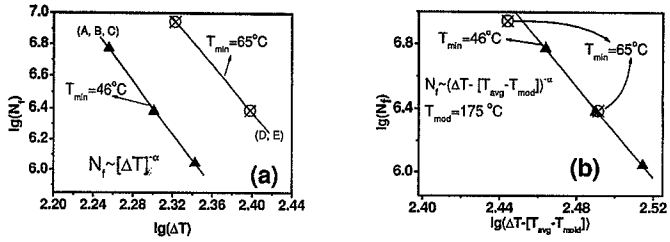


Figure 5. Log-Log plot: (**a**) used Coffin-Manson equation; (**a**) Used the a new approach model

To plot N_f as a function of ΔT for all conditions (A, B, C, E, and D), using equation (7), the T_{avg} is calculated by integrating the temperature cycle profile of each condition and the moulding temperature of 175°C was taken from the packaging process. C1 and C2 are assumed the same. The plotted result is shown in Figure 5b. It is clearly shown that the new model fits well for all the test results. The question is why the test conditions A, B, and C was well fitted with the Coffin-Manson equation as shown above. The test conditions A, B, and C have the same the T_{min}, and duty cycle is 10% so that the T_{avg} is almost the same for the three conditions. This means that in this case the equation (7) can be simplified to yield.

$$N_f \propto [(T_{max} - T_{min}) + C]^{-q} \tag{8}$$

Where, C is a constant. This is the same form as the Coffin-Manson equation.

CONCLUSIONS

Fast thermal cycling was used to study interlayer dielectric cracking induced failures of multilevel interconnects. It is shown that the Coffin-Manson law can only be used to model the failure rates of the fast thermal cycling under a certain test condition. A modification is needed for this failure mechanism. An extended Coffin-Manson equation has been proposed that models well the failure rates of all our test results from fast thermal cycling tests.

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