A 12b 1.7GS/s Two-Times Interleaved DAC with <-62dBc IM3 Across Nyquist Using a Single 1.2V Supply

Erik Olieman, Anne-Johan Annema, Bram Nauta
University of Twente, IC-Design Group
Enschede, The Netherlands

Ankur Bal, Pratap Narayan Singh
STMicroelectronics
G. Noida, India

***Abstract*—A two-times interleaved DAC using only a single supply voltage in a standard 65nm CMOS technology is presented. The interleaving architecture suppresses most of the non-idealities commonly found in high-speed DACs. Spurs generated by the interleaved architecture are suppressed by a novel calibration algorithm. The design achieves IM3 levels below -62dB across Nyquist with a clock frequency of 1.7GHz. The circuit's active area is 0.4mm^2 and the power consumption is 70mW from a nominal 1.2V supply.**

I. INTRODUCTION

Current-steering DACs are the most popular type of DAC for high speed signal generation. They consist of an array of fixed current sources and current switches on top of them that direct the sources' current either to the positive or to the negative output. Several static and dynamic error mechanisms limit the performance of current steering DACs; the dynamic typically limit the performance of high speed DACs [1]. The most important dynamic errors in current-steering DACs are due to the output capacitance of the current sources and due to switching errors related to e.g. timing mismatches.

The output capacitance of each current source usually is sufficiently constant for more than 12b resolution. However, the total capacitance at either of the DAC output nodes is code dependent, which results in harmonics in the DAC's output signal. This can be solved by e.g. adding cascode transistors with an added bias current at the cost of voltage headroom and power consumption [2].

The impact of switching errors can be reduced by using return-to-zero (RZ) switching [3], which is effective to improve linearity. However RZ switching drastically reduces the signal power while the power in the image frequencies is increased, which yields higher requirements on the subsequent filtering. Another known issue of RZ designs is their higher susceptibility to clock jitter compared to non-return-to-zero designs [4].

All these dynamic errors have in common that they occur around the switching time instance [5]. Timing errors are typically in the picosecond range while glitches and charging of the internal capacitances takes longer, but still only occupy a fraction of the total period. Some designs utilize this property of the dominant dynamic errors by disconnecting the DAC from the output around the switching moment [5]. In the DAC presented in this paper, dynamic errors are largely avoided using two interleaved sub-DACs (sDAC), each one connected half of the time to the output; the other half of the time the sDAC switches and settles to a new output value while being connected to a dummy output.

Since two sDACs are placed in parallel, and extra components are required to combine them into one output, this might look to be inefficient from both an area and a power viewpoint. However using interleaving, most of the dynamical non-idealities of individual sDACs do not propagate to the DAC output and hence the design of each individual sDAC can be simpler. Overall this translates in per-sDAC significantly reduced area and power requirements.

II. ARCHITECTURE

Fig. 1 shows the circuit diagram of the interleaved current steering DAC. In it, each sDAC essentially is a complete current DAC, including separate bias sources and decoder logic. The sDACs have a 6-6 segmentation, where the MSB sources are implemented with thermometer code and the LSB sources use binary code. Their output current goes to the sDAC multiplexer, which alternatively connects one sDAC to the output, and the other one to an identical dummy output. The resistive load consists of 50 Ohm on-chip resistors parallel to 50 Ohm off-chip resistors.

The interleaved DAC system in Fig. 1 theoretically solves many of the limitations inherent to a current-steering architecture, and the basic idea is already known for a long time [6]. Recent literature involving interleaved DACs, such as the architectures discussed in [7], also have two or more sDACs running in parallel at different phases. However they do not use an analog multiplexer to combine the sDACs, instead the output currents are summed directly. While that does remove the need for an analog multiplexer, it also means that since each sDAC is always connected to the output, any glitch generated by each sDAC propagates to the output. In [8] an analog multiplexer is used, but only simulation results are reported.

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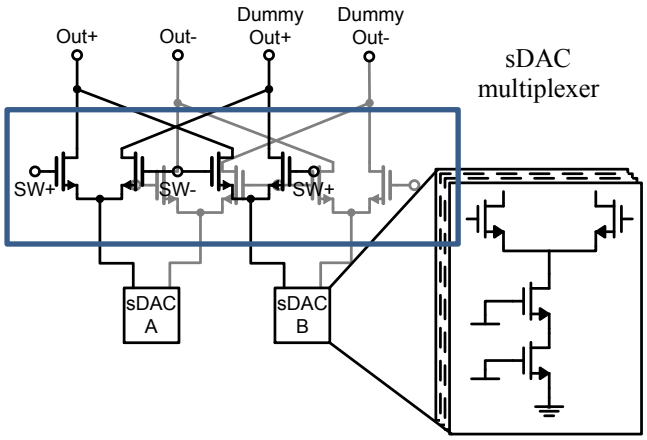

Figure 1: Interleaved DAC architecture consisting of 2 sDACs and an sDAC multiplexer

An interleaved architecture also introduces some new artifacts that limit the performance when not dealt with properly. This is probably the reason why this approach is not often used. Firstly, the multiplexer switch current is code dependent, which can cause significant spurs. Secondly both static matching demands and static timing demands become more stringent compared to those in a conventional current DAC. In our design both are dealt with.

A. Multiplexer switches

One of the strong points of conventional current DACs is that the switches used in these always switch the same current. Because of this, there is hardly any code-dependent switching and hence there is hardly any distortion products at the output due to switching. However, in interleaved DACs the multiplexer switches switch the full-scale output current, which is code-dependent.

Often the best way to switch currents is using transistors in saturation: these transistors provide reverse isolation and do not require a large signal swing at their gates. However their behavior is highly current-dependent which results in distortion. This distortion can be decreased a little at the cost of power by e.g. adding bleeder currents. In the design presented in this paper, the multiplexer switches are implemented with MOS transistors driven into triode. While triode operation requires relatively high drive voltage swings and does not provide much reverse isolation, triode operation is very beneficial in terms low distortion levels. To operate the multiplexer transistors in triode, an integrated (straight forward) capacitive level shift circuit is used to create gate drive voltages between 0.9V and 2V.

B. Static matching

The two sDACs are independent and therefore have uncorrelated INL curves. When interleaving, the difference in INL between the 2 sDACs causes an (interleaving) output spur located at a frequency equal to the fundamental tone mirrored around half Nyquist. The only way to eliminate this interleaving spur is to get similar (preferably identical) INL curves for both sDACs, using calibration. For calibration purposes small (digitally controlled) calibration current sources are included in parallel to all MSB current sources in the design.

A conventional way to calibrate is using a (more than) 12-bit linear ADC to calibrate the INL of both sDACs to near zero. This conventional way however requires a relatively complex ADC because of the required high linearity requirements over the full output signal range. The calibration for our interleaved DAC is different and requires only a low-linearity ADC. During calibration, first one of the sDACs is calibrated towards a sufficiently low DNL-INL and then the second sDAC is calibrated to get the same INL behavior.

To calibrate the first sDAC, each MSB source, which have a nominal weight of 64LSB, is calibrated to be equal to all LSB sources combined, a nominal weight of 63LSB, + one extra LSB source. Now the calibrating ADC only has to compare the value of the MSB source with a reference value and hence the ADC only needs to be monotone. Note that this method does calibrate the DNL, but due to cumulative errors the INL can still have a significant error. Next the MSB sources of the second sDAC are calibrated to have a transfer equal to that of the first sDAC. During this calibration phase, we only have to measure the difference between two values: again there are very low demands on the linearity of the calibrating ADC.

C. Dynamic matching

In interleaved DACs, the time intervals in which each sDAC is connected to the DAC output must be equal, otherwise spurs mirrored around half Nyquist occur. For a timing error Δt in the sDAC multiplexer, this spur gives rise to a lower bound on the spurious free dynamic range equal to:

$$\mathrm{SFDR}=20\log_{10}\left(\frac{1}{\Delta t * \pi f_{signal}}\right) \qquad (1)$$

This relation implies that for a full Nyquist signal at 1.7GS/s and an SFDR>70dB, the static timing error must be smaller than 110fs. These levels of timing accuracy cannot be obtained by matching only: also here calibration is required.

In our design we use a quasi-DC measurement to calibrate the timing. In it, first one of the sDACs is set to its maximum output value while the other one is set to its minimum value. The resulting average output voltage is dependent on the signals amplitude (previously calibrated, see section B) and the duty cycle of the generated square wave. The calibration can be repeated with the first sDAC at its minimum and the second at its maximum to further decrease mismatch effects.

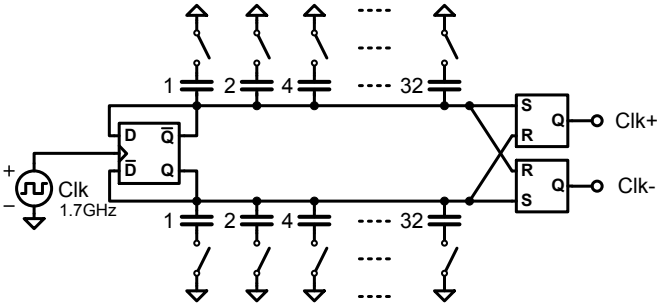

Figure 2: Timing generation + timing calibration circuitry

The timing calibration uses the timing generation circuit in Fig. 2 to adjust the edges of the clock signal until the duty cycle is sufficiently close to 50%. The circuit first divides the

input frequency by 2; a digitally controlled 2x6-bit capacitor bank can slightly delay both clock signals. Finally, the two SR-latches convert the time-delayed signals to two anti-phase square waves with a duty cycle that depends on the delay settings. The delay-range that can be created this way is ±3.3ps, with 50fs-55fs steps.

III. MEASUREMENT RESULTS

The DAC was produced in a standard 65nm CMOS technology. Fig. 3 shows the die micrograph, the active area is 0.4mm^2 and the chip is packaged in a standard QFN40 package. An on-chip sine generator with frequency and amplitude tuning control and dual tone option provides the test signals. The IC consumes 70mW from its single 1.2V supply, excluding sine generator. Parallel to the internal 50 Ohm resistors the DAC is externally loaded with 50 Ohm resistors, without the customary RF chokes which are generally required for sufficient voltage headroom. The interleaved DAC delivers 500mVpp-diff full-scale swing to the outputs.

A. Static matching

Fig. 4 shows the measured static INL of the two sDACs before and after calibration. Before calibration the two sDACs have different gains, resulting in a large difference in INL between the two sDACs. After calibration the INL is significantly improved, although the INL is still substantial because of both our rather noisy ADC and because we actually only calibrated the DNL. Most importantly, the differential INL is minimized: the second sDAC clearly follows the INL curve of the first sDAC curve, despite the noisy ADC. Before calibration the best-fit full-scale gain error is over 60LSB, after calibration this is less than 0.4LSB.

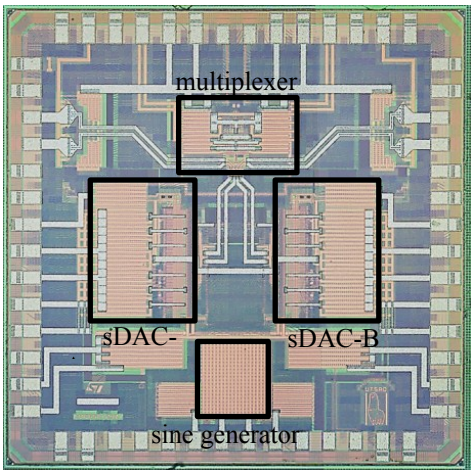

Figure 3: Die photograph

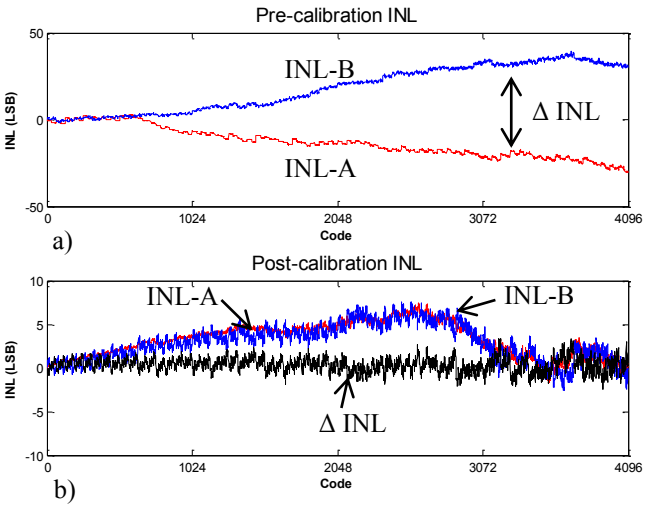

Figure 4: a) Static INL before and b) static INL after calibration

B. Spectrum

The spectral performance of the DAC is shown in Fig. 5. The median SFDR over Nyquist is 60dB, with a minimum of 58dB. The IM3 is above 62dB across Nyquist, with a median value of 73dB. Additionally it is clear that the interleaving spur does not limit performance. At Nyquist the interleaving spur is at -65dB; using (1) it follows that the timing error has been calibrated to around 210 fs.

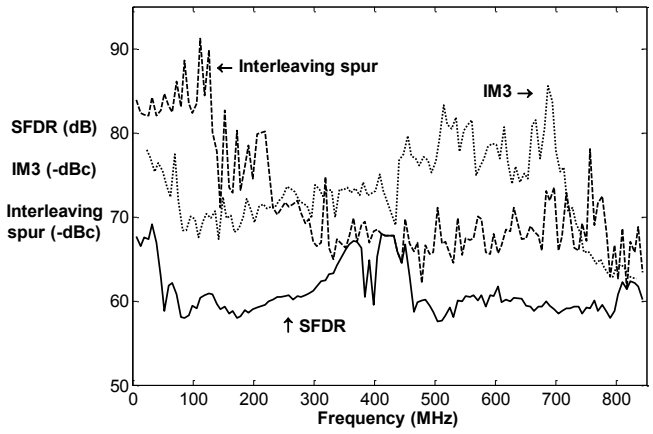

Figure 5: Spectral performance at 1.7GS/s

Fig. 6 shows the spectrum for an output frequency of 604MHz at a sample rate of 1.7GS/s. The figure shows that the HD3 is dominant, and that performance is not limited by the interleaving spur.

In order to demonstrate the performance improvement achieved by interleaving, the performance of an individual sDAC was measured without interleaving. In Fig. 7 the IM3 of an sDAC is plotted against the IM3 with interleaving enabled. Since the sDAC runs at only 850MS/s its performance rapidly drops above 425MHz, but also for lower frequencies it performs far worse than the complete interleaved DAC system.

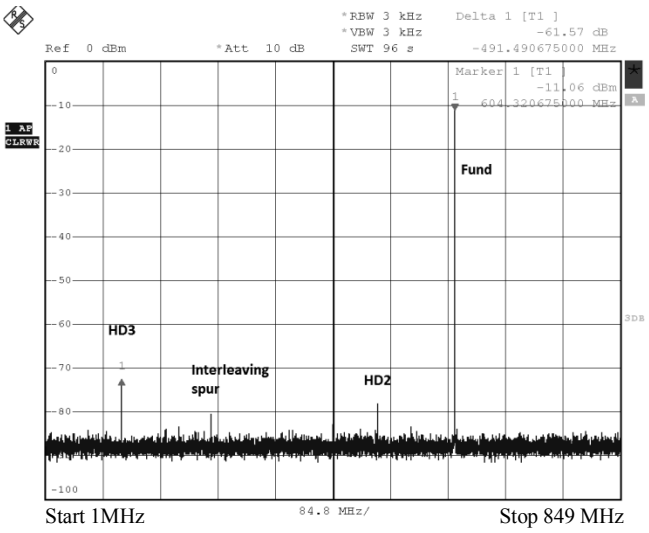

Figure 6: Spectral plot with an output frequency of 604MHz at 1.7GS/s

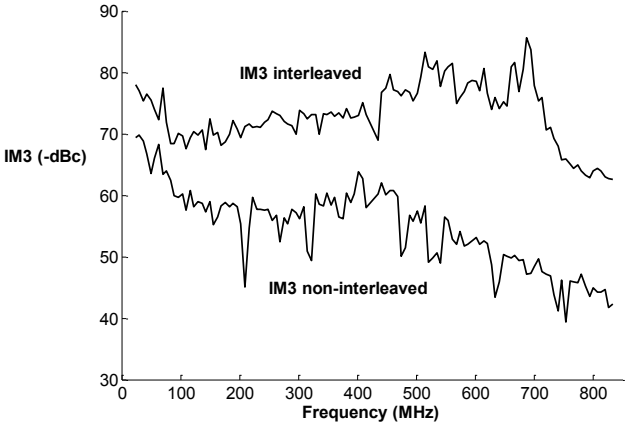

Figure 7: IM3 behavior with interleaving enabled and disabled at 1.7GS/s interleaved, 0.85GS/s non-interleaved

This also shows that compared to a non-interleaving DAC the area and power budget does not need to be doubled, since high performance can be achieved with two sDACs that only have moderate performance.

C. Low voltage operation

The interleaved DAC circuit was designed to operate at 1.2V, and shows only a graceful degradation of performance with lower supply voltages. The median SFDR drops by around 5dB when the supply voltage V_{supply} is lowered from 1.2V to 1V. Note that we use a resistive load, without the customary RF chokes that would lift the DC level of V_{out} to V_{supply}; consequently the actual voltage at the outputs gets as low as respectively 950mV and 750mV with 500mVpp-diff swing.

IV. CONCLUSIONS

A high speed interleaving DAC is presented that runs at 1.7GS/s at low supply voltages while achieving an SFDR across Nyquist that is better than previous non-return-to-zero DACs and does not have the higher clock jitter sensitivity and filtering requirements inherent to an RZ DAC. This interleaving DAC retains the advantages of conventional current steering DACs while the interleaving spurs that may occur when improperly interleaving are effectively suppressed using calibration of the DNL of one sub-DAC, calibrating the difference between the INLs of both sub-DACs to zero and calibrating the timing error to around 210fs.

TABLE I. COMPARISON TABLE

	This	**[1]**	**[2]**	**[3]**	**[9]**
Tech	65nm	180nm	65nm	40nm	65nm
Resolution [Bits]	12	14	12	12	9
Power [mW]	70	<600	188	40	60
V_{supply} [V]	1.2	-1.5/1.8	1.2/2.5	1.2	1.2
Area [mm^2]	0.4	4	0.825	0.016	0.04
Swing [$V_{pp\text{-}diff}$]	0.5	1.0	2.5	0.8 (RZ)	0.4
Fs [GHz]	1.7	3	2.9	1.6	3
SFDR[a] [dB]	58	52	52	70	49
IM3[a] [dBc]	-62.5	-65	-61	-70	-60
RZ	No	No	No	Yes	No
DEM	No	No	No	Yes	No

a. The worst-case SFDR/IM3 up to Nyquist/850MHz, whichever is lower

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