20.5 A 128f_s Multi-Bit ΣΔ CMOS Audio DAC with Real-Time DEM and 115dB SFDR

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Audio one-bit ΣΔ DA converters can have high resolution and low distortion. Switched-capacitor (SC) and continuous-time (CT) DAC's are comparable in performance, but the fault mechanisms and application issues are quite different. The Real-Time DEM algorithm presented here can only be used with CT DAC's. Those are limited in performance by clock jitter and inter symbol interference (ISI). Noise from clock jitter is proportional to the stepsize in the output signal and to the number of transitions. The stepsize and the oversampling rate will decrease if a CT multi-bit DAC is used, thus reducing the stepsize and the number of transitions. This reduces clock-jitter induced noise.

Smaller DAC stepsize also reduces the effect of ISI in two ways. Timing errors on small steps give less error charge, and correlation with the signal in the transition patterns can be reduced. However the static linearity of the multi-bit DAC must be very good, as it directly determines the large-signal distortion. To meet this demand dynamic element matching (DEM) techniques like data weighted averaging (DWA) are used to convert distortion introduced by the non-ideal DAC into a noise-shaped, out of signal band, error [1-3]. These DEM techniques require an additional digital block to scramble the unitary elements in the DAC. The scrambling easily results in repetitive patterns that give audible artifacts and increased noise in the audio band. Only complex scrambling [4] gives sufficient performance, but a small risk of audible artifacts will always remain. The real-time DEM DAC uses a new dynamic element matching algorithm that cancels the mismatch completely in a single sample unlike existing DEM techniques which only average the error asymptotically to zero with a number of samples. It also completely eliminates ISI.

Figure 20.5.1 depicts the system diagram of one channel of the dual DAC. The circuit has a I^2S input supporting all audio PCM sampling rates and a direct stream digital (DSD) input for Super Audio signals. The signals are upsampled to 128f_s and truncated by a 3rd-order 5-bit ΣΔ noise-shaper that prepares the data for the 5-bit DAC. The DAC has 32 well matched current sources and a digital block that takes care of the binary-to-thermometer code conversion and the rotation of this code for the DEM algorithm. This algorithm only allows 1 LSB change of the 5-bit DAC value. For a 128f_s 5-bit ΣΔ noise-shaper, this constraint has only a small impact on Dynamic Range. Matching of the 32 current sources is the starting point for DAC accuracy, but this only gives a 10 to 12 bit performance. The high switching speed of CMOS permits switching the current sources so that they all have an equal contribution to the output current within one sample period. This is shown in Fig. 20.5.2 for a 3-bit DAC. The thermometer code values '2', '3', '4' and '5' are not assigned to certain current sources for an entire sample period. Instead they are rotated over all sources resulting in phase-shifted PWM signals for individual sources. PWM signals that cross the sample period are adapted in length to the new sample value. Each phase one source is switched off and another source is switched on so the summed output current exactly behaves like a PCM signal, not considering matching errors. PWM signals have the advantage that the number of transitions is not signal dependent, so they are insensitive to ISI. In the 3-bit converter of Fig. 20.5.2, there are 8 phases in one sample period, and the timing of the 8 sources is shown. It can be observed that the order and distance of negative and positive transitions is dependent on the sample value and the source position, but within one sample period every source switches on and off exactly once. This reduces the effect of systematic errors in the rise and fall times of the current switches to a dc shift in the DAC current. The effects of non-ideal matching and phase timing can easily be estimated. The individual current sources are PWM modulated and have some distortion due to PCM-to-PWM conversion. As the summed currents show PCM behavior, this distortion apparently cancels out in the summing of the spectra of all sources. So the only distortion that remains is the mismatch part of a current that will still have a PWM character. This PCM-to-PWM distortion for a full scale 6.6kHz input signal at 128f_s/5.6MHz sampling frequency is –85dB [5]. So, if one of the 32 sources (-32dB) has a mismatch of 1% (-40dB), this will give a distortion contribution of –157dB. As mismatch of other sources wil add up in a random way, total distortion will be very low. Estimating the effect of a phase timing error starts with inspection of Fig. 20.5.2. During every clock phase one source is switched off, and another source is switched on. A timing error of 1% of the sample period, and 1% deviation in one of the current sources, give an error of $3x10^{-6}$ of the full-scale output current. In practice, timing and matching will be better, so sensitivity to phase clock noise and systematic timing errors is very low.

Figure 20.5.3 shows the circuit diagram of the DAC current switches. In the left part of the circuit, (FF/LS) are the data flipflop and the level shifter that connect the digital part with a 1.8V digital supply to the analog part with a supply voltage in the range 1.8 to 3.3 Volts. The circuit in Fig. 20.5.4 realizes optimal, limited swing, voltage drive conditions for the output current switches. For the whole range of supply voltages, the switches are operated with limited swing, so capacitive feedthrough and switching signals on the current sources are minimized.

The chip is made in a standard 0.18μm CMOS process with a 3.3 Volt thick oxide option. The chip area is $2mm^2$ including all digital signal processing. The total power consumption is approximately 150mW. Figure 20.5.5 shows –115dB distortion (full scale output including the external opamps) at an oversampling rate of 128 (5.65MHz sample clock, 181MHz phase clock). The distortion is hardly dependent on signal frequency, and the noise is -119dB (unweighted). Figure 20.5.6 gives an overview of the specifications.

References:

[1] R. Adams et al., "A 113dB SNR Oversampling Dac with Segmented Noise- Shaped Scrambling," *ISSCC Dig. Tech. Papers*, pp. 62-63, Feb. 1998.

[2] I. Fujimori et al., "A Multi-Bit ΣΔ Audio DAC with 129dB Dynamic Range," *ISSCC Dig. Tech. Papers,* pp. 152-153, Feb. 1999.

[3] R. Henderson et al., "Dynamic Element Matching Technique with Arbitrary Noise Shaping Function," *Proc. IEEE Int. Symp. Circuits Syst*., May 1996.

[4] X. Gong et al., "A 120dB Multi-bit SC Audio DAC with Second-Order Noise-Shaping," *ISSCC Dig. Tech. Papers*, pp. 344-345, Feb. 2000.

[5] M. Johansen et al., "A Review and comparison of Digital PWM Methods for Digital Pulse Modulation Amplifier (PMA) Systems," 107th AES Convention, Sept. 1999.

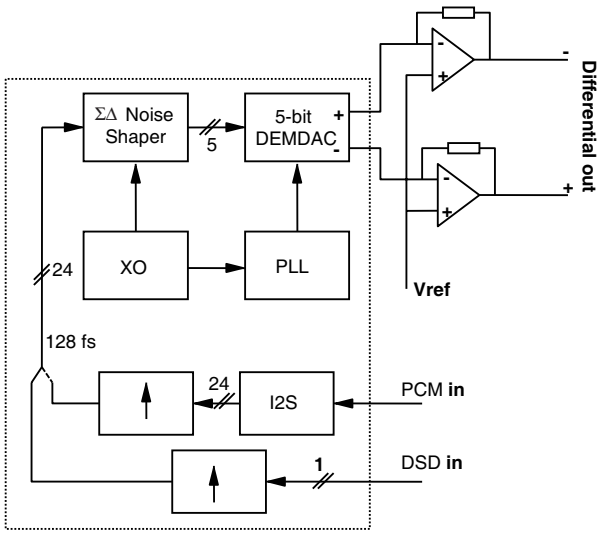

Figure 20.5.1: System diagram of the converter.

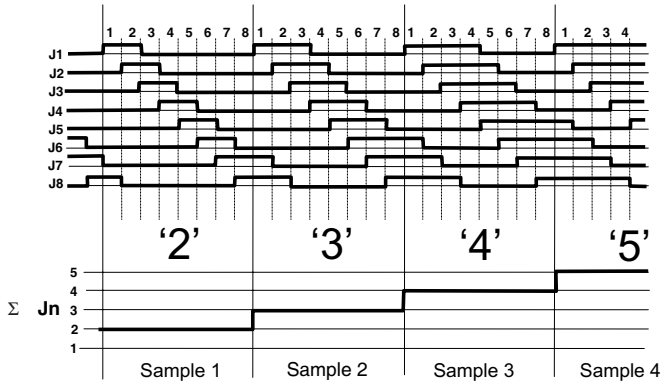

Figure 20.5.2: Switching diagram of the DAC current sources.

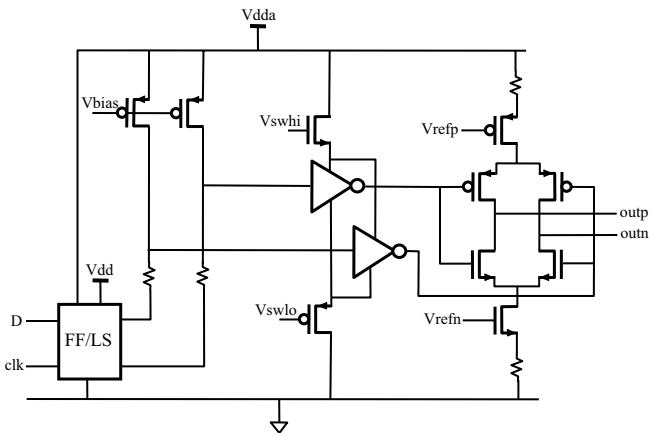

Figure 20.5.3: DAC current sources and driver circuits.

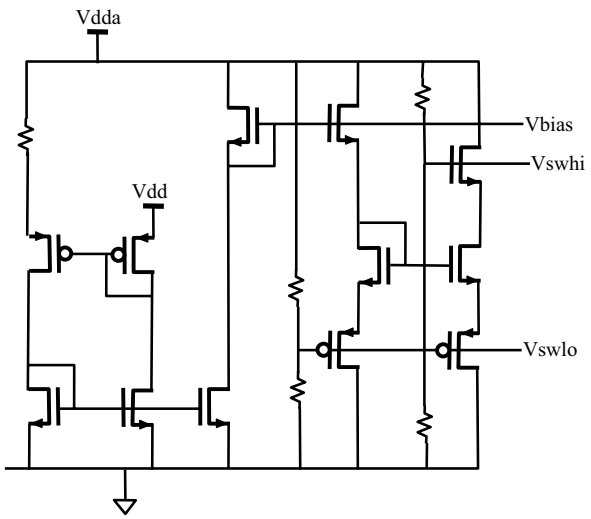

Figure 20.5.4: Supply adaptive biasing.

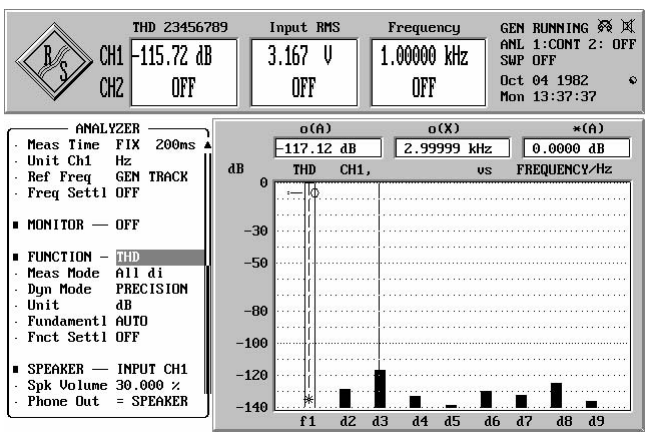

Figure 20.5.5: DA converter performance full-swing signal.

Analog supply voltage	1.8 – 3.3 V
Digital supply voltage	1.8 V
Total Power (supply Dig. 1.8V, An. 3.3V)	150 mW
SFDR 1 kHz output	- 115 dB
Noise (no input)	- 119 dB (unweighted)
Sampling frequency	128 fs, 5,6448 MHz
Chip Area analog + digital	2 mm^2
Process	0.18 um CMOS

Figure 20.5.6: DA converter performance summary.

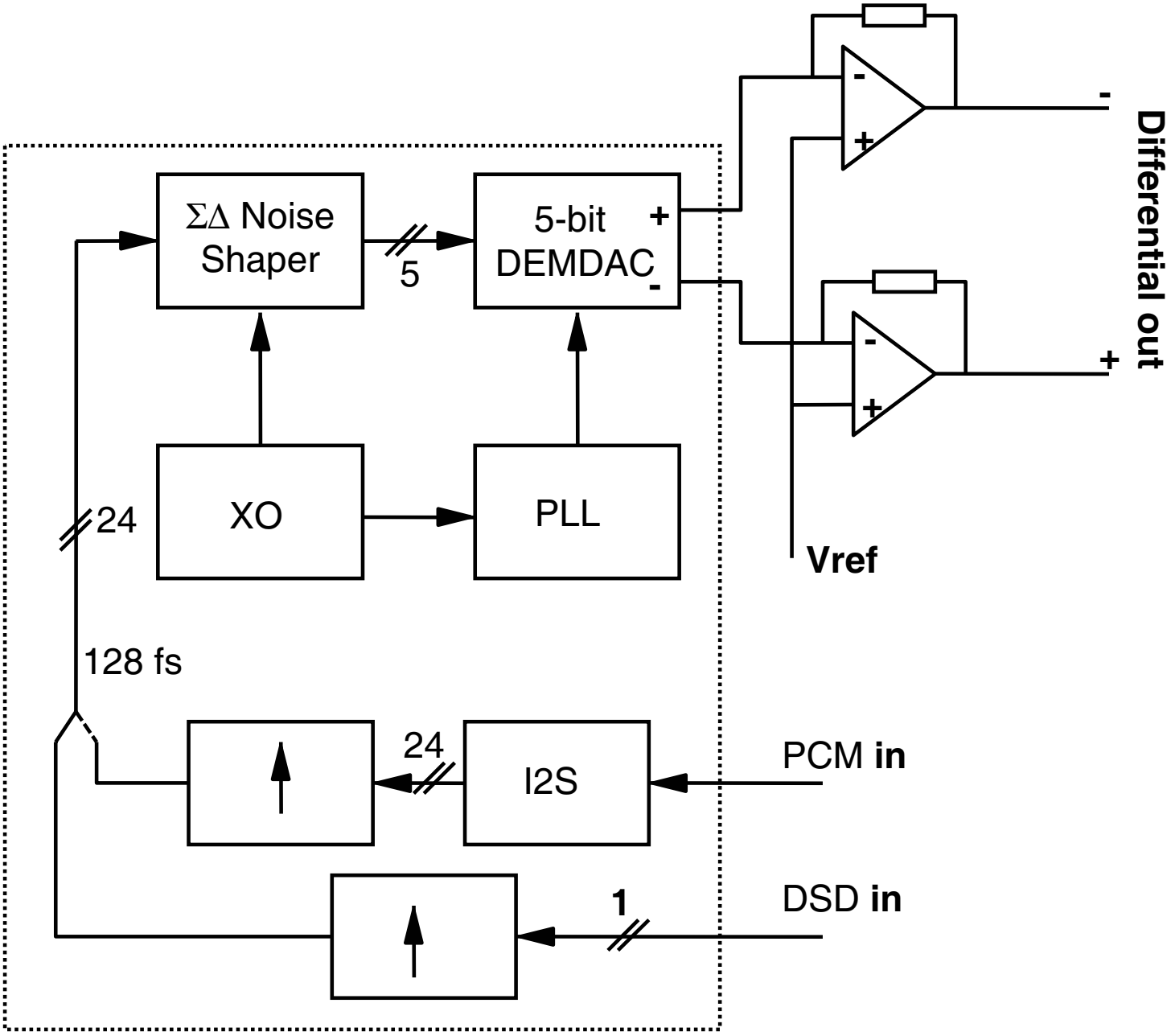

Figure 20.5.1: System diagram of the converter.

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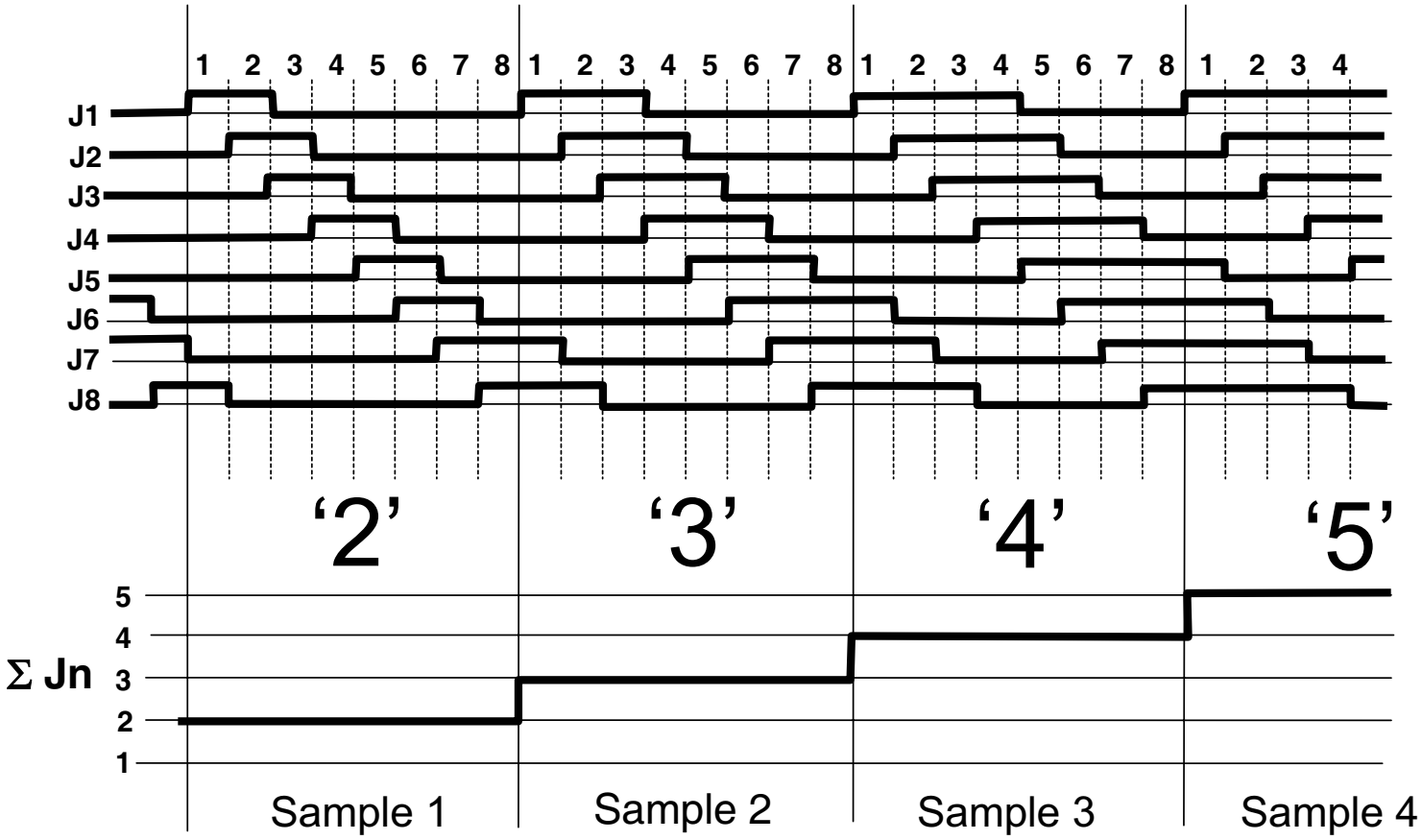

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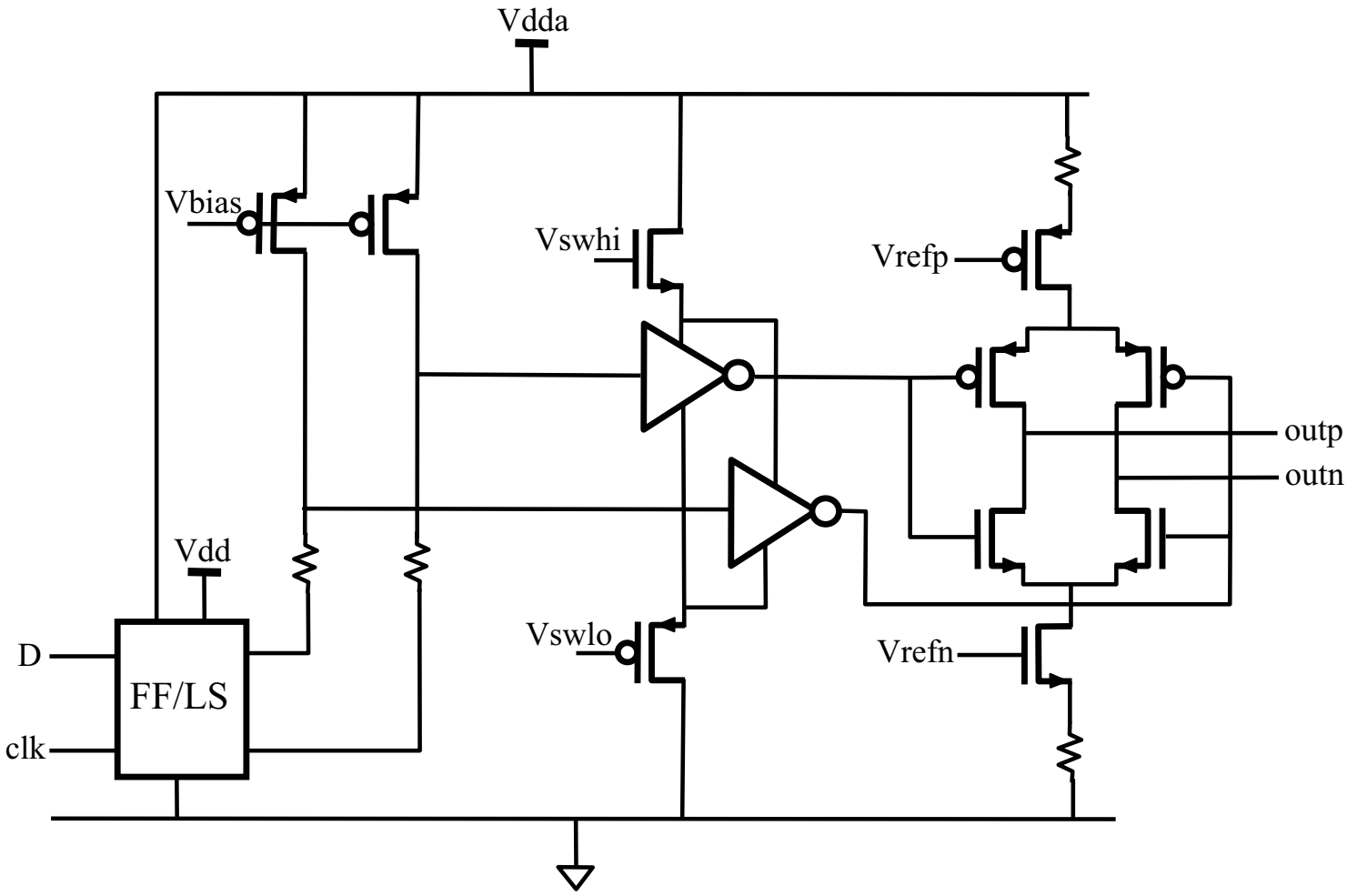

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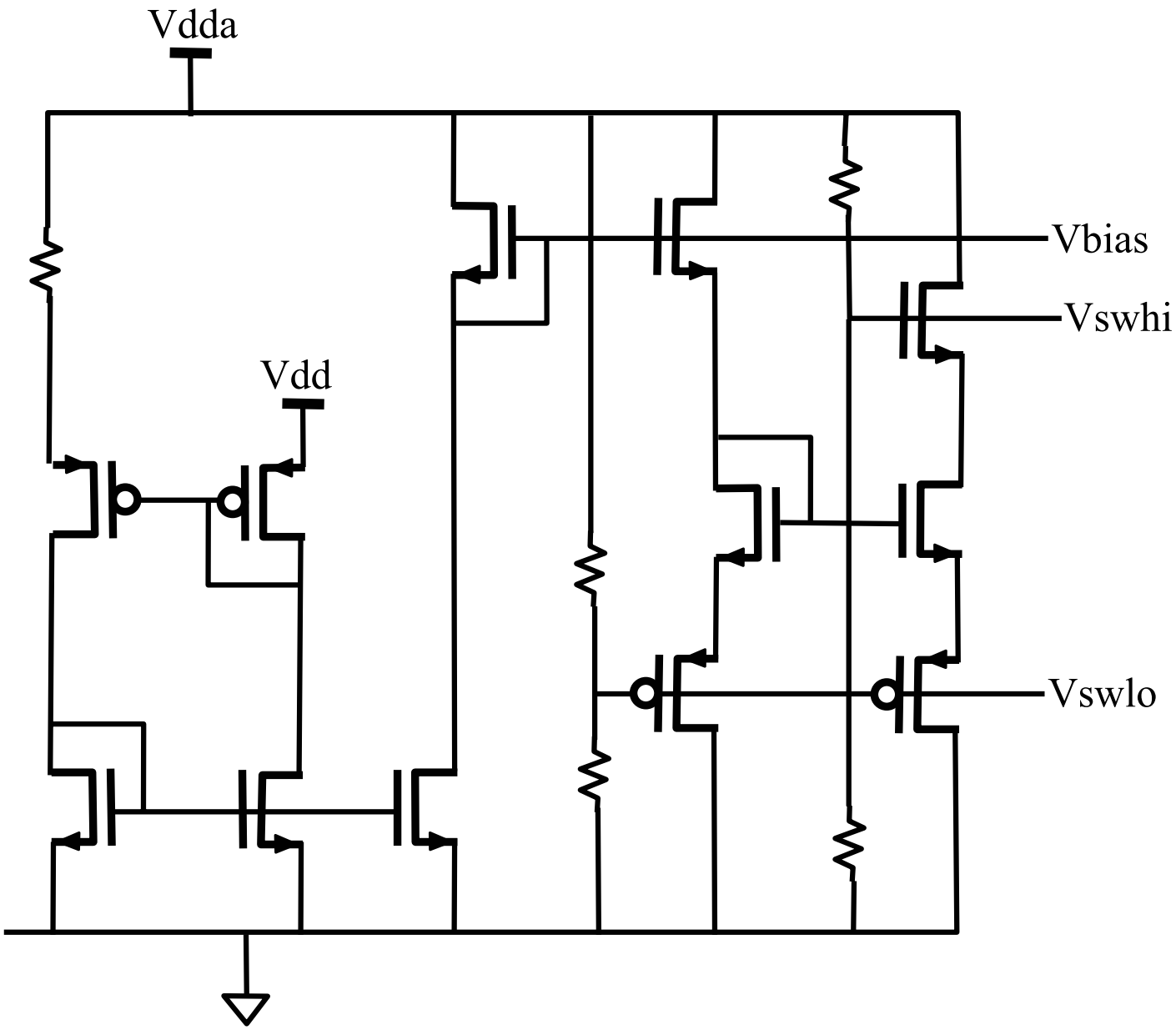

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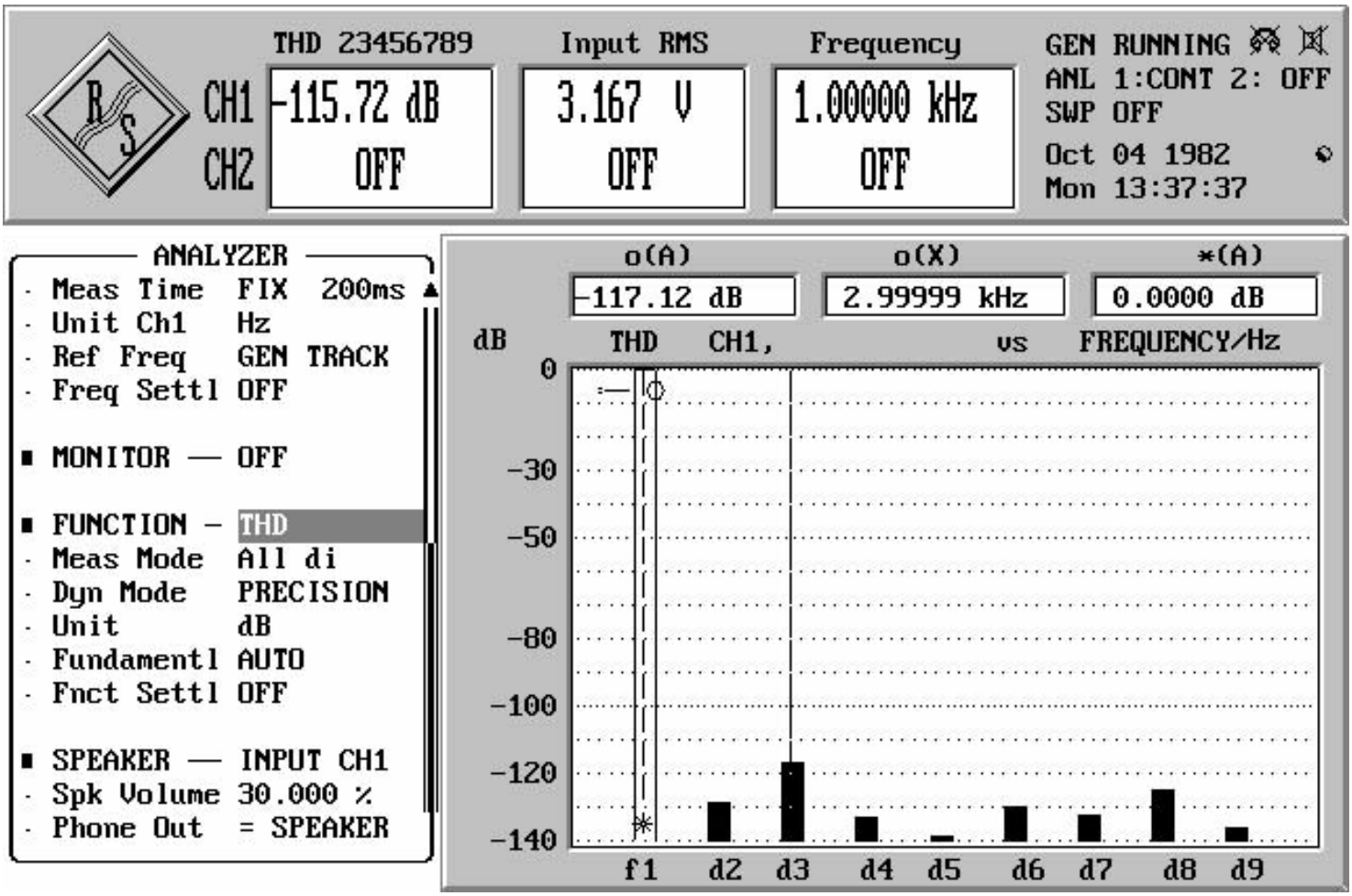

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