Multi-Band Linear Chirp Generation Based on a Type-III PLL

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***Abstract*—A type-III PLL is used to generate linear frequency ramps with 386 kHz RMS frequency error in L-band (3088 kHz in X-band) and 10% fractional bandwidth. Pulse durations can be as low as 10 µs without performance degradation. The system covers the L-, S-, C- and X-bands. A programmable output driver delivering −17.9 to +4.9 dBm differentially is included on chip. The system is fully integrated using a 250 nm SiGe BiCMOS process.**

***Index Terms*—Phase locked loops, Ultra wideband radar, BiCMOS integrated circuits,**

I. Introduction

Linear frequency ramps (chirps) are important for radar and imaging systems. A high bandwidth is necessary for a high range resolution [1]. For pulsed systems, a short chirp duration is needed to minimize the range below which no targets can be detected. This is because a short range corresponds to a short round trip time, hence a short pulse is required if the transmitter is to be deactivated when the echo is received. Flexibility in operating frequency is important, as lower frequency bands give a larger range and higher bands facilitate a larger bandwidth and thus a better resolution. Flexibility in output power can be helpful to taper an array aperture and to make sure the chip can be adapted to fit multiple systems with different drive power requirements. This paper presents a reconfigurable IC which can flexibly create very linear chirps in the commonly used L-, S-, C- and X-radar-bands. Apart from FMCW signals, this system is also capable of transmitting a single frequency ramp after which the output is powered off. The IC achieves chirps down to 10 µs in duration with 1 GHz chirp bandwidth and 3088 kHz RMS frequency error in X-band, or up to 125 MHz bandwidth with 386 kHz RMS error in L-band ($1/8^{\text{th}}$ of the BW and error in X-band). Through its single-chip nature, it opens the way to distributed radar transmitters.

This paper is divided into six sections. Section II describes the design on a system-level. Section III focuses on some circuit level aspects, with the first subsection discussing VCO design and the second subsection providing some details on part of the loop filter. Measurement results are discussed in section IV and a comparison with other work is made in section V. The final conclusions are treated in section VI.

II. System Overview

For flexibility reasons, we aim at frequency multiplication on a digitally created input chirp. Thus chirp speed and timing are digitally programmable. The challenge is to maintain a low RMS frequency error under such conditions. Frequency multiplication by N can be realized by an integer-N PLL. The block diagram of the proposed system is shown in fig. 1. The traditional structure of a PLL, consisting of a phase/frequency detector, filter, VCO and divider can be clearly distinguished. Additionally, there is a a second stage in the loop filter (GM, R_{F2} , C_{F3} and C_{F4}). Through this filter stage, a type-III PLL loop is created. Although we did not find designs exploiting such a PLL in literature, it is known from control theory that systems with one ideal integrator (type-I) can track a constant input with zero error. Increasing the type increases the order of the input signal which can be perfectly tracked. Since a PLL has phase as its input signal, a type-III PLL can track a signal with quadratic phase vs. time (a linear frequency chirp), with zero error, regardless of its sweep rate.

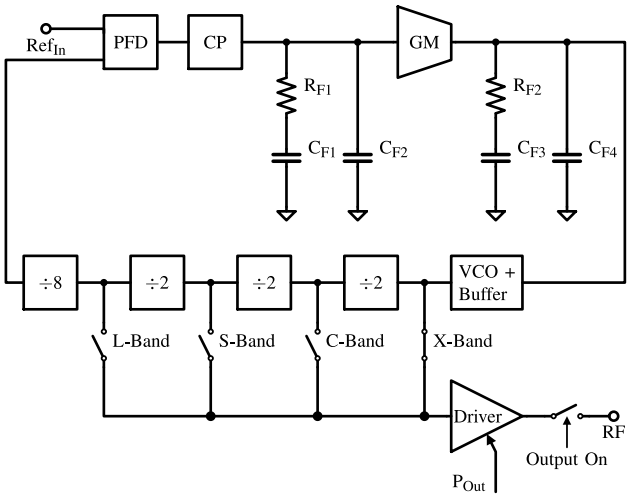


Fig. 1. IC Architecture

A set of switches at the input of the output driver can be used to connect either the VCO buffer or one of the dividers to the output driver. This way the system can create chirps in the different frequency bands mentioned earlier. The output driver can be set at 16 different output voltage levels on a linear scale. The output is designed to deliver a maximum output power of +6 dBm and a minimum of −18 dBm at the lowest frequency bands and produce a square wave like signal. At higher frequencies both the fundamental and the harmonics will be filtered by the bondwires and board capacitances, yielding a sine wave like signal at lower power.

The pulsed chirps are created by applying a signal at Ref_{in} at a frequency slightly below the start frequency of the chirp and starting the chirp slightly before the output is activated, to avoid the settling behaviour of the loop.

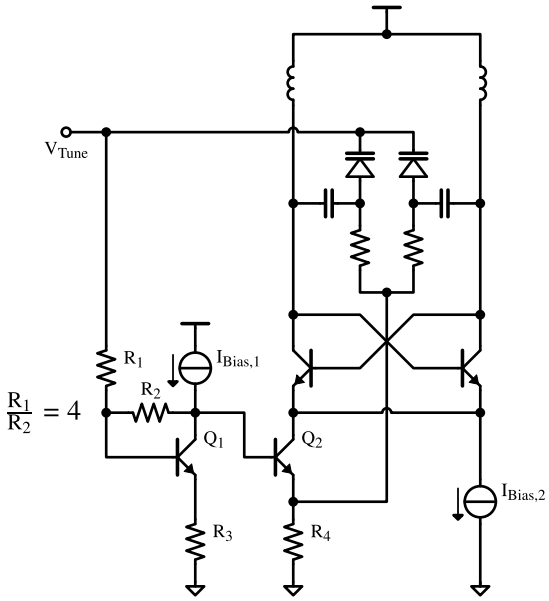


Fig. 2. Fast VCO Schematic

III. Circuit Level Aspects

A. VCO Design

An important circuit challenge in this system was to create a VCO that can be tuned over a wide enough range with available varicaps. In order to cover the entire X-band, two VCOs were used. One covers 7.2 to 10.1 GHz and the other covers 8.8 to 12.2 GHz. A third VCO could extend the maximum frequency to over 16 GHz, allowing full coverage from 0.9 to 16 GHz. However, this VCO was not added in this proof-of-concept. The overlap between the VCOs is more than 1 GHz to avoid VCO switching during a chirp.

Figure 2 shows the schematic of one of the VCOs. In this circuit, the tuning voltage is applied to an inverting amplifier, formed by R_1-R_3 and Q_1. This reduces the current trough Q_2 and R_4 as the tuning voltage increases, maintaining a fairly constant output amplitude and avoiding saturation of the BJTs in the subsequent (CML) stage. The voltage across R_4 is also used to increase the voltage across the varicap. Simulations show that this increases the tuning range by about 20%. The FoMs for both VCOs have been determined by simulation. Direct measurement is not possible because the phase noise and power of the VCOs cannot be measured directly. The traditional FoM for a VCO is calculated using (1) from [2].

$$FoM = L(\Delta f) - 20log\left(\frac{f_0}{\Delta f}\right) + 10log\left(\frac{P}{1mW}\right) \quad (1)$$

A frequently used variation of this FoM takes the tuning range of the VCO into account by adding an additional factor [3]. This FoM_T can be found in (2).

$$FoM_T = FoM - 20log\left(\frac{TR}{10}\right) \quad (2)$$

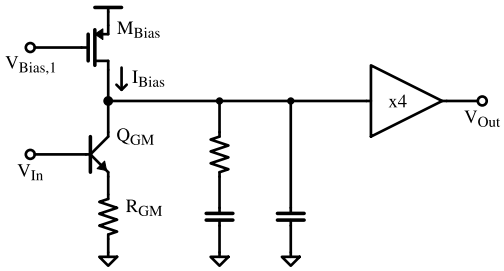


Fig. 3. Second Filter Stage Schematic

The simulations show a FoM_T of -181.8 dBc/Hz for both VCOs. This is comparable to, though not quite as good as, some designs that focus solely on VCO performance [3].

B. Second Filter Stage

A simplified schematic of the second filter stage, which turns the design into a type-III PLL, is shown in figure 3. As can be seen, its input consists of a transconductor created by Q_{GM} and R_{GM} which is biased by a constant current. This means that the circuit operates in class-A mode, where Q_{GM} is always on (the circuit would clip if Q_{GM} sinks more current than I_{Bias}). This was done to achieve a high bandwidth, operating the circuit in class-AB would require that the current through M_{Bias} can be varied. Because the available MOSFETs are relatively slow, and the process has no PNP devices, this would seriously impact the bandwidth of the circuit, compromising the phase margin. The gain stage in figure 3 consists of an operational amplifier with a resistive feedback network giving it a gain of 4. This was done to have an almost full scale voltage swing available at the VCO tuning node to maximise the tuning range. Without this gain stage the PMOS in the transconductor would go into triode for high tuning voltages and the bipolar device would go into saturation for low tuning voltages.

IV. Measurements

A chip micrograph of the IC, which was created in a 0.25 µm BICMOS process with a bipolar f_t of 140 GHz, can be found in fig. 4. The die measures 1.5 mm by 2 mm.

The functionality of the chip has been verified by applying three reference signals and measuring the frequency versus time behaviour. All three reference signals result in a center frequency of 11.5 GHz and a pulse duration of 10 µs, but the bandwidths differ. The first two signals are chirps with bandwidths of 1 GHz, and 100 MHz, the third has a constant frequency. Measurements have been performed by configuring the chip for L-band mode (see fig. 1) and measuring the output directly using an oscilloscope. This yields signals around 1437.5 MHz with bandwidths of 125, 12.5 and 0 MHz respectively. The signals were averaged 16 times to reduce quantization noise and band pass filtered using a filter with 60 dB out of band suppression and a passband between 1 and 2 GHz. The results, which can be found in fig. 5 show that the frequency error does not visibly change with chirp rate.

TABLE I
COMPARISON TABLE

Type	[4] FMCW	[5] FMCW	[6] FMCW	[7] FMCW	[8] FMCW	This Work Pulsed	
Technology	65 nm CMOS	90 nm CMOS	65 nm CMOS	SiGe Bipolar[a]	Board	250 nm BiCMOS	
Active Area	1.05	6.8	1.7	3[a]	?	3	mm^2
Supply Voltage	1.2	1.2	1.2	5[a]	?	2.5	V
Power Consumption	188[b]	406[b]	152	488[a]	?	380[c]	mW
Output Frequency	75.6 to 76.3	78.1 to 78.8	82.1 to 83.8	67.2 to 92.8	76 to 78	7.2 to 12.2 divided by 1, 2, 4 or 8	GHz
Chirp BW	0.7	0.7	1.5	25.6	2	1[d]	GHz
Fractional Bandwidth	1.3	1.3	2.3	32	2.6	10	%
RMS Frequency Error	<300[e]	1050[e]	180	?	?	3088[d]	kHz
Chirp Time	0.5[f,g]	0.25[f,g]	0.5 to 5[f]	4[f]	1[f,g]	$\geq$ 0.01	ms
Output Power	5.1	−2.8	?	−3 to −1	10	−17.9 to 4.9	dBm
Phase Noise @ 1 MHz	−85.3	−85	−84	−90	?	−86.0 to −81.4[d]	dBc/Hz

[a] Core IC; requires external ICs [b] Syntesizer + TX [c] Max power, CW Mode [d] In X-band [e] Including turn-around points [f] Only increasing freq. part [g] Lowest value reported

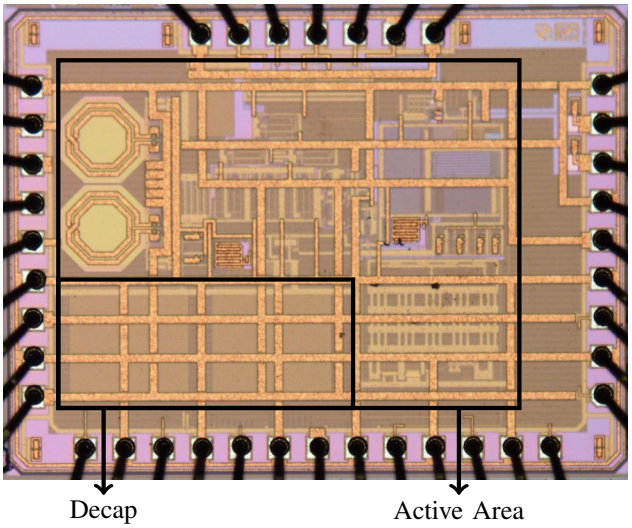
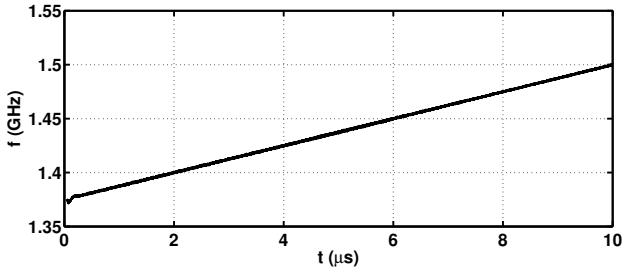
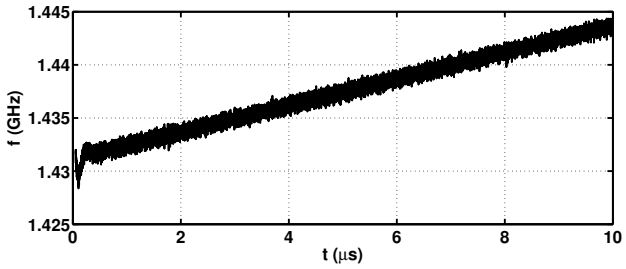


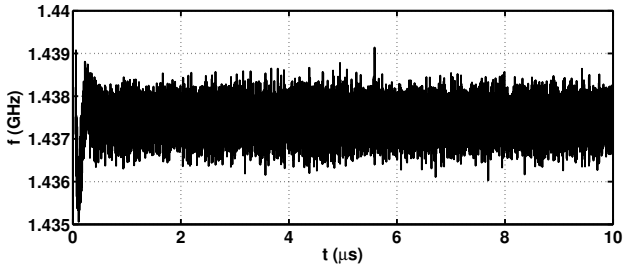
Fig. 4. Chip Micrograph



(a) 125 MHz in 10 μs



(b) 12.5 MHz in 10 μs



(c) Constant Frequency

Fig. 5. Frequency vs. Time

Figure 6 also shows the frequency error of the widest chirp (125 MHz) with respect to an ideal chirp. The RMS frequency error of both chirps is 386 kHz and that of the constant frequency is 391 kHz, which confirms the independence of frequency error and chirp rate.

The frequency error in higher bands cannot be measured directly using available equipment, but since lower bands are obtained by dividing the output, the error in X-band is expected to be eight times higher than that at L-band, which is 3088 kHz. The measurements show a short transient, which is caused by powering up the output driver, at the start of the chirp. This transient was ignored for the frequency error calculation.

As the system corrects for any frequency error at every reference edge, the frequency error will result in reference spurs. Therefore, spur reduction will improve the performance for every chirp rate. The spurs in this design are at −50 dBc to −58 dBc in L-band and −40 dBc to −45 dBc in X-band. An improvement is expected with a redesign of the charge pump.

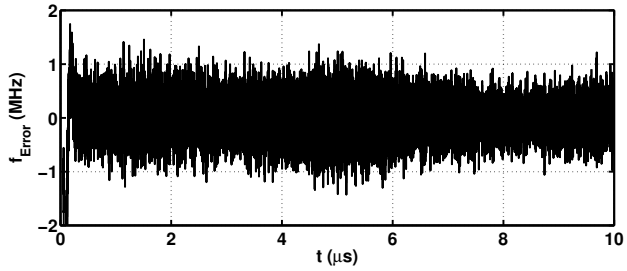


Fig. 6. Frequency Error

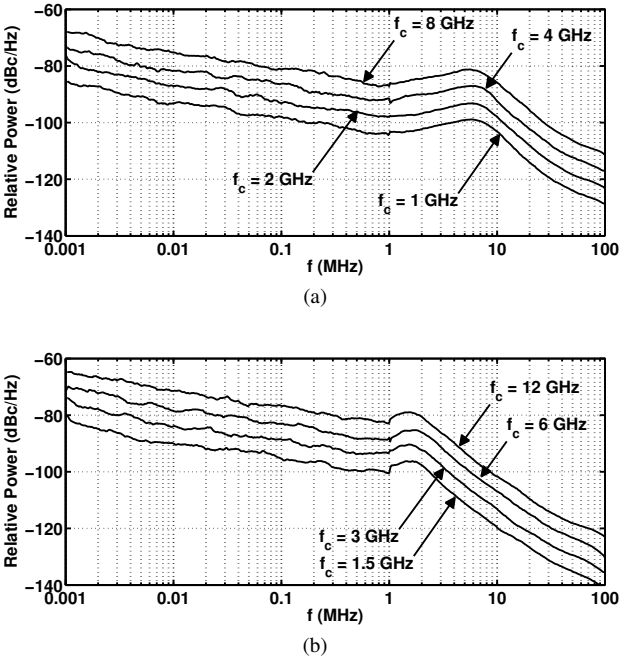


Fig. 7. Phase Noise

Figure 7 shows the phase noise of the system at each output band. Because the bandwidth of the system is so large, two plots are depicted here. Figure 7a depicts the phase noise of the slow VCO with the output frequency set at 8 GHz, fig. 7b shows the phase noise of the fast VCO at 12 GHz. The difference between these plots can be explained by the fact that the fast VCO is more noisy than the slow VCO, but also by the difference in VCO gain for the given frequencies. This gain influences the loop dynamics, which explains the difference in cut-off frequency which is clearly visible.

The relatively high phase noise at 1 MHz is also expected to be improved with a charge pump redesign. Due to the low 1/f corner of the bipolar devices, the phase noise is relatively low at small offset frequencies, which reduces range and Doppler inaccuracies. Furthermore, it allows for longer integration times and is hence beneficial for detecting slow-moving objects.

The output power was measured at -17.9 to $+4.9$ dBm in the lowest bands, dropping to -22.6 to -0.7 dBm at 12 GHz. The output power is slightly lower than predicted because in practice it will not be an ideal square wave.

V. Comparison to Other Work

As the authors are not aware of previous publications of pulsed systems with this level of integration on silicon, a comparison is made with several FMCW systems. The real benefits, however, are present for fast-chirping pulse-Doppler systems. This comparison can be found in table I. As can be seen, the frequency error can be improved upon, but the chirp rate is by far the highest reported. Fractional bandwidth is surpassed only by [7], which has a far lower level of integration than this work.

VI. Conclusions

A flexible system for the generation of pulsed linear frequency chirps has been presented. The system is capable of operation in L-, S-, C- and X-bands and achieves an RMS frequency error of 3088 kHz for a 1 GHz chirp in 10 μs at X-band. Due to the frequency multiplication in the system, the reference signal can be generated at low center frequency and bandwidth, allowing for digital generation.

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References

[1] M. Skolnik, *Introduction to Radar Systems*, McGraw-Hill, 2008.
[2] P. Baltus, et al., "A 3.5-mW, 2.5-GHz diversity receiver and a 1.2-mW, 3.6-GHz VCO in silicon on anything," *IEEE J. Solid-State Circuits*, vol. 33, no. 12, pp. 2074-2079, December 1998.
[3] Q. Wu1, et al., "A 10mW 37.8GHz Current-Redistribution BiCMOS VCO with an Average FOMT of -193.5dBc/Hz," *ISSCC Dig. Tech. Papers*, pp. 150-151, February 2013.
[4] Y. Li, et al., "A Fully Integrated 77GHz FMCW Radar System in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 216-217, February 2010.
[5] T. Mitomo, et al., "A 77 GHz 90 nm CMOS Transceiver for FMCW Radar Applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 928-937, April 2010.
[6] H. Sakurai, et al., "A 1.5GHz-Modulation-Range 10ms-Modulation-Period 180kHz RMS-Frequency-Error 26MHz-Reference Mixed-Mode FMCW Synthesizer for mm-Wave Radar Application," *ISSCC Dig. Tech. Papers*, pp. 292-294, February 2011.
[7] N. Pohl, et al., "An Ultra-Wideband 80 GHz FMCW Radar System Using a SiGe Bipolar Transceiver Chip Stabilized by a Fractional-N PLL Synthesizer," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 3, pp. 757-765, March 2012.
[8] C. Pfeffer, et al., "An IQ Modulator Based Heterodyne 77-GHz FMCW Colocated MIMO Radar System," *MTT Digest*, pp. 1-3, June 2012.