An Integrated 80-V Class-D Power Output Stage with 94% Efficiency in a 0.14µm SOI BCD Process

Haifeng Ma, Ronan van der Zee and Bram Nauta
IC Design Group
CTIT Research Institute, University of Twente
Enschede, The Netherlands

***Abstract*—In this paper we present a highly-efficient 80V class-D power stage design in a 0.14µm SOI-based BCD process. Immunity to the on-chip supply bounce is realized by internally regulated floating supplies, variable driving strength for the gate driver, and an efficient 2-step level shifter design. Fast switching transition and minimized switching loss are achieved with a 94% peak efficiency in the realized chip.**

I. INTRODUCTION

Piezoelectric actuators are increasingly adopted in a wide range of applications like smart materials for vibration and noise control, precision actuators, etc.[1]. In these applications, signal frequency is in the range of several tens to hundred Hz and the piezoelectric actuator can be electrically treated as a capacitive load. The higher efficiency offered by class-D power amplifiers compared to class-AB makes them ideal for driving such loads, where typically several tens of Watt reactive power are being processed and the compactness requirement mandates the usage of small or even no heat sinks.

Integrated high-voltage high-power class-D output stages for audio are discussed in [2-5]. One significant design problem of such switching power stages is the on-chip supply bouncing [2], [6]. The output current switching between the high-side and low-side power switches (Fig. 1) causes large di/dt and in turn on-chip supply bouncing caused by parasitic inductances. For high-voltage DMOS output devices, the maximum allowed gate-source voltage (V_{gs}) is the same as for normal MOS devices in the same process node and is much lower than their maximum drain-source voltage (V_{ds}). The trend to integrate more and more signal processing and features on the same chip as the power blocks necessitates the power stage design in deep-submicron process nodes. The supply bouncing magnitude of several volts, while not yet a problem in [2-6], makes the design in these smaller process nodes prone to performance degradation or even malfunction.

In this paper we present a gate driver topology that overcomes the supply bouncing issue and enables a high-voltage, high-power class-D power stage design in a deep-submicron process node. This is accomplished by 1) Gate drivers featuring an on-chip regulated floating supply voltage, 2)In-cycle variable gate driving strength to reduce bounce and 3) a power-efficient 2-step level shifting circuit that can handle supply bounce higher than the supply voltage of the low-voltage control circuits.

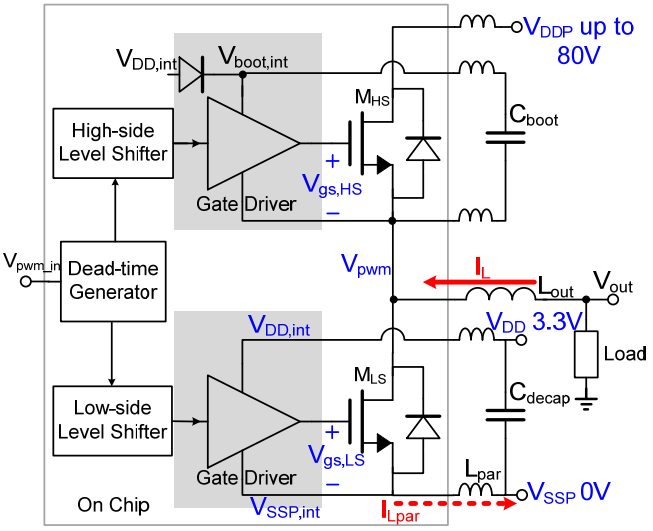

Fig. 1. Typical high-voltage and high-power class-D power stage topology

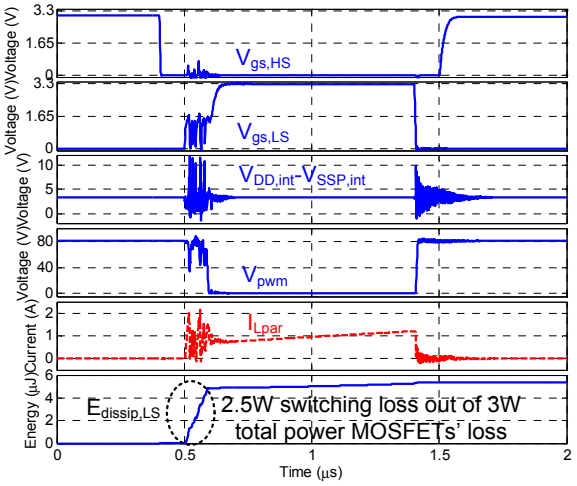

Fig. 2. Simulation waveforms of the power stage in Fig. 1, V_{pwm} high-to-low transtion interupted by the supply boucing and resulting in high switching loss

II. FLOATING GATE DRIVER TOPOLOGY

A. Supply Bouncing Issue

A typical class-D power stage for high-voltage high-power applications consists of two identical nDMOS devices as high-side (HS) and low-side (LS) switches configured as shown in

Fig. 1 [2-4]. Since for DMOS devices the maximum V_{gs} is typically much lower than the maximum V_{ds} , the LS gate driver is supplied by a separate low-voltage supply and externally decoupled. For the HS gate driver, an external bootstrapping capacitor is used as the supply. For each of these externally decoupled supplies, parasitic inductances exist between the on-chip power supply pads and the decoupling capacitors through bond wires, lead fingers, and PCB traces, which can easily added up to tens of nano-Henrys [2].

The on-chip supply bouncing happens when the load current is switching between the two power switches. Consider the case when the load current is flowing into the power stage as shown in Fig. 1 and the simulation waveforms as shown in Fig. 2. As the initial condition, the HS DMOS power transistor M_{HS} is on and the V_{pwm} node is staying near V_{DDP}. After M_{HS} is turned off, the switching transition begins when the LS DMOS power transistor M_{LS} is trying to turn on and take over the load current. A sudden increase of current flowing through M_{LS} will cause the on-chip $V_{SSP,int}$ node to rise while the gate driver positive supply $V_{DD,int}$ stays because of the external decoupling. The combined effect is that the on-chip gate driver supply becomes too small, affecting the switching transition behavior. As illustrated in Fig. 2 with a modeled parasitic inductance L_{par} of 10nH, a sudden increase of $I_{L,par}$ causes the internal $V_{DD,int}$-$V_{SSP,int}$ to bounce with a magnitude higher than the 3.3V low-voltage supply itself. The LS DMOS transistor turn-on process is interruptedly repeatedly by this process. There is significant switching loss in M_{LS} because it will see the high supply voltage V_{DDP} across it while conducting the load current during this oscillatory transition. In the example shown in Fig.2, out of the 3W total loss (including conduction loss), 2.5W is caused by just this transition.

One straightforward way to limit the influence of the supply bouncing is to carefully control the turn-on speed of the output power DMOS. However, with a 3.3V gate driver supply voltage, this means that the turn-on should be excessively slow to keep the bouncing within a safe margin. High switching loss must be traded off against a well-behaved switching transition.

B. Supply-Regulated Floating Gate Driver

To overcome the on-chip driver supply bouncing issue without sacrificing on the efficiency during switching transitions, a gate driver topology with on-chip regulated floating supply is proposed in this paper. As shown in Fig. 3(a), two on-chip voltage regulators are used to provide stable on-chip supply voltages to the gate driver circuits. The two regulators will track the two reference nodes $V_{SSP,int}$ and V_{pwm} respectively, so the on-chip bouncing will not be seen by the driver circuits. The unregulated input supply voltage for the regulators are chosen based on the estimated maximum bouncing magnitude plus their minimum operation voltage (12V unregulated V_{DD} is used here). The detailed gate driver circuit is shown in Fig.3 (b). The pull-up current has been divided into two parts. The main I_{pu} is supplied by the unregulated V_{DD} while an auxiliary I_{pu} is used to turn the output power transistor fully on. By this configuration the regulators are not required to supply the hundred milliamps I_{pu} and their design can be simplified. For the pull-down current path, a supply-bouncing minimization circuit is implemented and will be explained later.

A robust and efficient switching transition as shown in Fig. 4 is achieved by this gate driver topology. The turn-on of the LS power transistor can be fast without disturbing the internal gate driver supply too much.

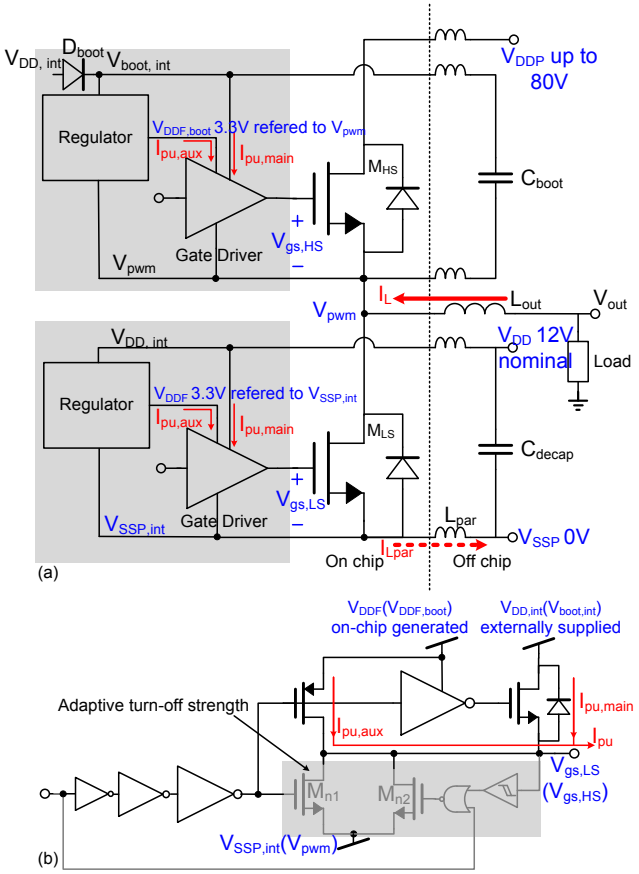

Fig. 3. Proposed power stage topology (a) supply bouncing influnce on the functinality of the gate driver is eleminated by the on-chip regulatred gate-driver supply (b) Detailed gate driver structure.

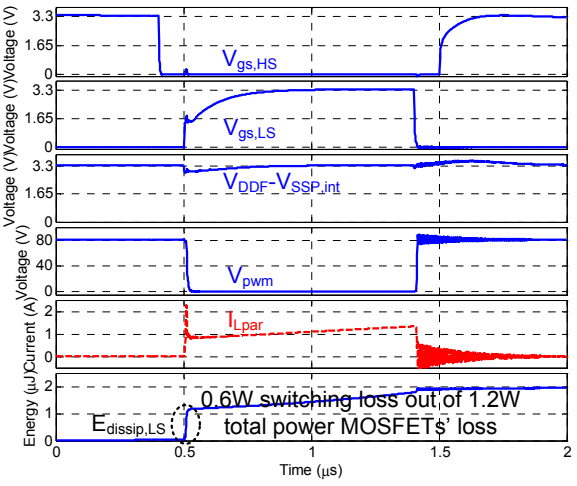

Fig. 4. Simulation waveforms of the power stage in Fig. 3, V_{pwm} high-to-low fast transition is achieved without getting interrupted by the supply bouncing. Switching loss is kept at minimum.

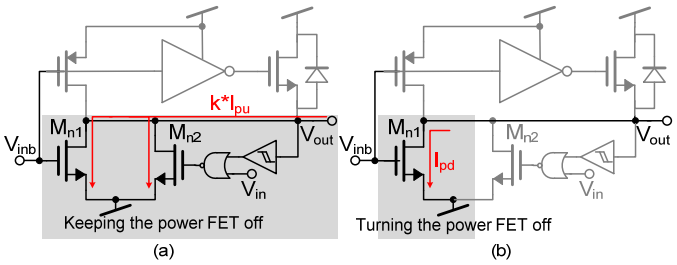

Fig. 5. Gate driver with adaptive turn-off strength (a) Stronger pull-down transistors for keeping the power transistor off (b) Weaker pull-down transistors for turning the power transistor off

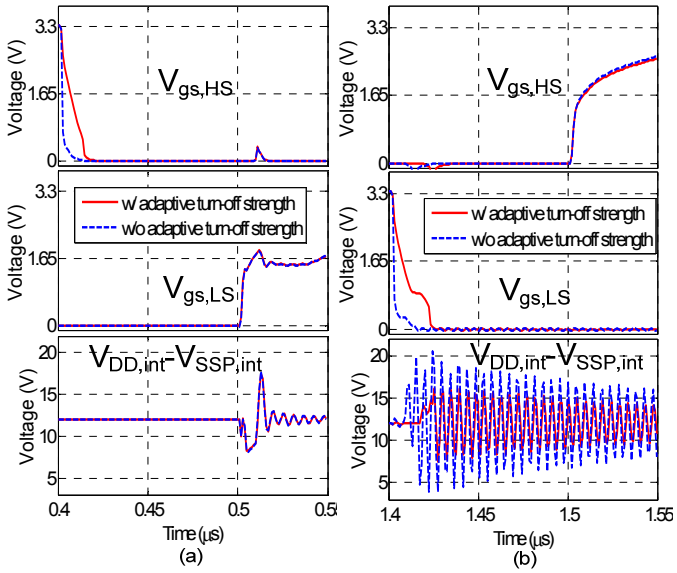

Fig. 6. Simulation waveforms for the on-chip supply bouncing with and without the adaptive turn-off strength (a) When one power transistor turns on, the other power transistor can be kept off (b) On-chip supply bouncing can be significantly minimized when turning the transistor off with less strength compared with that for keeping it off

C. *Supply Bouncing Minimization*

Although the gate driver circuits are now largely immune to supply bouncing, it is still desirable that the bouncing can be minimized for robust operation of the regulator circuit as well as for electro-magnetic interference considerations. As has been discussed in [3], the gate driver pull-down current for turning the power transistor off has to be much stronger than the pull-up current for turning it on in order to avoid cross conduction of the HS and LS power transistors during the output voltage transition. This means that the turn-off action can cause larger di/dt and thus larger supply bouncing than the turn-on action. To minimize the bouncing caused by this, adaptive turn-off strength has been used in the driver pull-down current path.

As shown in Fig. 5(a), when the driver input and output status have all been detected as already off, the combined strength of M_{n1} and M_{n2} will be used to keep its output off when the other driver is turning on based on the pull-up/pull-down current ratio requirement. However, when the driver is in the process of turning its output off and haven't yet reached the level determined by the Schmitt trigger, only the weaker M_{n1} will provide the pull-down current for turning off the output power transistor in order to keep di/dt low. Simulation waveforms for comparing the effectiveness with and without the adaptive driver turn-off strength are shown in Fig. 6. Fig. 6(a) shows that the same effect for keeping the power transistor off is obtained while Fig. 6(b) illustrated that the supply bouncing is significantly reduced when a weaker pull-down strength can be applied for turning the power transistor off.

D. *On-chip Floating Voltage Regulator*

The on-chip floating regulator circuit for both HS and LS usage are shown in Fig. 7. For fast response and low output voltage ripple, the output $V_{DDF}/V_{DDF,boot}$ has been excluded from the feedback loop [7]. The drawback on precision is not critical here since it's mainly digital signals processed in the gate driver blocks they supply. The output devices of the regulator are also DMOS devices to sustain the higher 12V V_{DD} as well as the bouncing superimposed on it.

On-chip decoupling capacitor C_G is important for power supply ripple rejection. Furthermore, it is important to minimize its parasitic capacitance $C_{par,sub}$ to the substrate as any disturbance from the V_{SSP}/V_{pwm} node will be coupled to V_B or V_{DDF} by a ratio $C_{par,sub}/(C_G+C_{par,sub})$. As an example, the output voltage V_{PWM} slews 80V in a few nanoseconds, even with 1% parasitic capacitance 0.8V will be couple to the 3.3V output, which is an unacceptable 25% variation. Consequently it is rather important that these decoupling capacitors are fully shielded from the substrate as shown in Fig. 7. Here for the metal fringe capacitor the whole fist metal plate is connected to the $V_{SSP,int}/V_{pwm}$ node such that V_B is fully shielded.

III. Power-Efficient 2-Step Level Shifter

Another important circuit block for the class-D power stage is the level shifter circuit. It is used for communication between signals referred to the digital ground V_{SSD} and those referred to the power ground $V_{SSP,int}$ or the floating HS V_{pwm}. As shown in Fig. 8, the supply voltage of the regulated gate driver supply V_{DDF} tracks $V_{SSP,int}$ and can be even lower than the digital ground V_{SSD} in the presence of bouncing. This makes direct level shifting referring to V_{DDF} not feasible. For reliable level shifting, a two-step approach has been adopted here, where the voltage level is first referred to the higher 12V $V_{DD,int}$ and then to $V_{SSP,int}$.

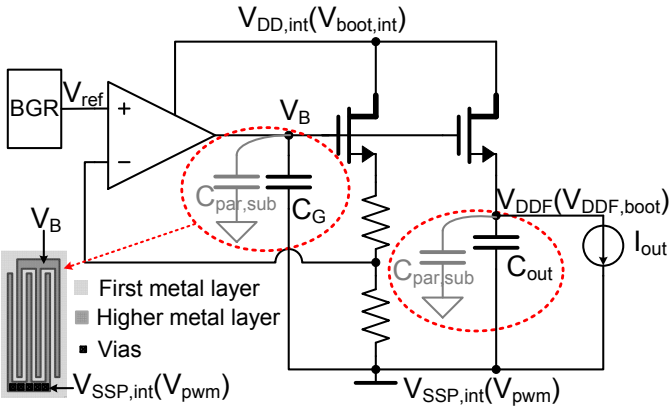

Fig. 7. On-chip regulator and its decoupling capacitor C_G implementation

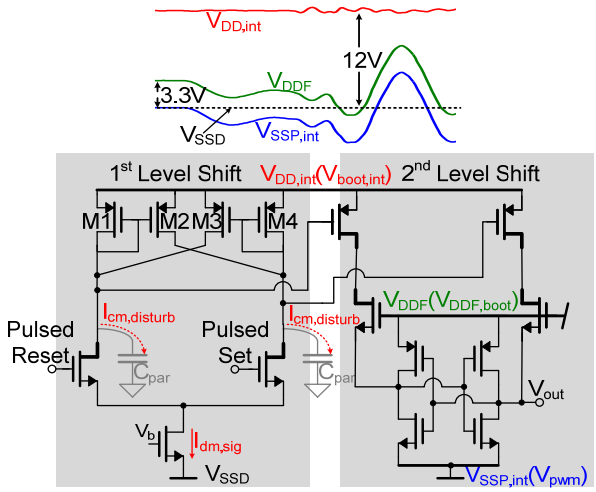

Fig. 8. Level shifter circuit and illustration of the on-chip supply/ground waveforms which necessitates a 2-step approach for the level shifting

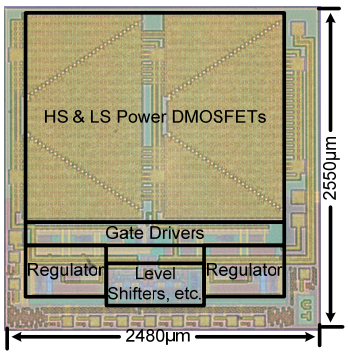

Fig. 9. Chip photograph of the 80V class-D power stage

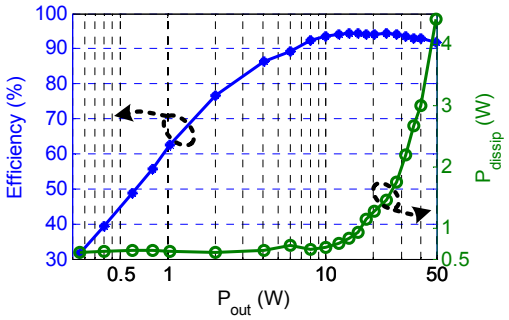

Fig. 10. Power efficiency and dissipation measurement results of the 80V output stage with 250kHz switching frequency.

For the HS level shifter circuit, the power dissipation could be significant because the current for transferring the signal has to flow between the 92V $V_{boot,int}$ and ground. Two approaches have been used to minimize its dissipation. Firstly, pulsed set and reset input are applied such that only pulsed current are bridging most of the 92V [8]. Additionally, we introduce an active load (transistors M1-M4) with partial positive feedback characterized by a lower impedance for common-mode disturbances like $V_{DD,int}$ or V_{pwm}, and a higher impedance for the differential-mode signal pulses. This way, significantly lower current pulses can be applied on the first level shifter for generating an effective output signal while maintaining its output immune to noise disturbance.

IV. Measurement Results

The 80V power output stage has been fabricated in NXP A-BCD9, a 0.14µm SOI-based BCD process and the chip photograph is shown in Fig. 9. For measuring efficiency, a current-source load instead of the capacitive piezoelectric load is used to make the power stage delivering active output power. For a fixed V_{pwm} duty cycle of 0.5 and switching frequency of 250kHz, the efficiency is shown in Fig. 10 with a measured 94% peak efficiency. For linearity measurement, the power stage within a hysteretic-based feedback loop can achieve THD+N below 0.1% for a 2kHz, 70V_{pp} sinusoidal output and a series-connected 2.2µF+3Ω modeling the piezo load[1].

Compared to other power stage designs, this design offers the best possibilities for integration with other mixed-signal functions thanks to the smaller process node being used, 0.14µm versus 0.35–3µm in [2-6]. This is permitted by the supply bounce immunity features, enabling its operation with a 3.3V V_{gs} other than 5-12V V_{gs} in [2-5] and 18V V_{gs}=V_{ds} in [6]. The supply bounce immunity also makes it compare favorably with respect to efficiency, which is >90% over almost a decade of output power variation.

V. Conclusions

Fast switching transitions are crucial for minimizing class-D switching losses. The introduction of regulated floating supplies, variable driving strength for the gate driver and a 2-step level shifter ensure fast switching transitions not disturbed by on-chip supply bouncing. A high-voltage, high-power class-D power stage with 3.3V V_{gs} is realized and measures with over 94% peak efficiency.

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