Global On-Chip Differential Interconnects with Optimally-Placed Twists

Eisse Mensink, Daniël Schinkel, Eric Klumperink, Ed van Tuijl and Bram Nauta

Abstract—**Global on-chip communication is receiving quite some attention as global interconnects are rapidly becoming a speed, power and reliability bottleneck for digital CMOS systems. Recently, we proposed a bus-transceiver test chip in 0.13 μm CMOS using 10 mm long uninterrupted differential interconnects of only 0.8 μm pitch. These small interconnects suffer from severe inter-symbol interference due to their high distributed resistance and capacitance. By using pulse-width equalization and low-ohmic termination, the inter-symbol interference is reduced and the achievable data rate is increased from 0.55 Gb/s/ch to 3 Gb/s/ch.**

Next to inter-symbol interference, the interconnects also suffer from crosstalk from neighboring interconnects. Analysis and measurements show that this crosstalk would impede the achievable data rate if it were not mitigated.

In order to cancel the crosstalk, one twist is placed in every even interconnect in the bus and two twists are placed in every odd interconnect in the bus. Analysis shows that there are optimal positions for these twists, depending on the termination of the interconnects. Theory and measurements show that only one twist at 50% of the even interconnects, two twists at 30% and 70% of the odd interconnects and equal source and load impedances are very effective in mitigating the crosstalk.

Index Terms—**Crosstalk, Data Bus, Interconnect, On-Chip Communication, Twists.**

I. INTRODUCTION

ON-CHIP communication is a field that is getting more attention, as (global) interconnects are rapidly becoming a speed, power and reliability bottleneck for digital systems [1]. In [2] we demonstrate a bus-transceiver test chip in 0.13 μm CMOS that uses 10 mm long uninterrupted differential interconnects of only 0.8 μm pitch (82 MHz RC-limited bandwidth) and achieves 3 Gb/s/ch. However, in [2] we do not analyze the twists that we use to cancel crosstalk. These twists are necessary, because due to small spacings (0.4 μm) and the 10 mm long parallel interconnects in the bus, there is a considerable amount of crosstalk. This crosstalk limits the achievable data rate if it is not mitigated.

Twists are also used in CMOS memory cells to cancel crosstalk between bitlines [3]. Recently, the use of twists in on-chip global interconnects was proposed [4]. They use eight
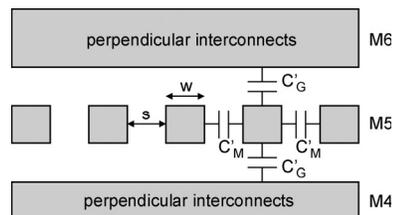
Fig. 1. Interconnect model.

evenly-spaced twists, but it appeared that via resistance was overlooked. In a recent paper [5], we show that only one twist in the even interconnects and two twists in the odd interconnects are sufficient. Furthermore, we show that the optimal positions for these twists depend on the termination of the interconnect. In this paper, we give a more detailed analysis and with the help of eye-diagram properties we show that a 2 times higher data rate is possible due to the twists.

In section II, the optimal positions for the twists, depending on the termination, are calculated. Section III shows measurement results from our test chip. Section IV gives conclusions.

II. OPTIMAL TWIST POSITIONS

A. Interconnect Model

Fig. 1 shows a model of the global bus (cross-section). The global bus is placed in metal 5 as we assume the top metal layer (metal 6) to be reserved for power and clock routing. Perpendicular interconnects in metal 4 and metal 6 are modeled by two metal plates.

The width (w) and spacing (s) are chosen for highest bandwidth per cross-sectional area: w = s = 0.4 μm [2]. For these narrow interconnects, the distributed resistance R' = 0.15 kΩ/mm and the total distributed capacitance $C' = 2C_G' + 2C_M' = 0.23$ pF/mm are simulated with a 3D EM-field simulator. The distributed inductance L' = 0.35 nH/mm only starts to dominate over the distributed resistance at a frequency of $R'/L'/(2\pi) = 68$ GHz. For 10 mm long interconnects, the attenuation at this frequency is very large (> 150 dB), so inductance does not play an important role.

The distributed capacitance between two interconnects, C_M' = 0.05 pF/mm, results in crosstalk (see Fig. 2): a signal from source V_S will not only appear at the output of the aggressor line (V_A), but also at the output of the victim line (V_V). The transfer functions $H_A = V_A/V_S$ and $H_V = V_V/V_S$ for 10 mm long interconnects are shown in Fig. 2 (low-ohmic R_S and
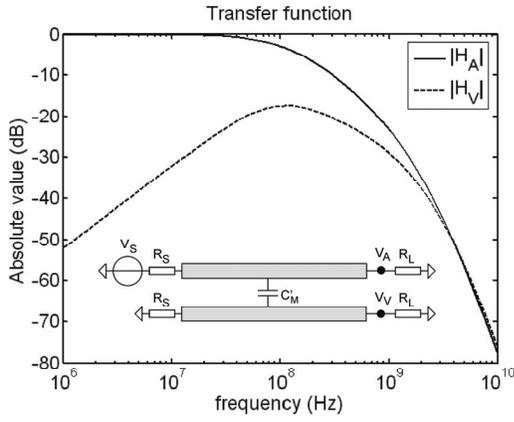
Fig. 2. Transfer functions of 10 mm long interconnects.

high-ohmic R_L, modeling an open or a small capacitive load).

The transfer functions of Fig. 2 show two properties of the interconnect: First, the interconnect has a limited bandwidth of only 100 MHz (82 MHz for a differential interconnect) that limits the achievable data rate. In order to have a data rate of 3 Gb/s, we make use of a low-ohmic R_L and pulse-width (PW) equalization [2]. Second, the neighboring interconnect creates severe crosstalk. Especially for frequencies above 1 GHz, the transfer functions H_A and H_V are almost equal. Therefore, in order to achieve the data rate of 3 Gb/s, it is necessary to mitigate the crosstalk.

B. Twist Analysis

The neighbor-to-neighbor crosstalk in the bus is reduced by using differential interconnects with twists. Fig. 3 shows how the twists are organized (interconnects in metal 5 and part of the twists in metal 4). Every differential interconnect has only one or two twists (alternately). The positions of the twists are at x_1*l_T, x_2*l_T and x_3*l_T, with l_T the total length of the interconnect.

1) Transfer Functions

The optimal positions of the twists are found, when the crosstalk is minimized. In order to find these optimal positions, we calculate the transfer functions H_A, H_{VDM} for differential mode crosstalk (crosstalk from differential aggressor is measured differentially at victim output) and H_{VCM} for common mode crosstalk (crosstalk from differential aggressor is measured common mode at victim output) as a function of the twist positions.

We will use an even and odd mode analysis. In even mode $V_{S2} = V_{S1}$ and in odd mode $V_{S2} = -V_{S1}$. First, we define four transfer functions (see Fig. 3):
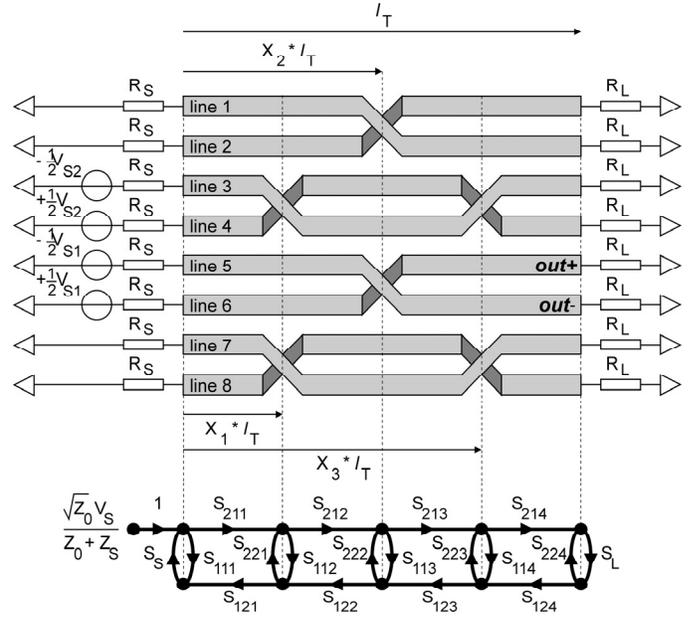

Figure 3: General model for twisted interconnects.

$$H_{even+} = \frac{out_+}{V_{S1}}\bigg|_{V_{S2}=V_{S1}}$$

$$H_{even-} = \frac{out_-}{V_{S1}}\bigg|_{V_{S2}=V_{S1}}$$

$$H_{odd+} = \frac{out_+}{V_{S1}}\bigg|_{V_{S2}=-V_{S1}}$$

$$H_{odd-} = \frac{out_-}{V_{S1}}\bigg|_{V_{S2}=-V_{S1}}$$

(1)

In the next section, we will show how these transfer functions can be calculated. With these transfer functions, we define:

$$H_{A+} = \frac{out_+}{V_{S1}}\bigg|_{V_{S2}=0} = \frac{1}{2}(H_{even+} + H_{odd+})$$

$$H_{A-} = \frac{out_-}{V_{S1}}\bigg|_{V_{S2}=0} = \frac{1}{2}(H_{even-} + H_{odd-})$$

$$H_{V+} = \frac{out_+}{V_{S2}}\bigg|_{V_{S1}=0} = \frac{1}{2}(H_{even+} - H_{odd+})$$

$$H_{V-} = \frac{out_-}{V_{S2}}\bigg|_{V_{S1}=0} = \frac{1}{2}(H_{even-} - H_{odd-})$$

(2)

Finally, we define H_A, H_{VDM} and H_{VCM}:

$$H_A = \left.\frac{out_+ - out_-}{V_{S1}}\right|_{V_{S2}=0} = H_{A+} - H_{A-}$$

$$H_{VDM} = \left.\frac{out_+ - out_-}{V_{S2}}\right|_{V_{S1}=0} = H_{V+} - H_{V-} \qquad (3)$$

$$H_{VCM} = \left.\frac{1}{2}\frac{out_+ + out_-}{V_{S2}}\right|_{V_{S1}=0} = \frac{1}{2}(H_{V+} + H_{V-})$$

2) Even and Odd Mode Analysis

In this section we show how we can calculate H_{even+}, H_{even-}, H_{odd+} and H_{odd-} with the help of s-parameters. The characteristic impedance and propagation constant of a distributed RC-line are [6]:

$$Z_C = \sqrt{\frac{R'}{j\omega(2C_G' + MC_M')}} \text{ and}$$

$$\gamma = \sqrt{j\omega R'(2C_G' + MC_M')} . \qquad (4)$$

R', C_G' and C_M' are defined in section 2.1. M is a Miller multiplication factor and depends on the signal that is on the neighboring interconnects. Because the twists divide the interconnect into four sections (see Fig. 3) M can have a different value for every section k.

For example, if we look at line 6 in even mode, we see that for all sections the capacitance to line 5 is seen double (the signal on line 5 has opposite sign). Therefore, the minimal value of M is 2. For the first section the capacitance to line 7 and for the second section the capacitance to line 8 are seen once (no signal on these lines). So, in sections 1 and 2 M = 3. For the third section, the capacitance to line 3 is seen double (the signal on line 3 has opposite sign), thus M = 4. Finally, for the fourth section, the capacitance to line 4 is not seen (the signal on line 4 has equal sign). Therefore, M = 2.

All values of M for the lines 5 and 6 (both in even and odd mode) are shown in Table I. Also, the length of every section is given.

TABLE I
VALUES FOR M AND l_k FOR EVERY SECTION K

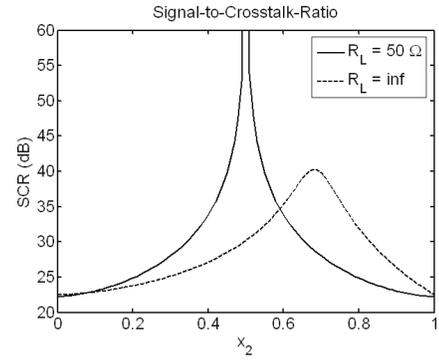| k	M				l_k
	line 5		line 6		
	even	odd	even	odd	
1	4	2	3	3	$x_1 * l_T$
2	2	4	3	3	$(x_2 - x_1) * l_T$
3	3	3	4	2	$(x_3 - x_2) * l_T$
4	3	3	2	4	$(1 - x_3) * l_T$

Fig. 4. Calculated DM SCR as a function of x_2 and R_L ($x_1 = 0$, $x_3 = 1$, $l_T = 10$ mm and $R_S = 50$ Ω).

With these values for M and l_k, the s-parameters [6] of every section k are (see bottom of Fig. 3):

$$S_{ijk} = \frac{1}{2Z_0 Z_{Ck}\cosh(\gamma_k l_k) + (Z_0^2 + Z_{Ck}^2)\sinh(\gamma_k l_k)} \times$$
$$\begin{bmatrix} (Z_{Ck}^2 - Z_0^2)\sinh(\gamma_k l_k) & 2Z_0 Z_{Ck} \\ 2Z_0 Z_{Ck} & (Z_{Ck}^2 - Z_0^2)\sinh(\gamma_k l_k) \end{bmatrix} \qquad (5)$$

Z_0 is a reference impedance and can be chosen freely. The source and load impedance are reflected in S_S and S_L:

$$S_S = \frac{Z_S - Z_0}{Z_S + Z_0}, \ S_L = \frac{Z_L - Z_0}{Z_L + Z_0} . \qquad (6)$$

Note that in the model with s-parameters $V_S = -\frac{1}{2}V_{S1}$ for line 5 and $V_S = +\frac{1}{2}V_{S1}$ for line 6.

Now, with the help of Mason's Rule [6], the transfer functions H_{even+}, H_{even-}, H_{odd+} and H_{odd-} can be found and thus H_A, H_{VDM} and H_{VCM} can be calculated. As the formulas are very complex, they are not shown here.

C. Signal-to-Crosstalk-Ratio

With the help of these transfer functions, the optimal positions for x_1, x_2 and x_3 can be found. We define the signal-to-crosstalk-ratio (SCR) as follows:

$$SCR = \frac{signal \ power}{crosstalk \ power} = \frac{\int_0^\infty X(f)|H_A(f)|^2 df}{\int_0^\infty X(f)|H_V(f)|^2 df} \qquad (7)$$

where X(f) is the power spectral density of the input signal and H_V can be either H_{VDM} or H_{VCM} giving DM SCR or CM SCR.

Fig. 4 shows the DM SCR as a function of x_2. In this case, $x_1 = 0$, $x_3 = 1$, $l_T = 10$ mm and $R_S = 50$ Ω. The SCR is highest if x_2 is 0.5 and $R_L = R_S$. However, if R_L is larger then R_S, the optimum value for x_2 is shifted towards 0.7 and the peak value
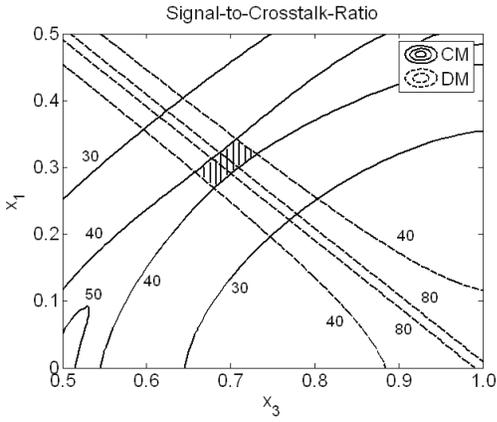
Fig. 5. Calculated contour plot of SCR as a function of x_1 and x_3 ($x_2 = 0.5$, $l_T = 10$ mm and $R_S = R_L = 50$ Ω).
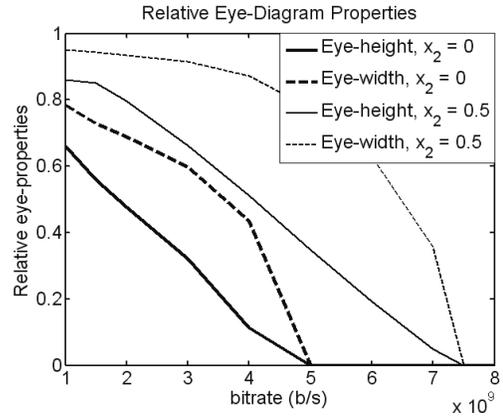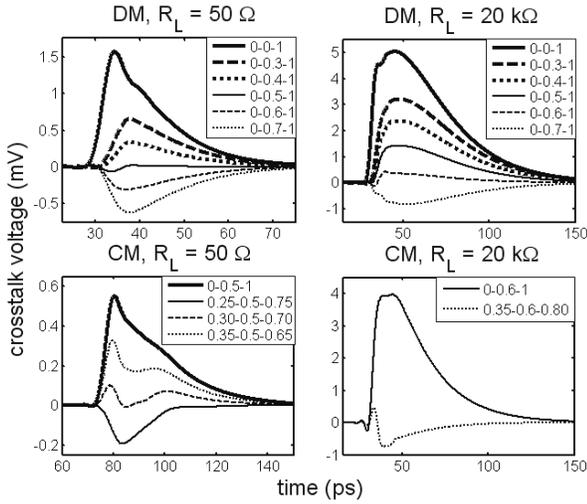

Fig. 6. 3D EM-field simulation step responses for different positions of the twist (x_1-x_2-x_3) and for two different load resistances. Both differential mode (DM) and common-mode (CM) step responses are shown. The length of the interconnects $l_T = 1$ mm.

Fig. 7. Eye-diagram properties with ($x_2 = 0.5$) and without ($x_2 = 0$) twist.

Fig. 8. Relative eye height as a function of x_2 and R_L.

of the SCR decreases. Note that the optimal case, one twist at $x_2 = 0.5$ and choosing $R_L = R_S$, nicely coincides with the fact that for highest bandwidth, both R_S and R_L should be chosen low-ohmic [2].

DM crosstalk can be cancelled with the twist at x_2, but there will still be CM crosstalk. This can be removed by the twists at x_1 and x_3. Fig. 5 shows the SCR for both DM crosstalk and for CM crosstalk as a function of x_1 and x_3 ($x_2 = 0.5$ and $R_L = R_S$). The figure shows that the DM crosstalk is canceled if $x_3 = 1 - x_1$. On this line, the CM crosstalk is minimal at $x_1 \approx 0.3$ and $x_3 \approx 0.7$.

So, the optimal twist positions are at $x_1 = 0.3$, $x_2 = 0.5$, $x_3 = 0.7$ and $R_L = R_S$.

D. 3D EM-field simulations

In order to check the optimal positions, two differential interconnects have been drawn in a 3D EM-Field simulator. The length l_T is only 1 mm to limit the simulation time. Note that for $l_T = 1$ mm, the crosstalk voltage is much lower than
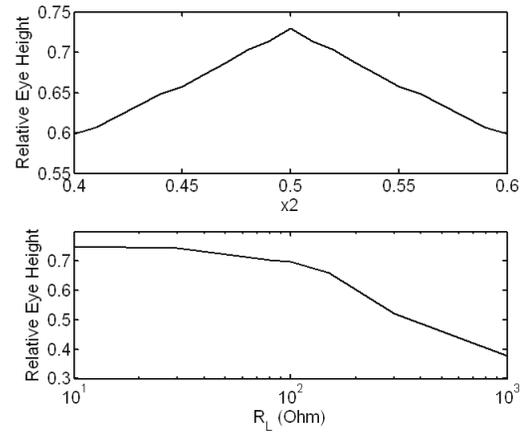
for $l_T = 10$ mm.

One of the differential interconnects has one twist and the other has two twists. Fig. 6 shows the simulated crosstalk voltage (step response) for different positions of the twists ($R_S = 50$ Ω). For DM crosstalk, the optimal position of the twist (x_2) is at 0.5 for an R_L of 50 Ω and between 0.6 and 0.7 for an R_L of 20 kΩ. This coincides with the theory, as the model of the previous section predicts 0.5 and 0.64 respectively.

For CM crosstalk, the optimal positions of the twists (x_1 and x_3) are at 0.3 and 0.7 for an R_L of 50 Ω and at 0.35 and 0.8 for an R_L of 20 kΩ. Again, this coincides with the theory that predicts $x_1 = 0.27$ and $x_3 = 0.73$ for an R_L of 50 Ω and $x_1 = 0.37$ and $x_3 = 0.82$ for an R_L of 20 kΩ.

E. Eyeproperties

By using a method similar to the method described in [7], it is possible to extract eye-diagram properties of the interconnect structure in Fig. 3 at the differential output out+ − out-. It is possible to find the eye-height (relative to the maximum received value) and the eye-width (relative to one symbol period) for different data rates. For a 10 mm long differential interconnect with $R_S = 65$ Ω, $R_L = 150$ Ω, $x_1 = 0$, $x_3 = 1$ and using PW equalization, Fig. 7 shows the relative eye-width and the relative eye-height as a function of data
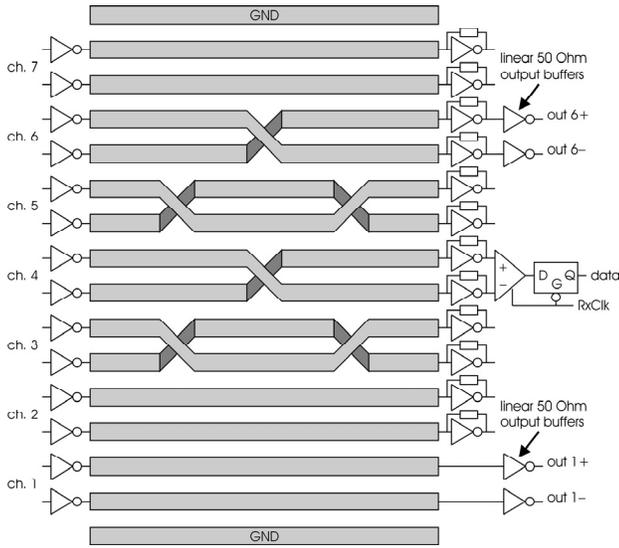
256

Fig. 9. Bus configuration of test chip.

Fig. 10. Measured transfer functions on output of channel 6.

Fig. 11. Measured transfer function on output of channel 1.

rate. Two cases are shown: $x_2 = 0$ and $x_2 = 0.5$. The figure shows clearly that without twisting, the crosstalk limits the data rate. If we look at 50% eye-height, a 2 times higher data rate is possible by using the twist at $x_2 = 0.5$.

In Fig. 8, the relative eye height is plotted against x_2 (upper) and R_L (lower). The data rate is 3 Gb/s. The figure shows that quite some tolerance in the position of the twist and the value of the load resistance is allowed, without reducing the eye height too much.

III.   MEASUREMENTS

On a test chip [2], a bus of seven 10 mm long differential interconnects is measured. The seven channels (see Fig. 9) are driven by inverters with an R_S of 65 Ω. The R_L of about 150 Ω is made with inverters with a feedback resistor. So both R_S and R_L are low-ohmic.

The low-ohmic termination in combination with pulse-width equalization is used to achieve a data rate of 3 Gb/s. This data rate is measured on channel 4, as described in [2]. In this paper, we show the results of measurements on channels 1 and 6. These measurements show the effectiveness of the twists.

Fig. 10 shows the measured transfer function from ch. 6 and the crosstalk transfer functions from ch. 5 and 7 to ch. 6. As expected, the crosstalk from ch. 5 is less than the crosstalk from ch. 7 (double twist in ch. 5 at $x_1 = 0.3$ and $x_3 = 0.7$ reduces CM crosstalk, see top Fig. 10) and both the crosstalk from ch. 5 and ch. 7 is reduced for the differential output (single twist in ch. 6 at $x_2 = 0.5$ reduces DM crosstalk, see bottom Fig. 10).

The transfer functions of Fig. 11 have a smaller bandwidth due to the high-ohmic termination of ch. 1. There is more crosstalk from ch. 2 on out1+ then on out1−, because out1− has no signal carrying neighbor. The bottom graph shows that
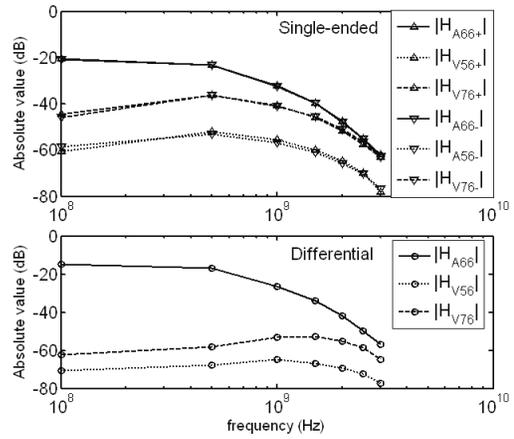
the crosstalk is not reduced for the differential output (no twist in ch. 1).

In Fig. 12 the measured single ended (SE) output and the differential (DIFF) output of ch. 6 are plotted in eye-diagrams for a data rate of 2.5 Gb/s. For reliable communication, the eye should be open. The eye-diagram for the SE output is almost closed (crosstalk from ch. 7). Looking at the DIFF output, the influence of the twist is seen. The eye is almost completely open.

IV.   CONCLUSIONS

By using pulse-width equalization and low-ohmic termination, we achieve a data rate of 3 Gb/s over 10 mm long differential interconnects with a bandwidth of only 82 MHz [2]. However, because of the small spacing, long interconnects and high data rate, the crosstalk is considerable. Therefore, in order to achieve 3 Gb/s the crosstalk has to be mitigated also. The twists that we use for this are analyzed in this paper. Our analysis shows that the optimal positions of the twists depend on the termination of the interconnect. Differential mode crosstalk can be canceled with only one
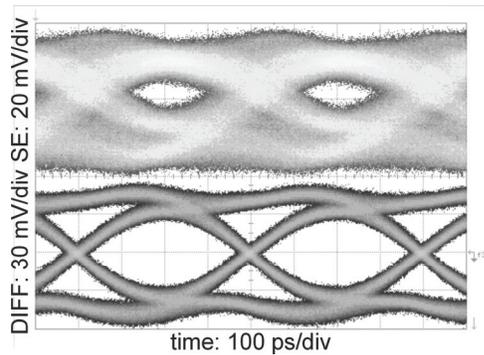
Fig. 12. Single-ended (SE) and differential (DIFF) eye-diagram measurements.

twist at 50% by choosing equal load and source resistances.

Two twists in the neighboring interconnects at 30% and 70% reduce common mode crosstalk.

An analysis with eye-diagram properties shows that a two times higher data rate is possible due to the twisting, while also measurements show the effectiveness of the twists.

REFERENCES:

[1] R. Ho, K.W. Mai, and M.A. Horowitz, "The future of wires," *Proc. IEEE*, pp. 490-504, April 2001.

[2] D. Schinkel, E. Mensink, E. Klumperink, E. van Tuijl, and B. Nauta, "A 3Gb/s/ch transceiver for RC-limited on-chip interconnects," *ISSCC Dig. Tech. Papers,* pp. 386-387, Feb. 2005.

[3] M. Aoki et. al., "A 60-ns 16-Mbit CMOS DRAM with a Transposed Data-Line Structure," *IEEE J. Solid-State Circuits,* vol. 23, no. 5, pp. 1113-1119, Oct. 1988.

[4] R. Ho, K. Mai, M. Horowitz, "Efficient On-Chip Global Interconnects," *IEEE Symposium on VLSI Circuits*, June 2003.

[5] E. Mensink, D. Schinkel, E. Klumperink, E. van Tuijl, and B. Nauta, "Optimally-Placed Twists in Global On-Chip Differential Interconnects," *Proc. 31th Eur. Solid-State Circ. Conf (ESSCIRC)*, pp. 475-478, Sept. 2005.

[6] P.A. Rizzi, Microwave Engineering: Passive Circuits, pp. 168-176, 541-548, Prentice-Hall, 1988.

[7] P. Hanumolu et. al., "Analysis of PLL Clock Jitter in High-Speed Serial Links," *IEEE Trans. On Circuits and Systems II*, vol. 50, no. 11, pp. 879-886, Nov. 2003.