

A Wide Bandwidth Fractional-N Synthesizer for LTE with Phase Noise Cancellation Using a Hybrid- $\Delta\Sigma$ -DAC and Charge Re-timing

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Abstract—This paper presents a 1MHz bandwidth, $\Delta\Sigma$ fractional-N PLL as the frequency synthesizer for LTE. A noise cancellation path composed of a novel hybrid $\Delta\Sigma$ DAC with 9 output bits is incorporated into the PLL in order to cancel the out-of-band phase noise caused by the quantization error. Further, a re-timing circuit is proposed to reduce the nonlinearity in the Charge Pump and provide pulse shaping signals to decrease the charge mismatch. Therefore, a wide loop bandwidth can be obtained while keeping reasonable performance of out-of-band phase noise. The proposed synthesizer is simulated in 90nm CMOS process, consuming 21mA from a 1 V supply.

I. INTRODUCTION

In wireless applications, $\Delta\Sigma$ fractional-N PLLs are preferred as frequency synthesizer due to their wide bandwidth (BW) and fine frequency resolution. Unlike integer-N PLLs, which need a low reference frequency to guarantee fine frequency resolution, in principle, the reference frequency (f_{REF}) of fractional-N PLL can be chosen to any high value with the advantage of non-integer division numbers. Hence, the corresponding loop bandwidth can be increased until it reaches the limitation for system stability ($BW < f_{REF}/10$). However, the main drawback for wide bandwidth fractional-N PLLs is the quantization noise from the $\Delta\Sigma$ modulator. It is well known that the quantization noise will be fed into the PLL and finally converted to phase noise [1]. To alleviate the impact of quantization noise on the PLL output spectrum, the loop bandwidth has to be narrow enough to ensure that the instantaneous error charge at the CP output can be greatly suppressed before it disturbs the VCO. A small loop bandwidth, however, will slow the PLL response down. Incorporating a noise cancellation path in a $\Delta\Sigma$ fractional-N PLL can break up this trade-off between the noise and speed [2]. As shown in Fig.1, the quantization error $e_q[n]$ caused by the $\Delta\Sigma$ modulator is mixed with the frequency control word K and converted to an error charge $Q_n[n]$ which will contribute to the phase noise. On the other hand, $e_q[n]$ is extracted by subtracting the output of $\Delta\Sigma$ modulator from its input and then convert it to a charge $Q_{DAC}[n]$ through the noise cancellation path composed of a Digital-to-Analog Converter (DAC). If the

D/A conversions in the signal path and the cancellation path are equal, the error $e_q[n]$ can be fully cancelled, leaving a clean control voltage $V_{ctrl}(t)$ for the VCO. Consequently, the loop bandwidth will only be limited by the condition of system stability. However, due to temporary charge mismatch and the additional noise generated by the nonlinearity in each block [2], a portion of the error charge $Q_r[n]$ will be deposited to the loop filter and hence reduce the performance of this noise cancellation technique. To alleviate these nonlinear effects, we propose a high resolution DAC and a novel re-timing circuit in order to minimize the residual error charge $Q_r[n]$.

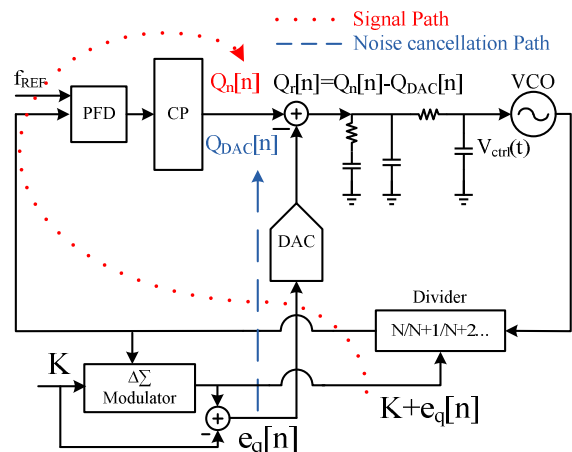


Fig.1 $\Delta\Sigma$ -fractional-N PLL using noise cancellation path.

II. LOOP ARCHITECTURE

Compared to a classical $\Delta\Sigma$ fractional-N PLL the architecture shown in Fig.2 is proposed to meet the LTE's system requirements. First of all, the combination of the VCO and divide-by-two/three circuits are used to guarantee that the output range can cover the desired frequency bands (700 ~ 2600 MHz) on one hand, and avoid the VCO pulling effect on the other hand. Secondly, the adoption of a second order $\Delta\Sigma$ modulator with 18 bits DC input M can ensure that the PLL

output has the required minimum channel spacing. Furthermore, the utilization of a re-timing circuit and synchronous divider can both alleviate the nonlinear effect in the PFD/CP and decrease the charge mismatch between the signal and noise cancellation paths. Finally, a novel hybrid $\Delta\Sigma$ DAC is developed to increase the output resolution and decrease the system complexity and area cost simultaneously.

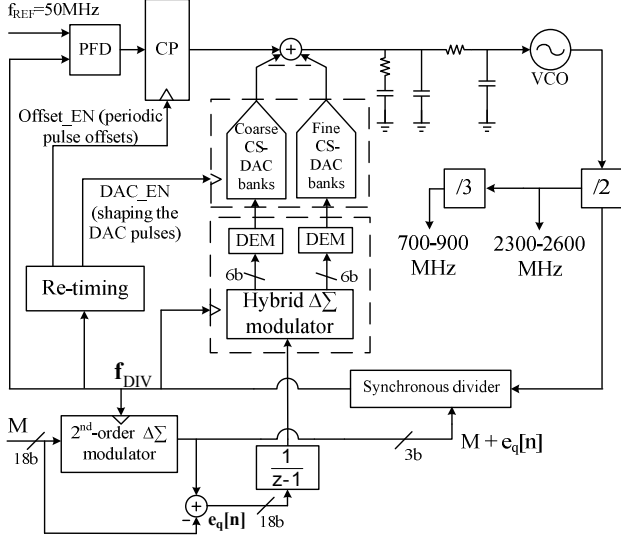


Fig.2 Proposed wide BW fractional-N frequency synthesizer utilizing hybrid $\Delta\Sigma$ DAC for noise cancellation.

III. CIRCUIT DETAILS

A. $\Delta\Sigma$ DAC

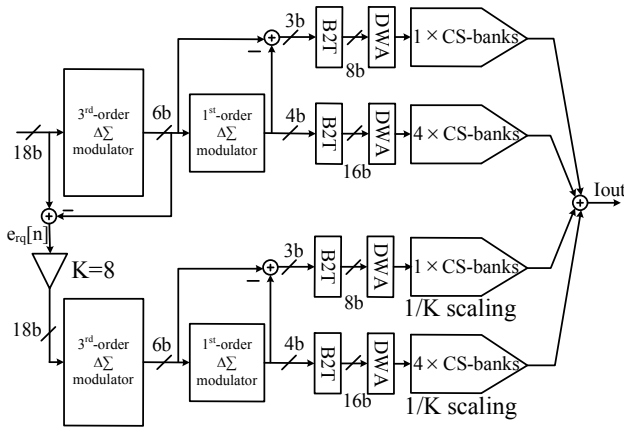


Fig.3 proposed hybrid $\Delta\Sigma$ DAC with 9 equivalent output bits.

In order to avoid the additional noise of the $\Delta\Sigma$ DAC to deteriorate the out-of-band phase noise of the PLL, a high resolution DAC with more than 8 bits resolution is required [2]. The segmented DAC [3] is a candidate for this work. However, complicated Dynamics Elements Matching (DEM) algorithms and Current-Steering (CS) banks are needed for higher resolutions. Another good choice for achieving high resolution is the cascaded DAC [4]. Since more digital blocks and smaller sized analog components are required for higher output resolution, the complexity and area cost can be greatly reduced. However, due to the fact that the analog mismatch between the CS banks will become worse when the scaling

ratio is increased in each stage, the scaling ratio and number of stages should be carefully concerned.

In our work, the "hybrid" (combination of segmented and cascaded architectures) $\Delta\Sigma$ DAC shown in Fig.3 is proposed. A segmented modulator is adopted in each of the cascaded stage in order to increase the output resolution. Since only two cascaded stages are needed to obtain more than 8 output bits, the analog mismatch between CS banks can be alleviated, compared with the typical cascaded DAC architecture which requires larger scaling ratio to reach the same resolution. Its output signal represented in Z domain is given by:

$$Y_{Total}(z) = STF_1(z)X(z) + \frac{1}{K}NTF_2(z)E_{rq}^2(z) \quad (1)$$

where $X(z)$ represents the input signal, $STF_1(z)$ is the signal transfer function of the first stage. $NTF_2(z)$ and $E_{rq}^2(z)$ are the noise transfer function and re-quantization noise of the second stage respectively. Hence by setting the scaling ratio K to 8, the equivalent output bits can be up to 9, meeting the requirement of this phase noise cancellation technique [2].

B. Charge Pump

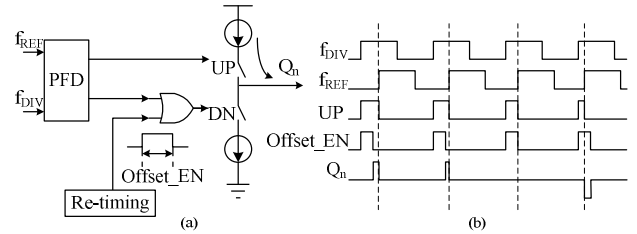


Fig.4 Proposed PFD/CP with timing offset: (a). Schematics; (b). Timing diagram.

Non-linearity in the PFD/CP is one of the troublesome problems in PLL design. Particularly in fractional-N PLLs whose multi-modulus divider dynamically toggles its dividing ratio to achieve the required fractional value, the wide output pattern range of the $\Delta\Sigma$ modulator will result in a noise folding effect when the quantization error $e_q[n]$ comes to the nonlinear PFD/CP. Providing a current offset can have the CP working in a more linear region and hence reduce the noise folding effect [5], [6], as seen in Fig.4. On the other hand, since the output charges of the CP will be reshaped by the timing offset OFFSET_EN and become asynchronous with the DAC output, it will increase the risk of a narrower overlapped region between the output charges of CP and DAC and thus increase temporary charge mismatch. As shown in Fig.2, to avoid the increment of the charge mismatch between the output of CP and DAC, it is necessary that the timing offset and the shaping signal for the proposed CP and DAC are both provided by the re-timing circuit. More details of the re-timing circuit will be illustrated in the next section.

C. Re-timing Circuit and Synchronous Divider

As mentioned above, imperfect charge cancellation will result in voltage ripples on $V_{ctrl}(t)$ which will contribute to the phase noise of the PLL. This is due to the fact that the CP output pulse is Pulse-Width-Modulated (PWM) while the DAC output pulse is Pulse-Amplitude-Modulated (PAM). What's more, most existing works [2],[6] align the rising

edges of DAC pulses with the rising edges of the divider output f_{DIV} , which will probably result in a zero overlapped region between the two pulses, as shown in Fig.5 (a). This means that the VCO will be disturbed significantly before the two pulses can be fully cancelled by each other. When we time the pulses as in Fig.5 (b) and (c), however, the overlap of the pulses will help to cancel the error charge to some extent before it is delivered to the loop filter and hence reduce the voltage ripple on $V_{ctrl}(t)$. Obviously, the case in Fig.5 (c) will result in the smallest voltage ripple and thus is expected to occur in each periodical period. On the other hand, as illustrated before, the timing offset $OFFSET_EN$ will be fed to the CP in order to overcome its nonlinearity. This will increase the occurring probability of the case in Fig.5 (a), introducing higher voltage ripple on $V_{ctrl}(t)$ compared with Fig.5 (b) and (c).

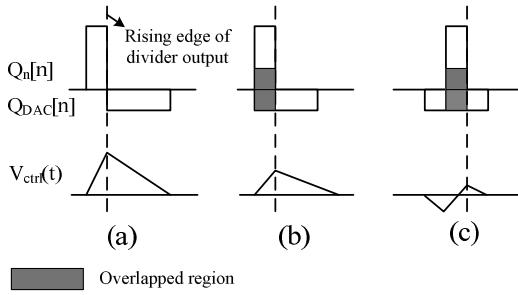


Fig.5 Effect of imperfect charge cancellations on $V_{ctrl}(t)$.

To avoid the case in Fig.5 (a) while reducing the nonlinear effect in CP, the re-timing circuit combined with the synchronous divider is proposed in Fig.6 (a) and the corresponding timing diagram is shown in Fig.6 (b). By introducing the shaping signal DAC_EN which will have the DAC output $Q_{DAC}[n]$ to be aligned with its rising edge, we can guarantee that the CP output $Q_n[n]$ are around the middle area of the $Q_{DAC}[n]$ in most of the periodical periods. The disturbance to the VCO will therefore be greatly reduced compared to Fig.5 (a). Additionally, the delays cell in Fig.6 (a) is composed of a chain of current starved inverters in order to delay the phase of DQ for efficient charge cancellation.

The synchronous divider is composed of a cascaded of five 2/3 cells which have the divide ratio ranging from 32 to 63, covering the desired frequency bands. P0 to P4 are used to switch the divide ratio of each 2/3 cell between 2 and 3 and part of them are provided by the $\Delta\Sigma$ modulator in order to implement the dynamics divide ratio. The DFF flip-flop is adopted in order to align the rising edges of divider input with its output which can help to avoid the phase noise caused by the asynchronous 2/3 cells [5].

IV. SIMULATION RESULTS

Fig.7 depicts the transistor-level simulated results of the phase noise of the VCO. The current consumption is from 1.18 to 1.66mA from a 1V supply. The corresponding Figure-of-Merit (FoM) is from -193 to -189.7dB.

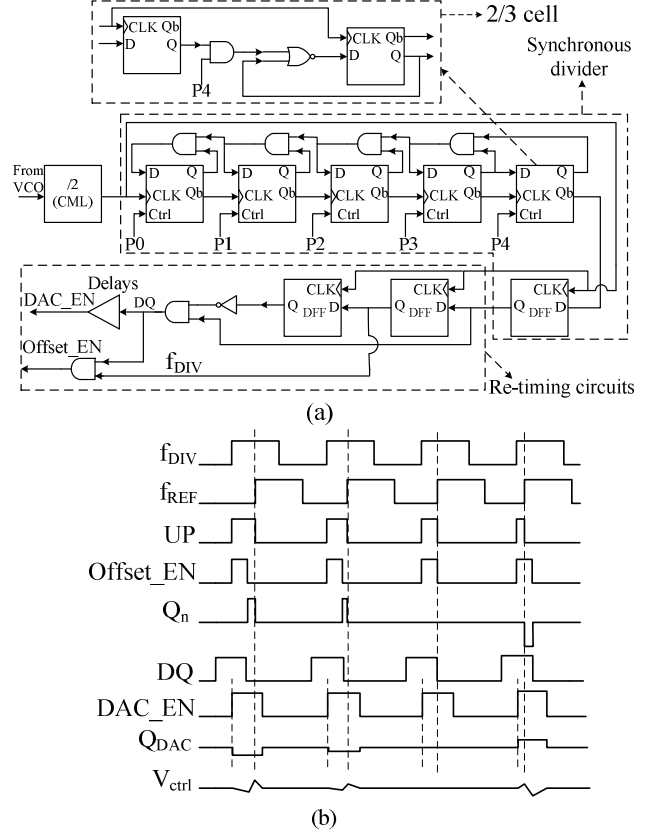


Fig.6 Proposed Re-timing circuit and synchronous divider: (a). Schematics; (b). Timing diagram.

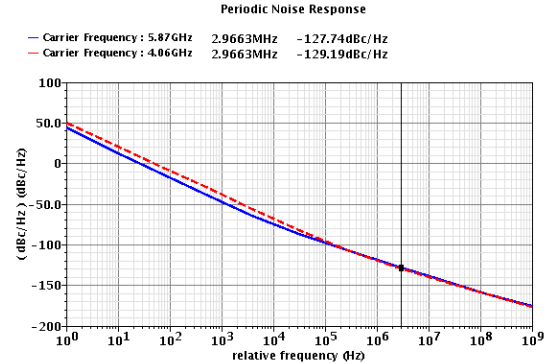


Fig.7 Simulated results of the VCO phase noise at the tuning edges of the output frequency.

As mentioned previously, the charge mismatch and the phase noise from the $\Delta\Sigma$ DAC are the two main reasons for the performance deterioration of this noise cancellation technique. To save simulation time, the charge mismatch and phase noise of the $\Delta\Sigma$ DAC will be examined separately. First of all, the impact of the phase noise contributed by the $\Delta\Sigma$ DAC can be estimated at the transistor-level, when we ignore the phase noise from the PLL's $\Delta\Sigma$ modulator. As shown in Fig.8, when disregarding the phase noise of the $\Delta\Sigma$ modulator for the PLL, the phase noise from the $\Delta\Sigma$ DAC has little impact on the performance of the out-of-band phase noise. Then what's left is to examine the impact of the charge mismatch (which will result in an imperfect cancellation of

the noise of the PLL's $\Delta\Sigma$ modulator) on PLL phase noise when enabling the noise cancellation path. However, the simulation at the transistor-level for estimating the charge mismatch is very time-consuming and impractical and hence not included in this work. Nevertheless, the charge mismatch can be estimated by using a behavioral model in Simulink. As seen in Fig.9 (a), when enabling the noise cancellation path, the PLL transient response becomes more smoother. If we zoom in the diagram, as shown in Fig.9 (b), we find that the effective voltage ripple on the control voltage is greatly suppressed from a magnitude of 100 mV to 5 mV approximately. The charge mismatch is therefore alleviated effectively. The simulated performance of the synthesizer is summarized on Table I.

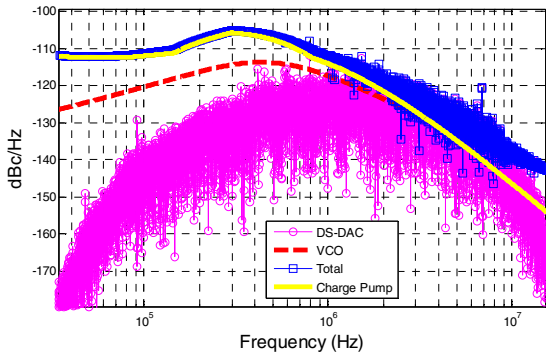


Fig.8 Simulated result of the impact of the noise of the $\Delta\Sigma$ DAC on PLL phase noise when disregarding the phase noise from the PLL's $\Delta\Sigma$ modulator.

V. CONCLUSION.

In this paper, a 1 MHz bandwidth $\Delta\Sigma$ fractional-N PLL utilizing a noise cancellation path is proposed. A hybrid $\Delta\Sigma$ DAC with 9 output bits is designed for the noise cancellation path in order to suppress out-of-band phase noise and keep a reasonable complexity and area. Charge mismatch and nonlinearity in PFD/CP can be alleviated with the assistance of a re-timing circuit. Therefore a wide loop bandwidth can be maintained while keeping reasonable phase noise performance. The synthesizer is simulated in 90nm CMOS process and consumes 21mA from a 1 V supply.

Table I. PERFORMANCE SUMMARY

Architecture	$\Delta\Sigma$ fractional-N PLL	
Process	90-nm CMOS	
Loop Bandwidth	1MHz	
Output Frequency	(3.8 GHz ~ 5.6 GHz)/2 or /6	
FoM of VCO	-193 ~ -189.7 dB	
Power Supply	1V	
Current	Total	21.0mA
	VCO	1.4mA (av.)
	PFD/CP	4.0mA
	$\Delta\Sigma$ Modulator	0.6mA
	$\Delta\Sigma$ DAC	3.6mA
	Buffers + Dividers	4.4mA
	I/Q Generator	7.0mA

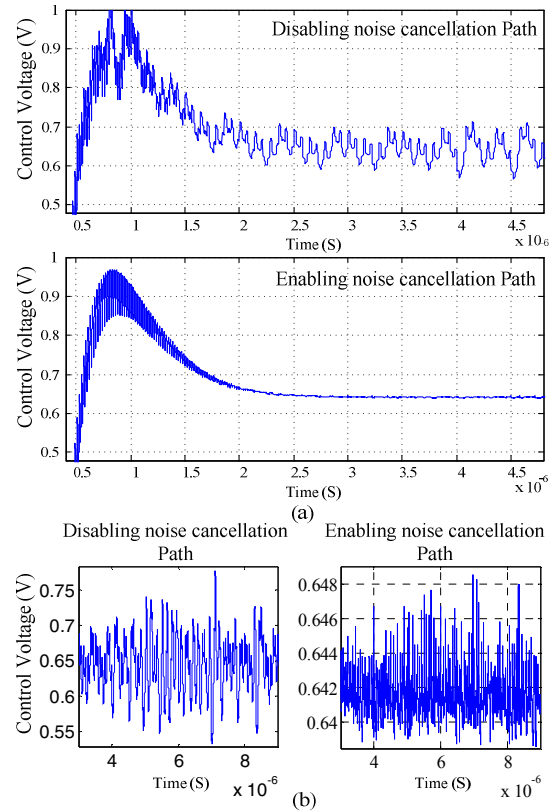


Fig.9 Behavioral simulated results of (a). PLL transient response; (b). Voltage ripples due to the charge mismatch and quantization noise of $\Delta\Sigma$ DAC.

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