A Narrow-to-Wideband Scrambling Technique increasing Software Radio Receiver Linearity

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***Abstract*—Radio receivers and transmitters produce distortion products which are high above the noise floor. These products emanate from a combination of a low-order nonlinearity and the narrowband nature of the signal of interest. In this work, a scrambling system is proposed that can be added to a receiver, reducing these distortion products. Continuous time-domain signal manipulation is used to spread the spectral power of a narrowband signal, before it passes through non-linear receiver circuitry. Digitally the original signal shape is reconstructed. This way, the distortion created by the nonlinearity does not result in dominant tones, improving IP2 and IP3 figures without increasing the intrinsic circuitry linearity, saving power and maintaining flexibility. This topology became possible through using new designs and topologies, which allow signal manipulation using passive components only. Additionally, a new high speed DAC design allows a voltage supply rail to be used as a sub-mV accurate reference. The concept is demonstrated using a software-radio approach, in which the sampling and buffering represents the nonlinear processing. With a 2.2$V_{pp,diff}$ 100 MHz input signal, the measured distortion products are below -74 dBc. At 1.4 GHz input this number is 60.2 dBc. The scrambling hardware uses 54 mW in a 65nm CMOS process.**

I. INTRODUCTION

Radio receivers & transmitters are usually judged by their linearity performance. The reason for this is the nature of the often present relatively narrow-band input signals, whether these are desired signals or unwanted interferers. The non-linear transfer created by high-speed analog circuitry like source-followers, gain-stages, mixers and filters can be described as a polynome:

$$y(t) = \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) + \ldots + \alpha_n x^n(t) \qquad (1)$$

The output y(t) contains the unwanted terms α_2 and α_3, which are responsible for low IP2 & IP3 figures, creating distortion products out of any narrowband input signal. Usually work is done minimizing α_2 and α_3 (making the analog stage more linear) [1]. Rather than doing this however, IP3 can also be improved by ensuring x(t) is not narrowband. If the signal proceeding into the non-linear section is relatively wide-band, distortion from α_2 and α_3, will not manifest as spectrally concentrated tones. This way, without having to maximize the inherent linearity of the circuitry, the power per distortion product can be significantly reduced. Practically this means that a relatively narrowband signal has to be 'scrambled' (temporarily making it much more wide-band) before it passes into the non linear section, after which it is 'recovered' digitally. This approach is only possible if the scrambling stage itself is very linear and has a high-bandwidth. This has been realized using a novel design, which is explained next.

II. SYSTEM TOPOLOGY OVERVIEW

A test chip has been fabricated to proof the concept in a software-radio context. This implies a direct conversion of a large bandwidth without intermediate downconversion or selectivity. Unwanted blockers as well as harmonic multiples of the input frequency (as aliasing folds back any distortion product), can therefore appear in-band. As the incoming signal is digitized, an ADC frontend (including a sampler and a source follower buffer) constitutes the non-linear section. The topology is shown in figure 1.

The narrow-to-wide-band scrambling is done using an ADC, DAC and signal subtractor. This system creates a 2-bit approximation V_{DAC} of the input signal V_{in_A} which is subtracted before it passes through the non-linear section. The non-linear section is a sampler, buffer and the main ADC. Figure 1c shows the signal shape of V_{in_S}, (called the 'residue signal') the signal power of which is spread over a large number of harmonic tones. A second beneficial effect is the factor-of-4 signal swing reduction, reducing the total signal power itself as well.

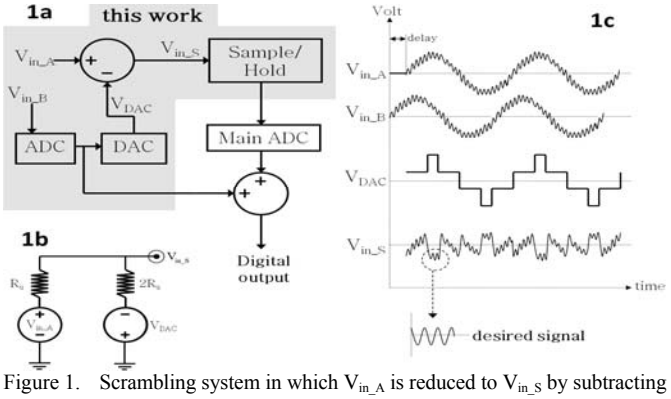

Figure 1. Scrambling system in which V_{in_A} is reduced to V_{in_S} by subtracting a 2-bit coarse DAC signal. 1a) block diagram, 1b) resistive subtractor, 1c) typical signals.

Similar to a 2-step or pipeline ADC, analog signals are subtracted before quantization, however in this topology the subtraction (i.e. the scrambling) occurs before sampling; hence in the time-continuous domain. To enable this topology, 2 crucial problems had to be solved.

Firstly, the scrambling requires an accurate, fast memory-less operating DAC, having very stable output levels. This is needed to accurately reconstruct the original signal shape digitally. A new design is proposed, using the supply voltage as a reference voltage, which shows to have the required properties (further explained in section V).

Secondly, the signal subtraction itself should be very linear. A very high degree of linearity can be obtained if a fully passive solution, based on resistive voltage division, is used. In this case only resistors separate the DAC, sampler circuit and the input signal source, resulting in mutual loading. A subtractor topology has been developed (explained in section V) that completely eliminates such mutual loading while fully maintaining the linearity advantages of passive components.

A third problem is the time needed for the signal manipulations needed to create V_{DAC}, which results in a phase shift between V_{DAC} and V_{in_A} at the subtraction point, where both should be phase-aligned. However, as the incoming signal is relatively narrowband, it is periodical, so signal values at the appropriate phase can be sufficiently accurately estimated from past samples. Various ways of exploiting this, as explained in section IV, enable sufficiently accurate phase-alignment at the subtractor. As assessing the feasibility of the scrambling technique in this proof of concept of scrambling is prioritized, in our test chip such solutions are omitted and 2 input signals are used instead (V_{in_A} and V_{in_B}) which are identical except for a phase shift.

III. Spreading the Spectrum; A Simplified Example

An example, in which harmonic distortion is considered, using a sine shaped input, shows the potential of the scrambling concept. Eq. (1) is simplified to a mildly 3rd order nonlinear voltage transfer:

$$y(t) \approx x(t) + 0.01x^3(t) \tag{2}$$

This nonlinearity has an IP3 figure of 11.55 V; suppose

$$x(t) = 2\sin(2\pi 10^6 t) \tag{3}$$

Now y(t) contains a -40 dBc 3rd harmonic. If, instead, the signal of (3) is first passed through the scrambler system shown in figure 1, then through the non-linear section (2), after which it is reconstructed, the output spectrum looks like shown in figure 2. This simulation shows that the most powerful tone is at -82.4 dBc, which results in an SFDR improvement of 42.4 dB.

2 bits of 'swing reduction' reduces the swing by 75% or 12 dB. Purely lowering the input signal power by 12 dB in an IP3 dominant nonlinear system results in a 24 dB improvement of the 3rd harmonic tone. The linearity improvement from the scrambling is much more substantial. The reason for this is that both swing reduction and spectral spreading decrease the power of unwanted tones, and the digital recovery restores the full signal swing.

Obviously, in many receivers, intermodulation products instead of harmonics pose problems. Applying a narrowband signal instead of the sine (3), these IMD products are equally suppressed using the scrambling technique. This improvement does not depend on the absolute voltage swing levels or frequency of the incoming signal.

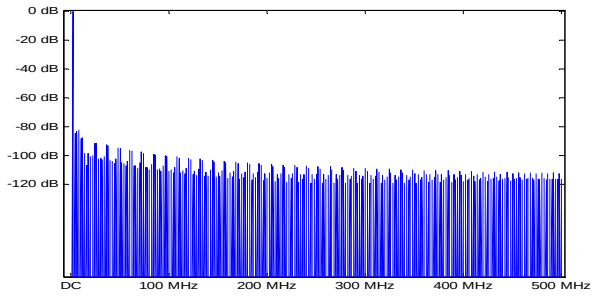

Figure 2. Simulated spectrum of reconstructed original signal, after passing through the scrambler and nonlinearity.

IV. Phase-Alinging the Input and DAC

As the narrow-band input signal is dominant in power, the time-domain input signal shape is periodical and relatively stationary. In the time domain, this means shifts in amplitude or phase are minor between adjacent signal periods, allowing the previous period to serve as a prediction for the next. This property can be used to create proper phase alignment at the subtractor.

If digital delay is 'added' (by simply using flip-flop stages) to the latency caused in the coarse 2-bit path such that the total delay equals a signal period, the phase difference at the subtractor equals 1 period. If adjacent signal periods are sufficiently alike, the residue signal has its intended shape. A certain mismatch is allowed; either if the delay is not exactly 1 period, or if adjacent periods are not exactly alike, the output shape is not ideal (i.e. the swing is slightly larger) but the swing reduction and spectrum spreading properties of the signal scrambling remain, maintaining all linearity advantages. Depending on the statistical signal properties, a delay of several periods rather than 1 can be applied, making the system feasible for higher input frequencies.

As the mismatch would only result in a slight voltage swing increase at the main ADC input, an overrange suffices to enable full reconstruction in the digital domain (analogous to the overrange in the 2nd ADC in a two-step ADC approach).

A different way of creating phase alignment delay is using a digital FIR prediction filter [2], which, using adaptive coefficients, is calibrated using the autocorrelation properties of the input signal.

The abovementioned techniques exploit the fact that the input signal is narrowband hence periodical in nature. Therefore, rather than the narrowband nature of the input signal being a burden through linearity problems (as in traditional radio hardware) in this topology it actually is advantageous.

V. DAC-Subtractor Implementation

The DAC and subtractor are designed to meet all demands mentioned in section II regarding linearity, bandwidth and prevention of mutual loading. In the design, strict control over all currents through all paths, under any scenario is achieved,

as well as prevention of distortion by adding differential currents (such that their sum equals zero) before they enter a non-linear section.

The resistive subtractor (fig. 1b and 3a) uses signal superposition. Since both V_{in_A}, and V_{DAC} are differential, subtraction is simply realized by swapping the 2 terminals of V_{DAC}. A 2-to-1 ratio is used for the R_u resistors, creating a 2-1 weighted voltage division. A larger ratio (e.g. 4-to-1) would reduce the power loss from V_{in_A} to V_{in_S} and increase the power loss from V_{DAC} to V_{in_S}. To minimize the input power loss (because the input power is limited), the V_{DAC} swing should be made as large as possible. Considering the options, a 2-to-1 resistor ratio was decided as a best compromise.

In a normal resistive adder (fig. 3a) the signal sources have to source or sink current from each other, causing mutual loading which creates distortion. To prevent this unwanted influence, a modified bridge-type subtractor (fig. 3b) with 4 current paths is used instead, in which a differential input voltage source is always connected to a DAC voltage source. This way, input signal variations do not cause current flow in the DAC, and no DAC activity is seen at the system input. Therefore the DAC output voltage levels are not modulated by the input signal. Furthermore, this creates the possibility of using a load-sensitive input signal source (in a radio context this could be e.g. a mixing stage) without a buffer, which is normally used to shield sensitive circuitry from intolerable loads, charge dumps or switching noise.

The DAC output code changes only during the hold phase of the sampler circuit, minimizing the capacitive load the DAC sees during the transition, so it is fully settled before the tracking phase of the sampler begins. By resetting the sampler capacitor value before tracking, sampler memory effects are avoided.

As stated before, the DAC output swing should be as large as possible (therefore headroom consuming cascode current output stages are undesired). Furthermore, the DAC's output impedance should be as low as possible. This can be achieved if the DAC is implemented as a combination of CMOS inverters and resistors (fig. 4a) having values $3R_u$ and $6R_u$ to create 2-bit weighting. Such a design has the lowest possible output impedance (only a single deep triode biased MOSFET between the supply and output)

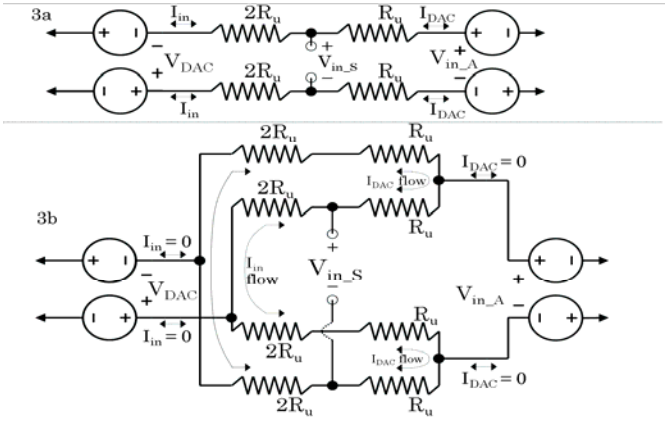

Figure 3. Differential DAC-substractor in which a) signals flow into the voltage sources V_{DAC} and V_{in} and b) a bridge topology where currents flowing between V_{DAC} and V_{in} are prevented

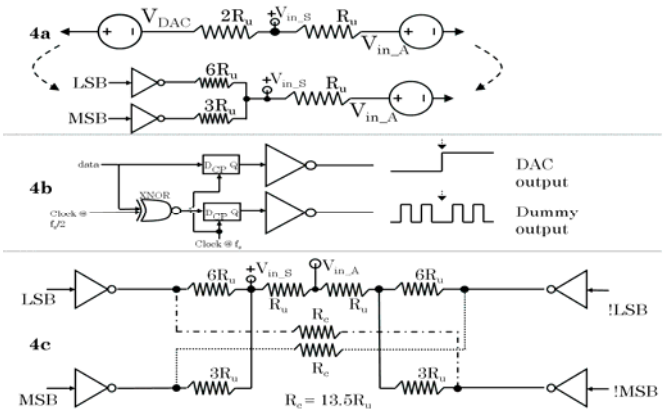

Figure 4. The DAC is implemented with inverters, while b) dummy switching and c) Rc is added for code independent supply current of the DAC.

and the highest possible swing (the triode transistor only consumes several mV of headroom). This however implies the use of a supply voltage as the DAC reference. As 12 bit resolution is desired using a supply of 1.2V, this particular supply rail should be stable within several hundred μV. This requires both on-chip decoupling and a DAC design with accurately draws a constant I_{DD} from this rail regardless of the input code, so that dI/dt bouncing on the reference supply rail is controlled and causes virtually no voltage bouncing. The design as explained below has achieved this goal, allowing for the supply to be used as a voltage reference subsequently allowing the novel DAC design.

VI. Creation of Accurate Supply Voltage Reference

To achieve constant I_{DD}, dummy switches are employed (fig 4b) that switch whenever a DAC output inverter does not switch. The dummy switches are driven by an XNOR gate and the $f_s/2$ clock, and both dummy and data signals are aligned using DFFs. This creates a constant number of CMOS 0→1 and 1→0 transitions per sample. In this way the DAC works perfectly differentially. As no net current from the input passes into the DAC, no input signal scenario can affect I_{DD}.

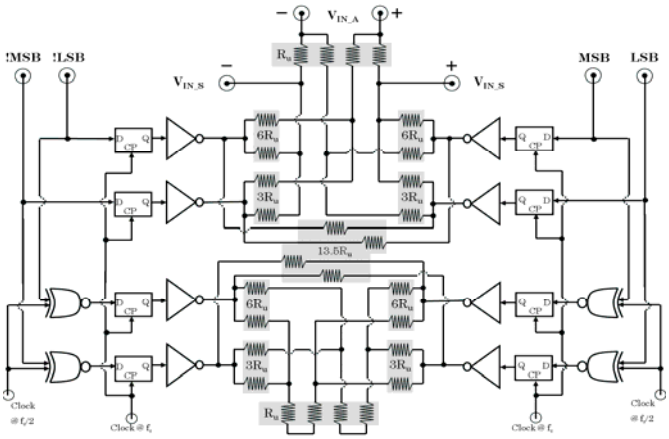

Figure 5. Complete scrambling system, featuring the DAC and subtractor, combining the techniques of figures 3b, 4b and 4c.

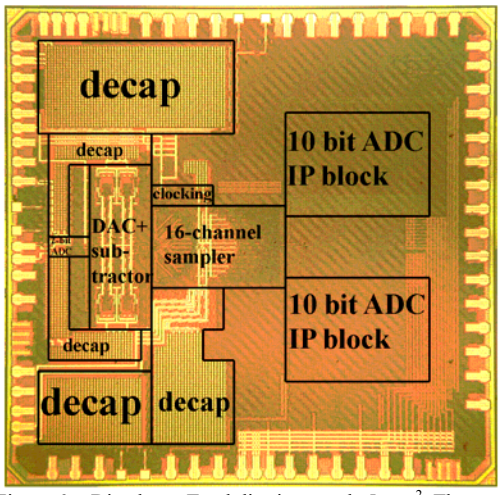

Figure 6. Die photo. Total die size equals 5 mm^2. The scrambling hardware (2-bit DAC, 2-bit ADC, subtractor and clocking) use 0.27 mm^2.

Furthermore, the total DAC current flowing through all resistors is made code-independent by adding a resistor R_c. Fig. 4c depicts the 2 top current paths shown in fig. 3b which are connected to the positive V_{IN_A} terminal, after the substitution shown in fig. 4a. If the DAC code is either 01 or 10, a current flows from MSB to LSB and from !LSB to !MSB, or vice versa. If the DAC code is either 00 or 11, R_c mimics this current. Network analysis for this circuit gives R_c=13.5 R_u.

Finally, this resistor scheme is also applied to the dummy switches. Figure 5 shows the complete DAC-subtractor system, which combines the techniques of figures 3b, 4b and 4c.

For ease of layout, a resistor R_l=6R_u creates the 6R_u, 3R_u and R_u values. This way the resistor widths scale with 1/R, keeping the parasitics proportional to the conductivity and preventing current density differences. This increases accurate resistor scaling and prevents generation of distortion. As R_c=13.5R_u=2.25R_l, R_c was created as 4 parallel + 2 series R_l resistors. This way, the entire structure in figure 4 can be made using only multiples of a single resistor, which improves matching. R_l =180Ω. Analyzing the subtraction node impedance from one of the V_{IN_A} terminals, a completely stationary 50ohm resistive load is present, forming an innocent load to sensitive input circuitry.

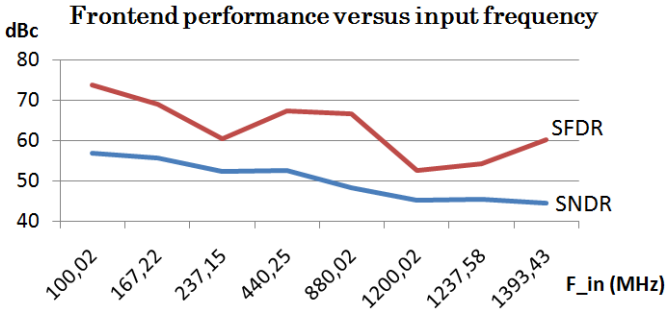

Figure 7. Measured software radio frontend performance, using the scrambling system, versus input frequency. SNDR includes all unwanted terms over a 50 MHz bandwidth. SFDR includes any unwanted tone, including harmonics, intermodulation products or other (spurious) tones.

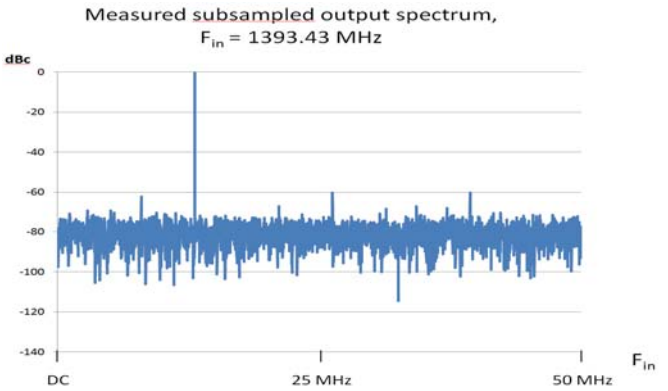

Figure 8. Output spectrum, measured at 100 Ms/s; taken from main ADC data after digital recovery of original signal. No dominant 2nd or 3rd harmonic is present, all unwanted tones are weaker than -60 dBc.

VII. Test Setup Details and Measurement Results

Packaged chips (die photo shown in fig. 6) and an evaluation board were used for testing. Next to the scrambling hardware, the ADC front-end uses a 16-times interleaved sampler, low-jitter clocking and high linearity buffer techniques just as in [3] to allow high-frequency testing and a switching matrix similar to [4], allowing simultaneous subsampled measurement of 2 slices using 2 ADCs. The ADCs are library IP blocks.

Using a sinewave input at F_s = 800 MS/s, DAC supply = 1.2V, and a clocking V_{DD}=1.6V for proper clock timing, both SNDR and SFDR (including harmonics), typically measured among slices and multiple samples, are given in fig. 7. A typical output spectrum is given in fig. 8. At higher frequencies, poor coherence between signal generators deteriorates the performance, but undesired products are always below -52 dBc. The DAC, using the supply as reference, showed memory-less operation at sub-mV accuracy at 800 Ms/s. A 1GS/s ADC [5] having comparable linearity performance consumes 1.2W. The entire scrambling frontend incl. 16 S&H's only needs 0.5W, mostly consumed by clocking and the 16 high linearity buffers in the samplers. The 2-bit ADC and DAC-subtractor forming the bolt-on scrambling system together use 54 mW. The scrambler improves on linearity performance and does not create any mutual loading on either the input signal source or the sampler. This is of high value towards software radio.

VIII. References

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