Metal mask free dry-etching process for integrated optical devices applying highly photostabilized resist

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Photostabilization is a widely used post lithographic resist treatment process, which allows to harden the resist profile in order to maintain critical dimensions and to increase selectivity in subsequent process steps such as reactive ion etching. In this paper we present the optimization of deep UV-curing of 0,3-3.3 μm thick positive resist profiles followed by heat treatment up to 280 ^{0}C. The effectiveness of this resist treatment allows for metal mask free reactive ion etching with selectivity up to 6 for silicon structures, thermal silicon oxide and silicon oxynitride. This procedure is demonstrated by the results obtained in etching of various integrated optical structures.

Introduction

Positive photo resist is not only widely used as a mask for patterning structures in the semiconductor industry but also for manufacturing of a wide range of optical devices. In contrary to electronic devices, where many patterning steps involve small lateral dimensions in combination with a small step height, the main challenge in the patterning of optical devices consists in the high lateral resolution together with mostly a large step height. In our research group a large variety of optical devices based on Si, Si_3N_4, SiO_2 and SiO_xN_y waveguides have been designed, realized and tested.[1,2] For optical waveguide fabrication, the majority of those applications require a steep, vertical step which can be up to several microns high. In order to realize low loss optical waveguides, side walls with low roughness are crucial. When applying reactive ion etching (RIE) on standard processed resist structures, the imposed ion bombardment often causes damage to the resist profile resulting in increased sidewall roughness. In addition, when exceeding the glass transition temperature (Tg) of the resist; re-flown masking material will disturb the maintenance of dimensions.

In order to make the resist structure thermally stable and strong so that it can withstand high temperatures which occur during the RIE and Ion Implantation, several resist treatment methods have been proposed. Deep UV hardening followed by -or in combination with heating[3,4,5], the plasma resist stabilization technique[6], and photoresist polymerization through pulsed photomagnetic curing[7] have been proposed to strengthen the resist profile. In addition, hard baking of the resist structure at high temperature is also necessary to increase the resist selectivity during the RIE.

Of the proposed resist treatment methods, deep UV-curing and thermal heating is a widely used post lithographic process, to harden the resist profile in order to maintain critical dimensions and increase the resist selectivity necessary during the subsequent process steps such as RIE and ion implantation. In the following we apply this method to several integrated optics structures with critical dimensions.

Resist treatment procedure

1- Experiments

The experiments were carried out with various wafers. Blank silicon wafers, thermal and PECVD oxide, thermal nitride and SiON of various thicknesses were used. The resist types used were the positive resist OIR 907/12, diluted resist of 500 nm, OIR 907/17 and OIR 908/35 of Arch Chemicals. After standard cleaning and resist spinning; the wafers were exposed with the Electronic Visions EV620 Mask aligner with 12 mW/mm^2 conventional G-line (436 nm) light source. Different laser written masks were used with amongst others waveguide structures of various dimensions, ranging from 0,9 -4 μm. For the photonic crystals and gratings OIR 907/12 was diluted to obtain a thickness of 300 nm. The resist was single exposed with a period of 500 nm by a Laser Interference Lithography (LIL) system (266 nm) for the gratings and double exposed for the photonic pillars.
In contrast to the standard DUV-curing process, mostly in nitrogen or oxygen atmosphere[8], the wafers were first intensely irradiated in an air filled chamber after which they were baked at temperatures of 180-280 ^{0}C for 1-3 hours.
After DUV-curing and a hardbake step, the structures were etched in Elektrotech Twin System PF 340 Reactive Ion Etching, Plasmatherm 790 parallel plate Reactive Ion Etching or Alcatel Adixen DE Inductive Coupled Plasma machines. The profiles were measured with Dektak 8 of Digital Instrument Veeco Metrology Group and examined with the Scanning Electron Microscope of JEOL, type JSM-5610/5610LV.

2- Results and discussion

In figure 2 the process optimization is presented for resist 907/17, 1.2 μm and diluted resist of 300 and 500 nm. Figure 2 (a) is a picture of the resist profile after development in the OPD4262 positive resist developer. Figure 2 (b) is the optimized result of DUV-curing followed by hardbake at 250 ^{0}C for 2 hours. The integrity of the resist profile is retained quite well, including the line width control and the sidewall angle.
Figure 2 (c) is the result of a hardbake at 280^{0}C for 1 hour. The profile shrinkage is more pronounced in the width as well as in the height compared to figure 2 (b). Thus to maintain the integrity of the resist profile, the hardbake should be applied below 280^{0}C. Figure 2 (d) is 300 nm DUV cured and hardbaked resist at 180^{0}C for 2 hours used for etching of gratings. Figure 2 (e) is 500 nm hardbaked resist at 180^{0}C for 2 hours used for amongst others etching of silicon oxynitride.

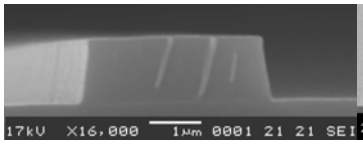

Figure 2(a)

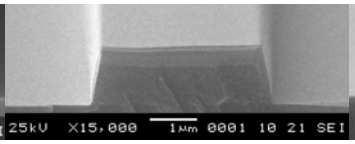

Figure 2(b)

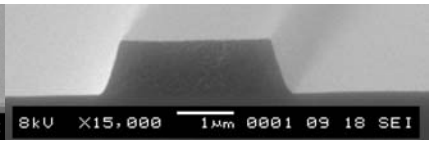

Figure 2(c)

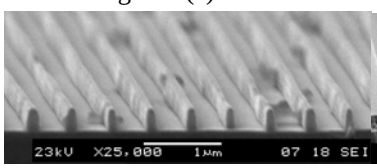

Figure 2(d)

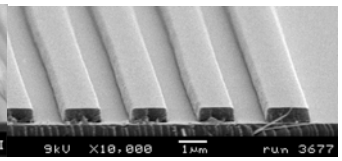

Figure 2(e)

The hardbake should be carried out step by step to the final temperature of 180^{0}C or higher in order to maintain the integrity of the resist profile.
Obviously the thicker the resist, the longer the irradiation and also a proper optimization is required. Characterizing and determining the proper sequence of UV exposure and

thermal rise to a final temperature are paramount to the success of photostabilization[8]. In Figure 3 the process optimization is presented for resist 908/35, 3.3 µm.

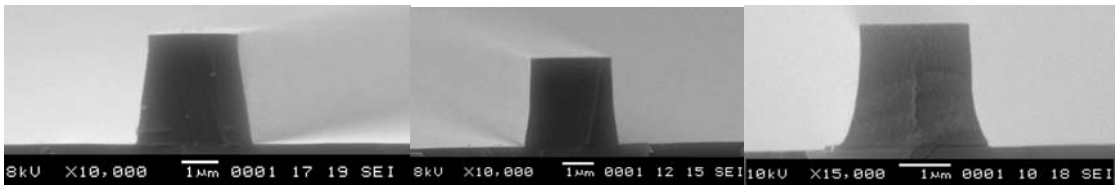

Figure 3(a) Figure 3(b) Figure 3(c)

Experiments have been carried out with resist 908/35 which gives profile heights around 3,3 µm. In figure 3 (a) a SEM picture is presented of resist 908/35 after development. Figure 3 (b) is the result of optimized hardbake at 180^0C for 2 hours after DUV-curing. Figure 3 (c) is a similar resist profile baked at 280^0C for 1 hour. As can be seen, the integrity of the profile is still well maintained, although the forming of the so-called "foot", as observed in figure 2 (c) as well, is clearly present. It appears that the bottom of the profile is slightly broader than the top which is of course partly inherent to the lithographic process, as can be seen in picture 3 (a) whereby the difference between broadness of the top and bottom is around 0.8 µm for this type of resist. The behavior of a so-called "foot" is also clearly observed by I. Pollentier et al.[9]

3-Etch selectivity

Experiments have been carried out with resist baked at 180 and 280^0C to investigate the etch selectivity. There was no noticeable difference measured between resist baked at 180 and 280^0C. Therefore, for the further experiments, the resist profiles were standard hardbaked at 180^0C for 2 hours.

For silicon oxynitride layers of 1.5 -2.5 µm deposited on silicon and etched in the Plasmatherm 790 dry etching machine, a selectivity of 5 was obtained. For layers of 1.5 -2.5 µm SiON deposited on 8 µm thermal oxide a selectivity of 6 was obtained. For silicon a selectivity of 4-5 is obtained for etching controlled structures of 200 - 1000 nm in the PF 340 Reactive Ion Etching twin system. For oxide, a selectivity of 4 was obtained in the Plasmatherm 790 and a selectivity of 6 was obtained in the Alcatel Adixen DE Inductive Coupled Plasma etching machine. In addition, the silicon nitride selectivity never has been a problem; it is quite high.

4-Examples of optical structures in SiON, SiO_2 and Si

Initial experiments have been carried out with silicon oxynitride (SiON) layers ranging from 1.0- 2.5 µm, because from the lithographic point of view, SiON is the most difficult material in achieving high resolution and high etching steps. If the process could be optimized for SiON; other materials like oxide, nitride and silicon would form no problem.

Figure 4 (a) is an arbitrary SiON waveguide of 1.5 µm etched in the Plasmatherm 790 reactive ion etching machine using resist thickness of 1.2 µm. Figure 4 (b) is a microring resonator of SiON with waveguide width of 0.9 µm and the gap between the ring and waveguide of 0.6 µm. Under specific conditions it is possible for conventional contact mask lithography with a source wavelength of 436 nm, to open gaps of 0.6 µm between the waveguide and the resonator with 2.5 µm SiON on 8 µm thermal oxide

using diluted resist of 500 nm. The etch step in figure 4 (b) is 1.7 µm in SiON of 2.5 µm.

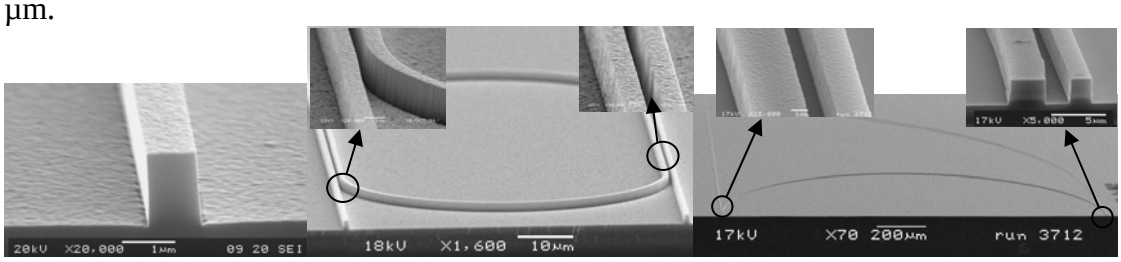

Figure 4(a) Figure 4(b) Figure 4(c)

Figure 4 (c) is a micro ring resonator of 2.5 µm height in SiON etched in the Plasmatherm 790, using resist of 0.9 µm. The gap is around 1.0 µm.

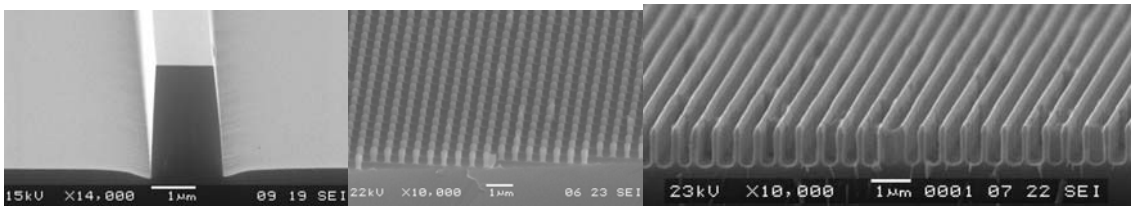

Figure 4(d) Figure 4(e) Figure 4(f)

Figure 4 (d) is a waveguide of 2.3 µm height etched in thermal silicon oxide in Alcatel Adixen DE Inductive Coupled Plasma (ICP) etching machine, using 1.2 µm resist. It would be possible with the same amount of resist to etch around 6 µm thermal oxide.
Figure 5 (e) is an example of photonic pillars of 750 nm etched in silicon and figure 4 (f) is an example of a grating of 750 nm height in silicon with 160 nm resist still on top of the structure.

As demonstrated in the aforementioned examples; optimization of UV radiation and temperature treatment after exposing provide a meaningful tool to produce a broad range of critical optical structures in silicon, thermal silicon oxide, nitride and silicon oxynitride.

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