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The Twente LINX backplane

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Abstract. The design of a control system is not finished with the derivation of the necessary control algorithms. When the controller is implemented in a digital computer the system designer has to schedule all control and calculation tasks within the sampling interval of the system. Higher sampling frequencies often improve the system performance. On the other hand, more sophisticated control algorithms require more computing time thus reducing the obtainable sampling frequencies. Therefore, it is important to minimise the overhead of sampling and communication. This paper describes a transputer–based I/O system fulfilling this requirement and shows how the sampling with this system is done.
Keywords. Link Based Backplane, Transputer Based I/O, Sampling, Parallel processing, Real-time Computer Systems, Control Engineering, Applications of Computers, Robot control, Transputers, Occam.

1. Introduction

At the Control Laboratory of the Electrical Engineering Department of the University of Twente much effort is put in the design of control algorithms for mechatronic systems [1], e.g. robots. Experimental setups at the laboratory include a one-link and two-link flexible robot and a high speed robot with six degrees of freedom. To control these robots advanced control algorithms have to be used. However, these algorithms are computationally intensive. The sampling frequencies for these systems are between 250 Hz and 1000 Hz.

In the past these robot set-ups were built using a PC with I/O boards for the interfacing and transputer cards for calculating the control algorithms [2]. In this setup the PC controls the sampling and transfer of data from and to the transputer. In order to achieve equidistant sampling the timer of the PC has to be used. Due to memory refreshes, harddisk accesses and screen and keyboard services an interrupt latency arises. This latency causes jitter, which can run up to 400 microseconds. This is unacceptable for control algorithms. Furthermore the single CPU on the PC–bus itself is a bottleneck. The maximum number of samples that can be obtained depends on the speed at which the CPU can access the I/O devices and perform the communications to the transputer network. If the number of I/O channels goes up the maximum sampling frequency goes down.

All this has led to the idea that the sampling should be done on the transputer boards, without interference from a central processor. This leads to a setup as shown in Fig. 1. The aim is to loose less than 5% of time to interface overhead at 1KHz, resulting in a required sampling frequency of 20 KHz. Therefore it was decided to design a dedicated transputer I/O system to meet these requirements. This system is based on the LINX backplane, which is a modular

* Detached at the Control Laboratory by Van Rietschoten & Houwens, Rotterdam

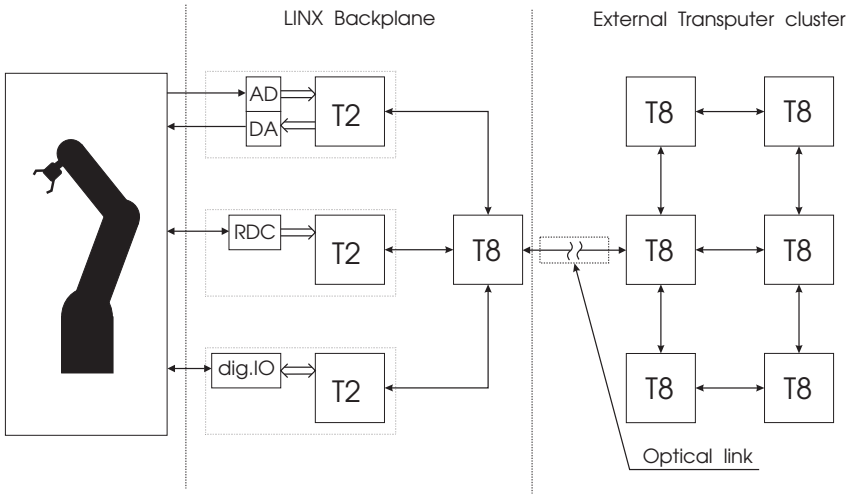


Fig. 1 Robot setup with Linx system and transputer cluster.

backplane for transputer–based I/O systems. In order to ease the design of the I/O cards a standard TRAnsputer Section called TRAS was designed. In order to connect the I/O cards to an external transputer cluster an optical link was designed.

The organisation of this paper is as follows: Section 2 describes the Twente LINX backplane, Section 3 describes the TRAS, Section 4 describes the optical link, Section 5 describes how sampling is done with the Twente LINX backplane and finally some results are given.

2. The Twente LINX backplane

The Twente LINX backplane was designed as a solution for the cabling problem. The mechanical design of the backplane follows the specifications of the VME standard. The LINX backplane is intended for use in an industrial environment. Therefore, special attention was given to the electrical and mechanical robustness of the system, following the VME specifications as close as possible. The design of the backplane was based on the following requirements:

- The backplane is primarily intended for real-time control systems with transputer based I/O.
- The backplane should be both electrically and mechanically reliable.
- The backplane should be reconfigurable under software control.
- A modular design should provide a flexible, inexpensive system.

The decision to design a special purpose backplane was made deliberately. The requirements resulted in the following architecture:

- The backplane provides the user with eight slots for transputer boards and two slots for linkswitch boards.
- Each of the linkswitch boards control 32 links on the backplane and several links from and to the external transputer cluster.

This adds up to a total of 64 links on the backplane, divided into two independent subsystems of 32 links each. From each slot, four links are connected to each subsystem. The switch card slots are placed on the left and the right of the transputer card slots. The layout of the LINX backplane is given in Fig. 2.

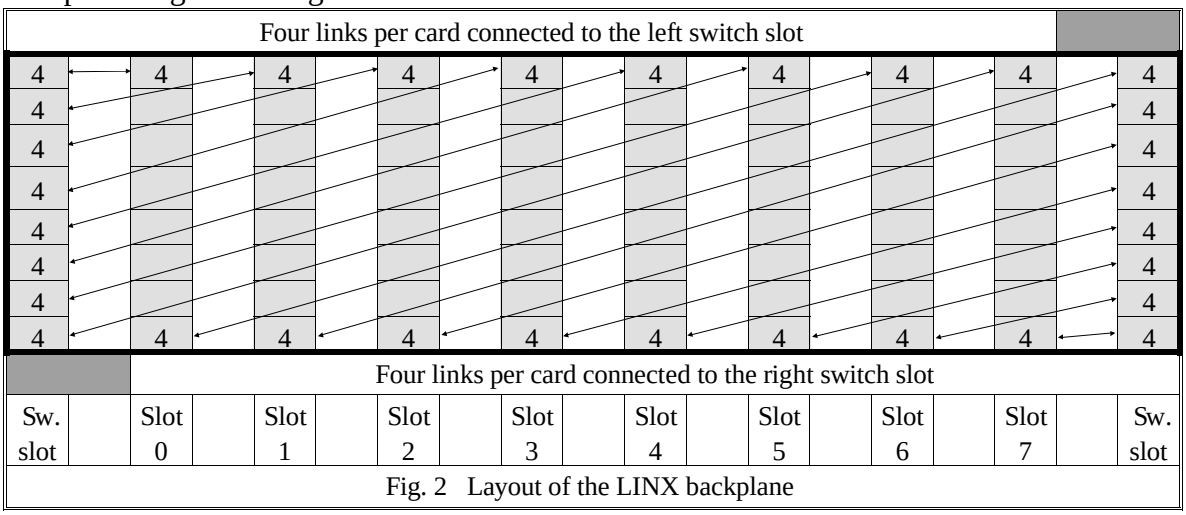


Fig. 2 Layout of the LINX backplane

2.1 System configuration

The system is based on a VME rack size of 3 or 6 HE (3 HE is a single height eurocard, 6 HE is a double height eurocard). A 6HE VME rack has room for two backplanes, one for the top row and one for the bottom row. The Twente LINX backplane definition is flexible by allowing that either the bottom row or the top row or both may contain a LINX backplane. In the first two cases the user can use 64 link interconnections; when two backplanes are used 128 link interconnections are possible. Each backplane contains eight slots for transputer (I/O) cards and two slots for linkswitch cards. The simplest configuration contains one switch card and one transputer card. The system may be expanded by adding more transputer boards. Each transputer slot has connections for eight links.

The configuration of the system depends on the number of transputers per board. When a single transputer per board is used, the system is fully reconfigurable on the link level. When two transputers per board are used, the system is fully reconfigurable on the transputer level.

For I/O subsystems a number of special provisions are made:

- The backplane has separate -15, 0 and +15 Volts analog power lines.
- There is a special sampling clock, called VarClock, that may be used to synchronize the sampling of different A/D, D/A and RDC converters.
- The backplane has separate -12, 0 and +12 Volts power lines for digital I/O logic like RS232 line drivers etc.

2.2 Link signals

Eight links are available at each slot. These links are placed at the top 8 and bottom 8 pins of the connector. The link signals are routed through the inner layers of a multilayer printed circuit board shielded by ground planes, thus avoiding crosstalk between transputer links. The link signals are defined in Table 1.

L0 out, L1 out, L2 out, L3 out. (slot 0...7)	Link inputs of the left switch slot for the output links 0...3 from each transputer card
L0 in, L1 in, L2 in, L3 in. (slot 0...7)	Output links of the left switch slot, connected to the input links 0...3 of each transputer card
L4 out, L5 out, L6 out, L7 out. (slot 0...7)	Link inputs of the right switch slot for the output links 4...7 of each transputer card
L4 in, L5 in, L6 in, L7 in. (slot 0...7)	Link outputs of the right switch slot to the input links 4...7 of each transputer card
LS1 in, LS2 in, LS1 out, LS2 out	Two links as direct interconnection between the left and right switch card

Table 1. Link signals

The impedance of a link on the backplane is between 50 and 60 Ohms. For buffering of the links 74AC244 type buffers is preferred. The links are buffered at both the sending and receiving side. The sending side should be connected through a characteristic impedance as illustrated in Fig. 3.

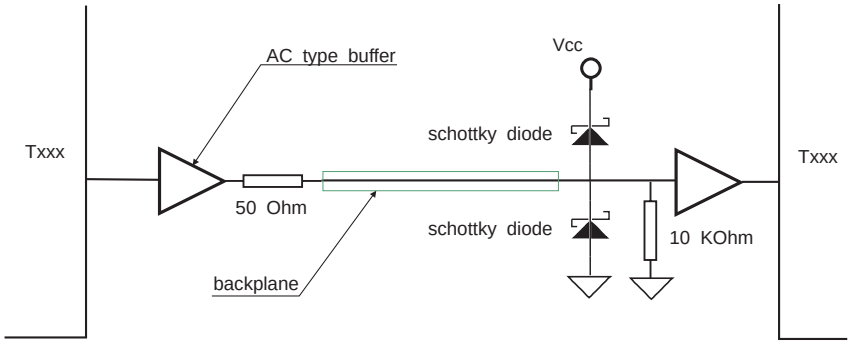


Fig. 3 Buffering of links

2.3 Power lines

Each slot contains five different supply voltages, three for digital circuits and two for analog circuits. The digital power lines are for +5, +12 and -12 Volts. The analog power lines are for +15 and -15 Volts. In order to obtain proper current loading multiple pins carry the same voltage (table 2).

gnd	Digital ground, 23 pins.
+5 Volts	+5 Volts supply, 6 pins.
+12 Volts	+12 Volts supply, 2 pins.
-12 Volts	-12 Volts supply, 1 pin.
agnd	Analog ground, 2 pins.
+15 Volts	+15 Volts supply for analog circuitry, 2 pins
-15 Volts	-15 Volts supply for analog circuitry, 2 pins.

Table 2. Digital and analog power lines

2.4 System services

System services are control signals on the backplane such as the system clock, reset etc. These signals are connected in a bus or in a daisy chain.

Reset	Global reset signal for all boards of a backplane. This signal is active high. The signal is generated by the left link switch card. Output at left switch slot, input on all other cards.
Analyse	Global analyse signal for all boards of a backplane. This signal is active high. The signal is generated by the left link switch card. Output at left switch slot, input on all other cards.
notError	Global error signal, this signal is active low. This signal propagates any error in the system. This is a open collector signal (Wired OR)
LinkSpeed	This signal selects the link speed for the backplane communication. A zero selects 10 Mbit/s, a one 20 Mbits/s. Output at left switch slot input on all other cards.
SysClock	The SysClock is a TTL level clock with a fixed frequency of 5 MHz. This clock is generated at the left link switch card. Output at left switch card, input on all other cards.
VarClock	The VarClock is a TTL level clock with a variable frequency. This clock is generated at the left link switch card. Output at left switch card, input on all other cards. This is a open collector signal.
LA in	Input from the left daisy-chain link.
LA out	Output to the left daisy-chain link.
LB out	Output to the right daisy-chain link.
LB in	Input from the right daisy-chain link.

Table 3. Signals comprising the system services

The system services signals, listed in Table 3, consist of three groups of signals i.e.:

- The *system control signals* consist of the Reset, Analyse, notError and LinkSpeed signals.
- The *system clocks* consist of two clock signals, one SysClock at a fixed 5 MHz frequency, and a VarClock with a variable frequency.
- The '*board control*' signals that make it possible to use cards with an on board link switch. To control this switch an extra link needs to be connected to the card. The method used is identical to the one used in the design of the Inmos TRAM motherboards. The link switches are controlled by an on-board T222. The boards are interconnected in a daisy-chain. In order to operate the daisy-chain, the left and right daisy-chain links of a card without a link switch have to be connected.

2.5 Signal description of the transputer card slots

A transputer card slot of the LINX backplane consists of a single 64/96 way DIN 41612 connector of which only row A and row C are used for the transputer card slots, as indicated in Table 4.

2.6 Description of the link switch slot

The two linkswitch slots on the backplane are identical, except for the Reset, Analyse, Error, Linkspeed and the clock signals, because these signals are generated by the left switch card and received by the right switch card (see Table 5). A switch card may be inserted in either one of these slots. As a minimum a link switch card or a hard wired switch card must be installed in the left slot. The links 0 to 3 of each transputer card slot are connected to the left switch slot. The links 4 to 7 of each transputer card slot are connected to the right switch slot.

Pin	A-row	B-row	C-row
1	L0 out	nc	L0 in
2	L1 out	nc	L1 in
3	L2 out	nc	L2 in
4	L3 out	nc	L3 in
5	gnd	nc	gnd
6	+5	nc	+5
7	LA in	nc	LB out
8	gnd	nc	gnd
9	LA out	nc	LB in
10	gnd	nc	gnd
11	VarClock	nc	gnd
12	SysClock	nc	gnd
13	gnd	nc	gnd
14	Linkspeed	nc	gnd
15	gnd	nc	gnd
16	+5	nc	+5
17	gnd	nc	gnd
18	+15	nc	+15
19	agnd	nc	agnd
20	-15	nc	-15
21	gnd	nc	gnd
22	Reset	nc	gnd
23	Analyse	nc	gnd
24	notError	nc	gnd
25	gnd	nc	-12
26	+12	nc	+12
27	+5	nc	+5
28	gnd	nc	gnd
29	L4 out	nc	L4 in
30	L5 out	nc	L5 in
31	L6 out	nc	L6 in
32	L7 out	nc	L7 in

Table 4. Transputer card slot

Pin	A-row	B-row	C-row
1	L0/L4 out 0	+5	L4 in 0
2	L1/L5 out 0	+5	L5 in 0
3	L2/L6 out 0	gnd	L6 in 0
4	L3/L7 out 0	LS1 out	L7 in 0
5	L0/L4 out 1	LS1 in	L4 in 1
6	L1/L5 out 1	gnd	L5 in 1
7	L2/L6 out 1	L in	L6 in 1
8	L3/L7 out 1	gnd	L7 in 1
9	L0/L4 out 2	L out	L4 in 2
10	L1/L5 out 2	gnd	L5 in 2
11	L2/L6 out 2	VarClock	L6 in 2
12	L3/L7 out 2	SysClock	L7 in 2
13	L0/L4 out 3	gnd	L4 in 3
14	L1/L5 out 3	LinkSpeed	L5 in 3
15	L2/L6 out 3	gnd	L6 in 3
16	L3/L7 out 3	+5	L7 in 3
17	L0/L4 out 4	+5	L4 in 4
18	L1/L5 out 4	gnd	L5 in 4
19	L2/L6 out 4	LS2 out	L6 in 4
20	L3/L7 out 4	LS2 in	L7 in 4
21	L0/L4 out 5	gnd	L4 in 5
22	L1/L5 out 5	Reset	L5 in 5
23	L2/L6 out 5	Analyse	L6 in 5
24	L3/L7 out 5	notError	L7 in 5
25	L0/L4 out 6	-12	L4 in 6
26	L1/L5 out 6	+12	L5 in 6
27	L2/L6 out 6	+5	L6 in 6
28	L3/L7 out 6	gnd	L7 in 6
29	L0/L4 out 7	gnd	L4 in 7
30	L1/L5 out 7	gnd	L5 in 7
31	L2/L6 out 7	+5	L6 in 7
32	L3/L7 out 7	+5	L7 in 7

Table 5. Left/Right linkswitch slots

3. The TRAnsputer Section TRAS

In conjunction with the LINX backplane a standard TRAnsputer Section (TRAS) was designed. Because most I/O applications do not require more than 16 bits the design was made with a T222. The T222 can address 64 Kbyte of memory. The on–chip high speed RAM takes up the lower 4 Kbyte of addressable memory. The other 60 Kbyte can be accessed via the External Memory Interface (EMI). Although the EMI is simple compared to other processors, the high speed of the T222 may cause timing problems if standard RAM or memory–mapped I/O is used. In order to obtain a standard transputer section that may be used on all I/O boards the TRAS (Fig. 4) was designed with a programmable timing interface.

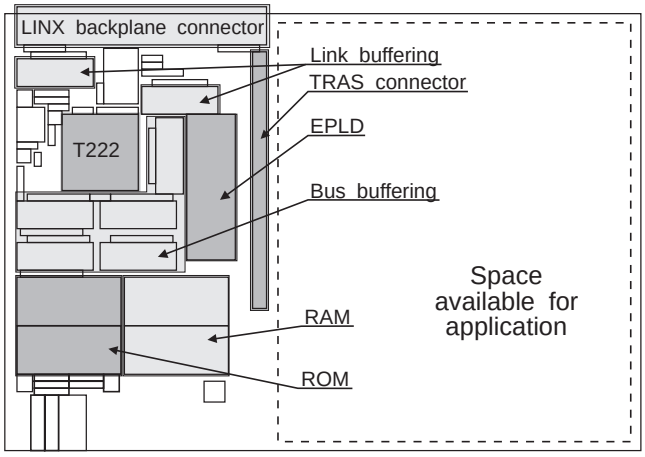


Fig. 4 Standard TRAnsputer Section TRAS

The TRAS consists of static RAM sockets, ROM sockets, buffering of addressbus, databus and control signals and buffering to and from the LINX backplane. The glue logic is contained in one EPLD, which is a programmable logic device. Because of this EPLD the TRAS can be adapted to the I/O application. Also the memory mapping of I/O devices can be changed this way. The only part of the TRAS that user needs to be concerned with is the TRAS connector (see Fig. 4). This connector has all the necessary signals to connect an I/O application to the TRAS. Also some user definable signals from unused pins of the EPLD are available. The signals available on the TRAS connector are listed in Table 6.

A[0..15]	Buffered address lines from the transputer.
D[0..15]	Buffered data lines from the transputer.
VarClock	VarClock from the LINX backplane.
ProcClockOut	Buffered 20 MHz clock of the transputer.
Reset	Board reset signal.
notMemCe	Buffered Mem Chip Enable of the transputer.
notMemWrB0 & 1	Buffered Mem Write signal of the transputer.
MemBAcc	Buffered Byte Access signal of the transputer.
EventReq	Event Request to the transputer.
EventAck	Event acknowledge from the transputer.
MemGranted	Buffered Mem Granted from the transputer.
MemReq	Buffered mem request to the transputer (to claim the bus).
notRead	Buffered read signal made in the EPLD.
notWrite	Buffered write signal made in the EPLD.
notError	Buffered board Error signal.
UserIO[0..11]	User definable pins from the EPLD.
VCC	Digital power supply 5V.
+12V & -12V	Digital power supply.
GND	Digital ground.
+15V & -15V	Analog power supply.
AGND	Analog ground.

Table 6. Signals available on the TRAS connector

3.1 TRAS I/O timing

One of the problems one has to deal with when designing a transputer–based I/O system is the combination of a fast processor and a slow I/O device. In that case the transputer has to be slowed down. This is possible with the MemWait pin of the transputer. However, the T222 will only react on the MemWait during state T2. A wait state generator has to make the MemWait signal high between 25 and 50 nano seconds after the notMemCe goes down. Because a rather slow EPLD was used with a cycle time between 20 and 30 nano seconds the MemWait may arrive too late. On the TRAS this is solved by keeping the MemWait high constantly. If the T222 starts a read or write cycle it will take the notMemCe low. The EPLD will keep MemWait high until a sufficient number of waitstates are inserted, after which the T222 will finish its read or write cycle. The disadvantage of this method is that there is always one wait state. If a slow I/O device is selected by the T222, the EPLD will keep the MemWait active for a longer period inserting extra wait states (Fig. 5.).

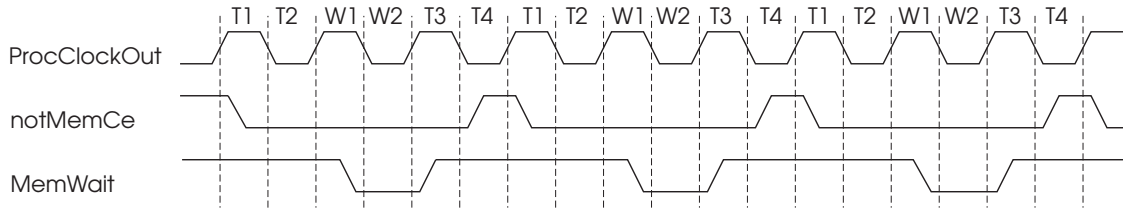


Fig 5. Wait state timing with one wait state

Another problem is the bus turnaround time of the T222 (this is the time between two notMemCe cycles). Most I/O devices have a so–called *data hold* time. This is the time that the device will hold the data on the bus after the read signal has gone away. However, the bus turn around time of the T222 is about 20 nano seconds. This is often too short for slow I/O devices and will cause a bus conflict if the next bus cycle is a write cycle. For this reason the so–called *release states* are introduced. These states are the number of clock periods the bus buffers stay in tri-state after a read cycle. Using these release states, the turnaround time for the I/O device can made longer (BnotMemCe) than the bus turnaround time of the T222 as illustrated in Fig. 6.

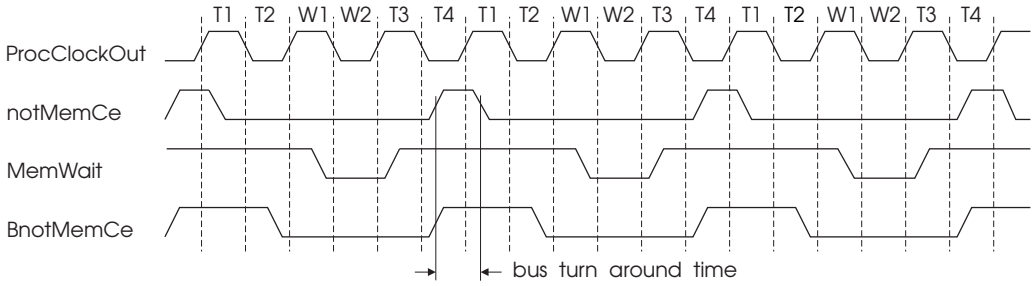


Fig 6. Release state timing with one release state

3.2 TRAS memory map

The memory map of the TRAS is divided into three parts e.g. RAM, ROM and I/O. Since the selection of these parts is done with an EPLD, the size of these memory parts can be tuned to the application connected to the TRAS. The memory map of the TRAS is implemented with a function table which looks like:

```
$(A[15..8]): RamCE, RomCE, SlowIO, FastIO;
   07Ch    :  0   ,  0   ,  1    ,    0  ; Slow IO page
   07Dh    :  0   ,  0   ,  0    ,    1  ; Fast IO page
07Eh..07Fh :  0   ,  1   ,  0    ,    0  ; ROM memory
   REST    :  1   ,  0   ,  0    ,    0  ; RAM
```

A logical one after the colon in this table indicates the activation of the memory part. This way any configuration of memory and I/O space may be realised. To obtain different numbers of wait and release states for different parts of the memory, the wait state generator and the release state generator are implemented with a state machine in the EPLD. This state machine refers to a function table which looks like:

```
$(A[15..8]):(NrWaitStates[3..0]),(NrReleasestates[3..0]);
   07Ch    :         8D         ,         9D          ; Slow IO page
   07Dh    :         0D         ,         0D          ; Fast io page
07Eh..07Fh :         4D         ,         1D          ; ROM memory
   REST    :         0D         ,         0D          ; RAM
```

In this function table the memory sections are given before the colon. After the colon the number of wait and release states for these sections are given. This allows different parts of the memory to have different numbers of wait and release states.

The TRAS supports the following features:

- Variable RAM, ROM and I/O space sizes and locations.
- DMA support.
- Event signals (interrupts).
- VarClock support for sampling and synchronisation of the I/O boards.
- User definable control signals (spare EPLD pins).
- A built-in wait state generator that can be tuned for each I/O device separately.

Because of the standard design of the TRAS, the application engineer can put his effort in designing the I/O application.

4. The Optical Transputer Link

The transputer link engine was originally designed for local communications on short distances. However in quite a few situations , we would like to distribute our transputer network over much longer distances. In industrial control environments for example, one could imagine several production processes to be part of a large transputer network.

In our laboratory, we use a Meiko* computing surface with 48 transputers to control several applications distributed over the laboratory. Each application is controlled by a local Twente LINX system with several transputer data acquisition boards and some T800 transputers for local computing power. The local LINX systems are connected to the central Meiko computing surface with optical links.

Using RS422 it is possible to extend the length of transputer network to about 30 meters at a link speed of only 5 or 10 Mbits/s. This is still not enough. Therefore an optical transputer link connection was designed using information from the Inmos application note [3]. The Inmos design was for a link speed of 5 Mbit/s, our aim was to maintain our overall network link speed at 20 Mbit/s at distances of at least 50 meters.

The advantages of an optical link are:

- no crosstalk
- large bandwidth
- electrical isolation
- no external noise

Disadvantages are:

- skew due to optical dispersion and interface logic
- lower communication bandwidth

* Purchased with a research grant of the Esprit Parallel Computing Action project nr. 4122

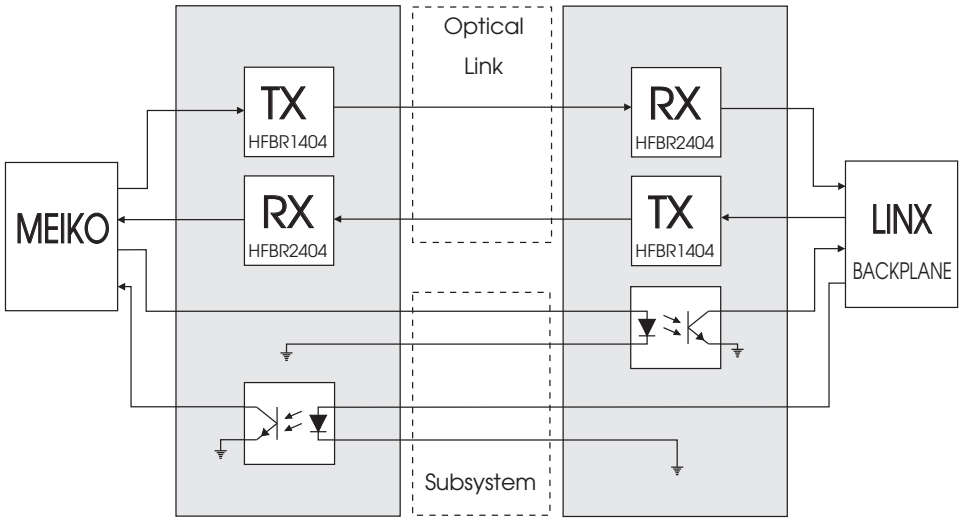


Fig. 7 Optical interface.

In Fig. 7 a block diagram of the optical link is given. The optical link consists of an optical fibre, the subsystem connection consists of an electrical wire using opto couplers for isolation.

There are two types of optical transmitters and receivers, these are:

- AC type of transmitters and receivers. AC receivers and transmitters have a high-pass filter, the optical sensitivity depends on the spectrum of the incoming data. When we look at the communication protocol of the transputer link, the link is ’0’ i.e. 0 Volt if there is no data, a continuing stream of zero’s (or one’s) is not received and the output of the receiver is undefined. So when using AC of receivers, some coding of the link signal has to be done to avoid a constant stream of ’0’ (or ones) on the transmitter input.
- DC type of transmitters and recievers. The disadvantage of using DC type components is that the interface will be more sensitive to external noise. Therefore great care has to be taken in the design of the printed circuit board.

Because a AC transmitter and receiver will cause significant more logic in the transmitter and receiver interface we decided to take the DC transmitters and receivers. The optical transmitter used is a HFBR1404 and the receiver is the HFBR2404 from Hewlett-Packard [4]. The optical fibre cable is the 50/125 of AMP. The optical components are DC receivers and transmitters.

Because an optical connection is rather expensive compared to an electrical connection, we decided to build the subsystem interface using normal electrical wire. However it is possible to use optical fibre as well.

4.1 Data rate of the Optical link

One of the disadvantages of extending the length of a link is that it takes more time for the data to arrive at the receiving transputer. The acknowledge will arrive later at the sending transputer. This will cause a lower communication bandwidth of the link.

As mentioned before we based the design on an Inmos application note [3]. However, the data rate does not match the equation on page 19 of the application note. The measurements showed that the data rate drops faster when extending the link length. Because not all the data needed

for the calculation of the data rate are given in the data books, this equation was extended with data obtained from the measurements. In Fig. 8 the measured timing and characteristic parameters are shown.

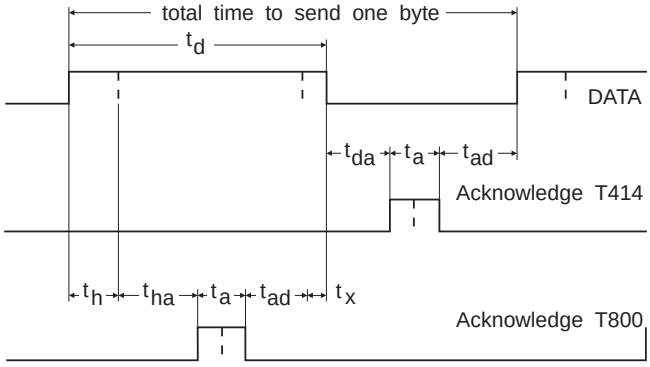


Fig. 8 Link timing for the T414 and the T800.

Variables obtained from the data books are R, t_h, t_d and t_a. Variables that are obtained from a T414 and a T800 measurement are t_s, t_{da}, t_{ad}, t_{ha},t_m and t_x. The time t_x is the effective slack between the time the acknowledge has been processed, and the time the acknowledged transmission has been ended. The variables t_l and t_c have been obtained from the data sheets of the components used. Using this extra information results in the next equations.

For the T414 link: $$R_e = \frac{1}{t_d + t_a + t_l + t_c \cdot l + \frac{t_s}{D_b} + t_{da} + t_{ad} + 0.25 \cdot t_m} \quad [byte/s]$$

For the T800 link: $$R_e = \frac{1}{t_h + t_a + t_l + t_c \cdot l + \frac{t_s}{D_b} + t_{ha} + t_{ad} + 0.25 \cdot t_m + t_x} \quad [byte/s]$$

$$t_x = \begin{cases} t_y \text{ when } t_y > 0 \\ 0 \text{ when } t_y \le 0 \end{cases} \qquad t_y = (t_d - t_h - t_{ha} - t_a - t_{ad}) - (t_l + t_c \cdot l)$$

Where:

- R Link speed in [bytes/s]
- R_e Effective data rate [byte/s]
- t_l Delay of interface logic [s] (buffers etc. in our case 100 ns)
- t_c Delay of the optical cable [s] (for a duplex cable this is 2 * 5 ns/meter)
- l Length of the cable [m]
- t_s Link setup time [s] 1 µs
- D_b Size of the data block sent in bytes (in our case 512 bytes)
- t_{da} Time after which ack is send if a byte is received, T414 250 ns, T800 200 ns
- t_{ad} Time data is sent after a ack is received, T414 225 ns, T800 200 ns
- t_m Delay due to memory access every four bytes, T414 400 ns, T800 50 ns
- t_{ha} Time after which ack is sent if header is received, T800 150 ns
- t_h Time header takes (2 bits), $\frac{2}{R}$
- t_d Time one byte takes (byte plus two start bits and one stop bit), $\frac{11}{R}$
- t_a Time acknowledge takes (one ack bit and one stop bit), $\frac{2}{R}$

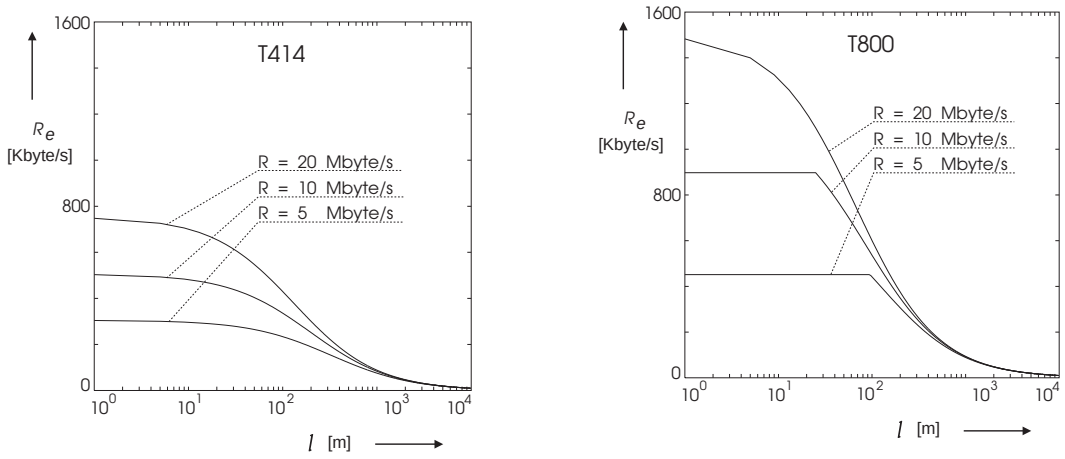


Fig. 9 Effective data rate versus link length for the T414 and the T800

The graphs (Fig. 9) show that extension of the length *l* of a link results in a significant drop of the data rate R_e. Also the delay due to link buffering or link switches will have a similar result. So if one wants to extend the link one should bear in mind the data rate needed for the application. If the link becomes more than 500 meter it does not matter what link speed is used. It is even better to go to a lower link speed because the link engine will tolerate more skew due to optical dispersion.

5. Sampling with the LINX backplane

Sampling in conventional systems is done with a multiplexer, a sample and hold (S/H) and an A/D converter as illustrated in Fig. 10.

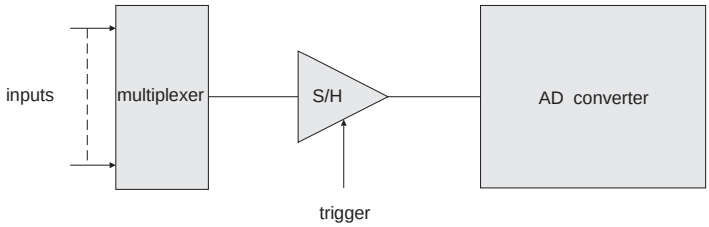


Fig. 10 Conventional A/D converter system

This method of sampling causes the samples to be shifted in time (Fig. 11), which will cause a phase error in the measured signal.

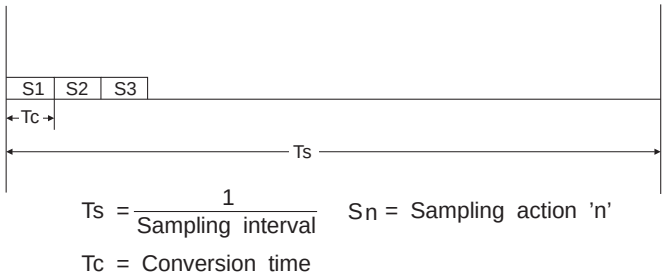
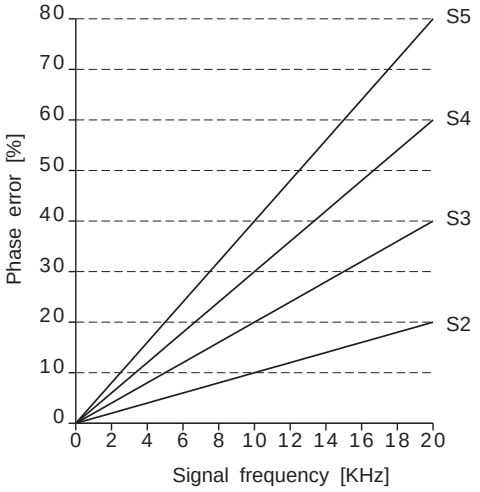


Fig. 11 Samples shifted in time

If the conversion time is low compared to the sampling interval, the assumption can be made that the samples are taken all at the same time, ignoring the error. If the conversion time becomes relatively large compared to the sampling interval, the phase error can no longer be ignored (Fig. 12).



The phase error is:

$$\varphi_n = n \cdot \tau \cdot f_s \cdot 100\%$$

Where:

τ	Conversion time
n	Sample number
f_s	Signal freqency
φ_n	Phase error of sample n

Fig. 12 Phase error at a fixed conversion time of 10 μsec

A better solution is to put a sample and hold on each input followed by the multiplexer. The advantage is that all signals are sampled at the same time. The total conversion time does not decrease because the A/D converter still has to do all conversions. This leaves less time for the computation of the control algorithm.

A second solution is to use for each input an A/D convertor. This has the advantage that there is just one conversion needed, which leaves more time for the computation of the control algorithm. However this solution is rather expensive.

In conventional systems a conversion is started by the processor. When sampling is done in this manner, the processor needs to be interrupted at equidistant points in time. Because the processor has to be interrupted, interrupt latency will occur, which will cause jitter. An additional problem in multi-processor systems is the synchronization between processors [5]. For this reason the VarClock signal was provided on the backplane. This way all the processors are synchronised, and all I/O devices on boards in the backplane are started at the same time (see Fig. 13). There will be no jitter because the VarClock is derived from a crystal controlled clock.

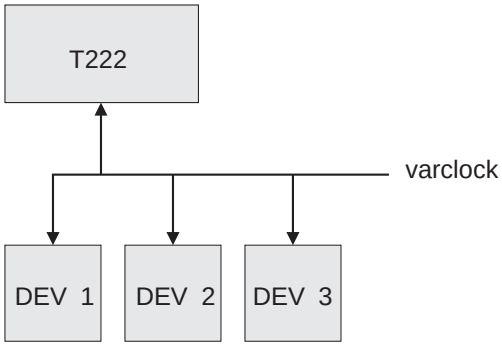


Fig. 13 Sampling with the varclock

6. Results

The LINX backplane and a number of TRAS I/O boards have been designed and implemented. These boards are:

- LINX TRAM-mother board. This is an INMOS B008 compatible TRAM mother board with 8 slots. It can be configured with two C004 link-switches.
- A/D-D/A board. This board has two A/D and two D/A converters. The A/D converters have an optional multiplexer on the output. These multiplexor should be omitted if high sampling frequencies are required.
- RDC A/D D/A board. This board has a Resolver to Digital Converter (an absolute angle encoder) with a velocity output, an A/D converter and a D/A converter. Especially useful for measuring angles and angular velocities for controlling servos.
- Digital I/O board. This is an digital I/O board with 96 programmable I/O pins and a counter/timer.
- TRAS prototype board. This board has a speed–wire prototyping area.

All these boards except for the TRAM mother–board are based on the TRAS. This made it possible to do the design and implementation of the digital I/O board in just three weeks. To connect the I/O systems to a central transputer cluster (a Meiko computing surface), an optical link board was designed for the LINX backplane. The optical link can be used at a speed of 20 Mbit/s over a distance of 50 meters, using low–cost optical components.

References

[1] A.W.P. Bakkers and J. van Amerongen, Transputer based control of mechatronic systems, 11th IFAC World Congress, Tallinn, Estonia, August 13-17 1990, Vol. 7, pp. 128-133, proceedings to be published by Pergamon Press.

[2] K.C.J. Wijbrans, J. Meijer and A.W.P. Bakkers, *Real-time sampling subsystem for the PC/AT*, Journal A, Vol. 30, Nr 3, September 1989, pp. 9-14.

[3] M. Rygol and T. Watson, *Connecting Inmos Links*, technical note 18, INMOS Ltd, April 1987.

[4] *Low-Cost Fiber-Optic Transmitter Interface Circuits*, application bulletin 73, Hewlett–Packard, June 1987.

[5] M. Shumway, Synchronizing Clocks in Multi–Transputer Networks, Proceedings of the 7th Developers Symposium "Transputer", München, October 1989, pp. 379-382, ISBN-89090-604-4.