

A multi-step P-cell for LNA design automation

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Abstract—This paper presents a novel way to efficiently implement parametric cells (P-cells). A narrow-band LNA is used as demonstration vehicle. In the P-cell, circuit parameters such as transistor size, bias condition and passive values are determined automatically for any given reachable target performance. To achieve both high accuracy and relatively high speed, a new iterative stepped approach is used with respect to speed and accuracy, starting with moderate-accuracy and fast optimization that yields the starting point for the next higher-accuracy and slower optimization step. The presented approach can be extended to other types of circuits.

I. INTRODUCTION

The low noise amplifier (LNA) is a critical building block in any RF front-end; it has an important effect on the noise performance of the overall system. As the market for wireless communication expands, the need for LNA with demanding performance specifications is increasing. However, like any other RF block, the design of LNAs is a time-consuming task that typically relies heavily on the experience of RF designers. LNA design automation can significantly simplify the design task and shorten the design-to-market time.

Available LNA design automation is mainly based on circuit synthesis [1-3]. Starting at some initial circuit component values such as transistor size, bias condition and passive values, the circuit performance metrics are calculated and then a cost function is evaluated. Typically, the calculation of circuit performance is done using conventional analog circuit simulators. Adaptation of circuit component values is done using e.g. a gradient descent algorithm that optimizes the pre-specified cost function. Already for small sized circuits the number of parameters is large and numerical optimization costs lots of time, while there is usually no guarantee that the algorithm finds a solution. In mathematical terminology the main problems are due to the large search space and sticking in local minima.

To speed up the LNA design automation process a novel multi-step approach is proposed that can solve the traditional drawbacks of optimization:

- The user selects a circuit topology and specifies target performance metrics, which are inputted to the P-cell. A straight-forward extension is that also the best performing (optimized) circuit out of a set of circuit

topologies is selected automatically by the P-cell based on defined cost function evaluation.

- The P-cell first makes a coarse optimization of circuit component based on the input specifications. This first step uses circuit analyses for noise and harmonics modeling. A built-in interface with state-of-the-art MOS models such as MOS model 11 (MM11) [4] or PSP [4] extracts the information of intrinsic noise and nonlinearities of the transistor. As a result this first step has moderate accuracy but is very fast.
- The result of the coarse optimization is used as starting point for a numerical optimizer, wrapped around conventional simulators such as Spectre [5]. Because of the relatively good starting point for the numerical optimizer this second optimization is very fast.
- The results of the second optimization can be used as settings for the layout generation. Extraction and optimization on the extracted circuit, taking into account layout parasitics (including those of passive components) and variability, can increase accuracy at a significant calculation time penalty.

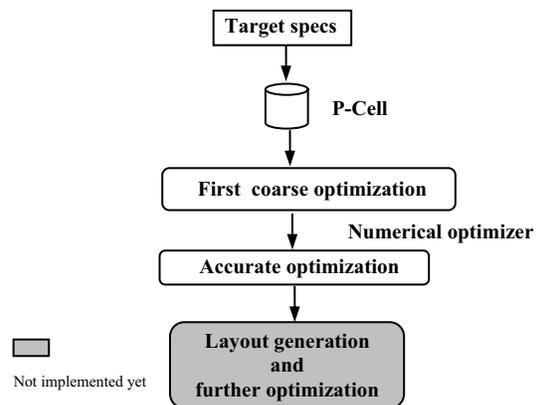


Figure 1. Block diagram of the multi-step approach for LNA design automation.

This paper is organized as follows. Section II discusses the approach for the building of P-cell. Section III discusses the implementation of the P-Cell, which consists of the LNA modeling and numerical root-finding. Section IV demonstrates

the design automation of a narrow band LNA using the proposed multi-step approach.

II. P-CELL BUILDING APPROACH

The goal of the P-cell is illustrated in Fig. 2: for any specified target circuit performance, the P-Cell first chooses the optimal LNA topology and then calculates the optimal values for each circuit component. In other words, the P-Cell determines the circuit parameters such as transistor size, bias condition and passive value automatically for any given circuit performance specifications, which is a reverse-direction approach compared with the commonly-used approach in the synthesis [1-3] (calculating the circuit performance metrics from chosen circuit parameters).

As the first step in the optimization process carried out in the P-cell, a coarse circuit optimization is done. This coarse optimization is fast and with moderate accuracy in reaching the target performance metrics. The realization of the reverse-direction approach is based on two blocks: LNA modeling and numerical root-finding, as illustrated in Fig. 3.

- In the **LNA modeling** block, small signal analyses including noise and harmonics are performed. State-of-the-art MOS models such as MOS model 11 or PSP [4] are embedded in the P-cell providing direct access to MOS transistor parameters and properties. As a result, the mathematical link between the LNA performance metrics with the circuit parameters such as bias, component values is built.
- **Numerical root-finding.** Based on the mathematical link built by the LNA model, the numerical root-finding algorithm performs the reverse-direction calculation for any given circuit performance metrics, which determines the value of the circuit parameters.

III. IMPLEMENTATION OF THE P-CELL

To demonstrate the multi-step design automation approach, a P-cell for the narrow-band inductively degeneration common source (IDCS) LNA [6] shown in Fig. 4a is implemented.

A. LNA Modeling

The linear small signal model in Fig. 4b is used to calculate the noise performance, input and output impedance and gain. All the parasitics of the transistor such as C_{gd} , C_{gs} , C_{ds} , r_{ds} are accounted for. The noise sources included are

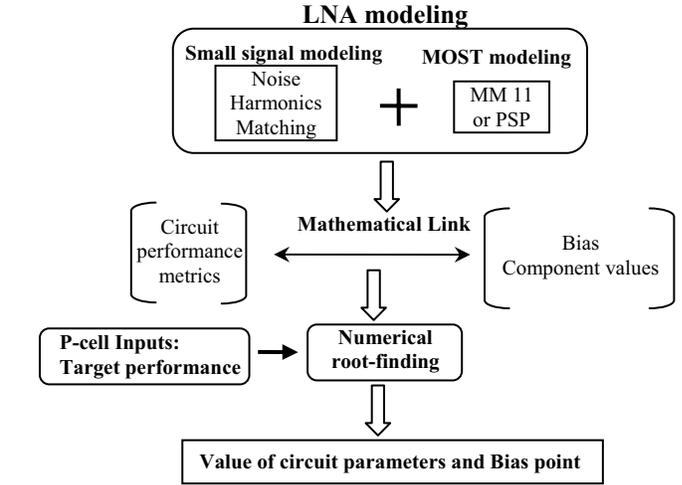


Figure 3. Block diagram of the reverse-direction approach in the P-Cell.

namely, gate induced noise $\overline{i_{g,n}^2}$, channel noise $\overline{i_{d,n}^2}$, flicker noise $\overline{e_{flicker,n}^2}$, parasitic resistance noise of gate and source inductors $\overline{e_{Lg,n}^2}$ and $\overline{e_{Ls,n}^2}$, resistive load noise $\overline{e_{Rload,n}^2}$.

In most of the previous work on LNA nonlinearity modeling, only the transconductance nonlinearities are taken into account [1], [6-8]. However, we have observed that for short channel MOST with moderate voltage gain also the nonlinear output conductance and cross modulation terms play a big role. For operating frequencies higher than 1 GHz the effect of the transistor's nonlinear capacitances also becomes important. Aiming for fairly accurate nonlinearity modeling a complete weakly nonlinear model is used shown in Fig.4 (c). This model includes four nonlinear current sources, namely, $i_{Rds}[v_{gs}(t), v_{ds}(t)]$, $i_{Cds}[v_{gs}(t), v_{ds}(t)]$, $i_{Cgs}[v_{gs}(t), v_{ds}(t)]$ and $i_{Cgd}[v_{gs}(t), v_{ds}(t)]$. Source i_{Rds} accounts for the nonlinear resistive drain-source current; sources i_{Cds} , i_{Cgs} , i_{Cgd} account respectively for the nonlinear capacitive drain-source current, for the nonlinear capacitive gate-source current and for the nonlinear capacitive gate-drain current. Assuming a zero source-bulk voltage for the transistor, these four sources are functions of MOST terminal voltage v_{gs} and v_{ds} , which are described by two-dimensional Taylor series expansions. Equations (1) and (2) show the series expansions used in this work for the weakly nonlinear resistive and capacitive current sources. The Taylor series' coefficients such as g_{x11} and $C_{ds,x21}$ are extracted directly from the embedded MOS models.

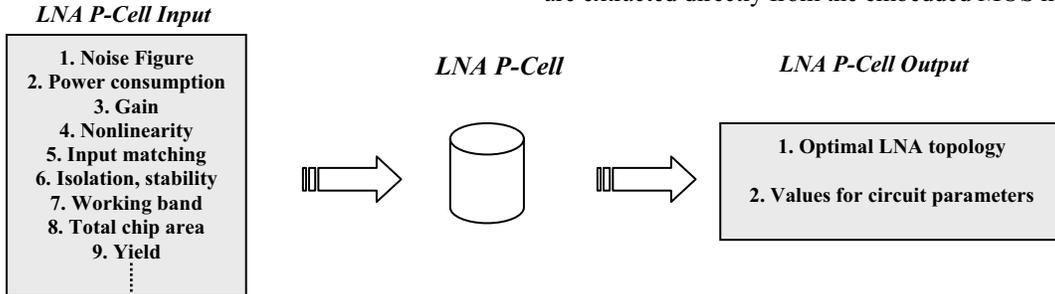


Figure.2 The function of the P-cell

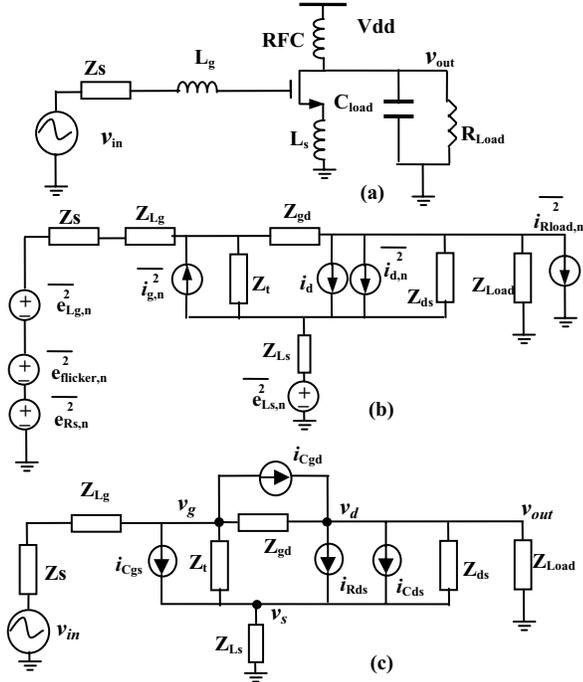


Figure 4. (a) Schematic of the IDCS LNA, (b) and its noise small signal model, (c) its nonlinearity model.

$$i_{Rds} = g_{m1}v_{gs} + g_{m2}v_{gs}^2 + g_{m3}v_{gs}^3 + g_{ds1}v_{ds} + g_{ds2}v_{ds}^2 + g_{ds3}v_{ds}^3 + g_{X11}v_{gs}v_{ds} + g_{X12}v_{gs}^2v_{ds} + g_{X21}v_{gs}v_{ds}^2 \quad (1)$$

$$Q_{Cds} = C_{dsT1}v_{gs} + C_{dsT2}v_{gs}^2 + C_{dsT3}v_{gs}^3 + C_{ds1}v_{ds} + C_{ds2}v_{ds}^2 + C_{ds3}v_{ds}^3 + C_{ds,X11} \times v_{gs}v_{ds} + C_{ds,X12} \times v_{gs}^2v_{ds} + C_{ds,X21} \times v_{gs}v_{ds}^2 \quad (2)$$

$$i_{Cds}(t) = \partial_t Q_{Cds}$$

A distortion analysis method similar to the one in [9] is used to derive the closed-form formulas for IIP2 and IIP3. To the best of our knowledge it is the first time that a complete weakly nonlinear model of transistor valid for all operating frequency has been used for LNA nonlinearity analysis. The combination of direct access to the embedded MOS model and the complete nonlinear modeling of LNA – including mixing terms and nonlinear capacitances – leads to a fairly accurate optimization result at relatively high speed for the first optimization step in the P-cell. This optimization result is then used for the numerical optimizer (second-step optimization).

B. Numerical root-finding

The mathematical link obtained in the LNA modeling provides the core relations between circuit performance metrics (noise figure NF, IIP3, IIP2, power consumption, S_{11} and S_{21}) and circuit parameters (V_{gs} , the transistor aspect ratio W/L , L_s , L_g). Under the constraint of input matching, numerical root-finding algorithms such as a Newton-Raphson (N-R) method are used to obtain the numerical solutions for the core relations, as illustrated in Fig. 5.

C. Capability of P-cell

Our P-cell implementation includes a number of functions, including:

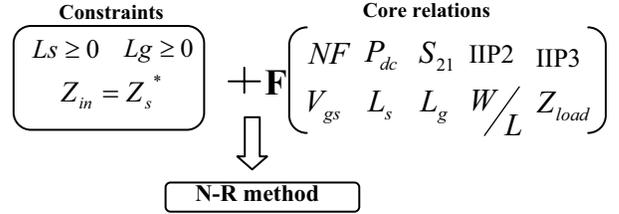


Figure 5. Block diagram of the numerical root-finding processing.

- Providing information about the reachable level of circuit performance, given some boundary conditions.
- Determination of component sizes and values for a set of target performance metrics.
- Calculation of the realizable minimum NF and maximum S_{21} , IIP2 and IIP3 for given operating conditions (operating frequency, output impedance of the input voltage source, power consumption range, load impedance and supply voltage).

IV. MULTI-STEP LNA DESIGN AUTOMATION

To demonstrate the multi-step design automation approach the IDCS LNA shown in figure 4a is designed for the operating condition listed in Table I, with various target values for NF, IIP2 and IIP3; a commercial standard 90nm CMOS process is assumed for the design

TABLE I. DESIGN VEHICLE BOUNDARY CONDITIONS

f (GHz)	V _{dd} (V)	Q _{Lg}	Q _{Ls}	P _{DC} (mW)	C _{Load} (fF)	R _{Load} (ohm)	Z _s (ohm)
5	0.6	10	10	<8	100	2000	50

An industrial numerical circuit optimizer is used as the second-step accurate optimizer. This numerical optimizer is wrapped around Spectre to optimize component values, bias conditions and more to satisfy a user-defined cost function. The optimization is done by iteratively evaluation of the (Spectre) simulation result and calculating a new set of component values and bias settings that reduce the cost function.

Firstly Fig. 6 shows the accuracy and speed of the first coarse optimization step in our P-cell for the specifications in Table 1 as a function of target NF (Fig. 6a), target IIP2 (Fig. 6b) and IIP3 (Fig. 6c). Each graph shows on the left y-axis the error between the target specification – e.g. target NF – and the actual value that follows from Spectre simulations using the exact component values and biasing settings as provided by the P-cell. The right y-axis shows the calculation time required for the P-cell on a Linux server with a 3 GHz Intel Xeon CPU and 3 GB memory. Note that within 2 seconds quite accurate results are provided by our P-cell, which is due to the fully modeling of noise and nonlinearity including e.g. conductance cross modulation terms and nonlinear capacitances of the MOS transistor.

Secondly a design example is used to show the overall performance of the P-cell with two-step optimization on hard

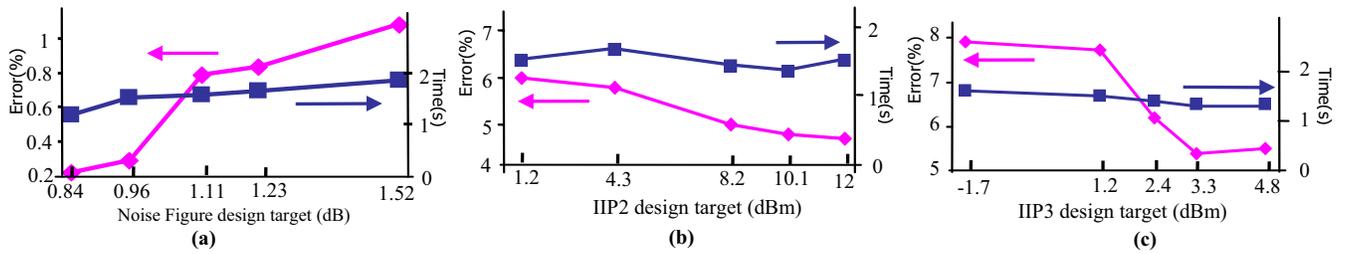


Figure.6 Benchmark of P-cell on accuracy and speed in meeting the design targets of (a) Noise figure, (b) IIP2 , (c) IIP3.

target specifications, for high performance applications. Table II lists the design targets and the Spectre-simulated performance using the exact component values and bias settings as provided by the P-cell after first coarse optimization and two-step optimization respectively. Because the first-step coarse optimization provides good initial settings for the second optimization step with high speed, the total optimization time is relatively short (around 15 seconds). Fig 7 shows Spectre simulation result of the circuit as optimized by the P-cell with two-step optimization.

TABLE II. DESIGN TARGET AND P-CELL RESULTS

	IIP3 (dBm)	IIP2 (dBm)	NF (dB)	V _{gain} (dB)	S11 (dB)	Pdc (mW)
Target	>5	>20	<1	>12	<-15	<8
P-cell (first coarse optimization)	6.55	41.39	0.862	13	-28	6.2
P-cell (two-step optimization)	6.6	42	0.86	13.8	-29	6

V. CONCLUSION

A novel way to build a P-cell for RF blocks is presented, implementing a multi-step approach in which the accuracy in the first step is moderate which yields high speed operation. Next steps have increasing levels of accuracy and use the result of the previous step as initial guess, which yields overall high speed and accurate operation. With the good noise and nonlinearity modeling – due to the inclusion of all nonlinear conductance and capacitances controlled by v_{gs} and v_{ds} – the high speed and good accuracy of this multi-step design automation approach was demonstrated on a narrow-band LNA design.

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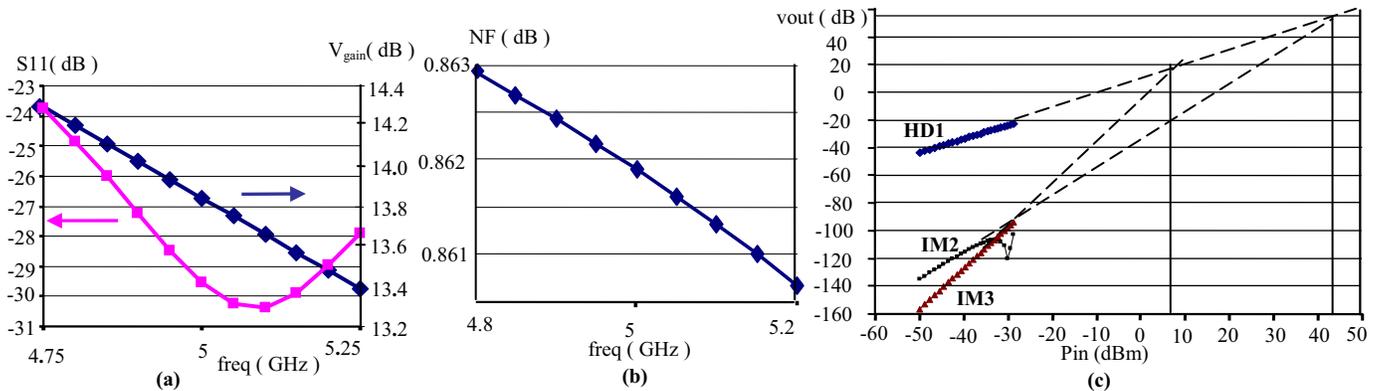


Figure.7 Simulation result of the circuit designed using P-cell (a) V_{gain} and S_{11} , (b) noise figure , (c) IIP3 and IIP2.