ORGANIC LAYERS ON SILICON RESULT IN A UNIQUE HYBRID FET

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Abstract: A Field-Effect Transistor (FET) is presented that combines the conventional lay-out of the silicon substrate (channel and source and drain connections) with a Si-C linked organic gate insulator contacted via an organic, conducting polymer. It is shown that this hybrid device combines the excellent electrical behavior of the silicon substrate and the ease of use and good properties of organic insulators and contacting materials.
Keywords: organic monolayer, FET, conducting polymer

INTRODUCTION

Fully molecular electronics have drawn a lot of attention over the past years [1] as potentially low-cost alternatives for silicon-based electronics. However, the superior electronic properties of the silicon-based devices have not yet been matched [2]. On the other hand, fully silicon-based FETs have reached the fundamental limits of the size of the SiO_2 gate insulator and alternatives are being pursued, mostly inorganic metal oxides [3]. We propose a combination of both worlds. A hybrid FET device is presented of which the gate insulator is replaced by a Si-C linked, organic monolayer and the gate contact is made via an organic, conducting polymer as shown in Figure 1.

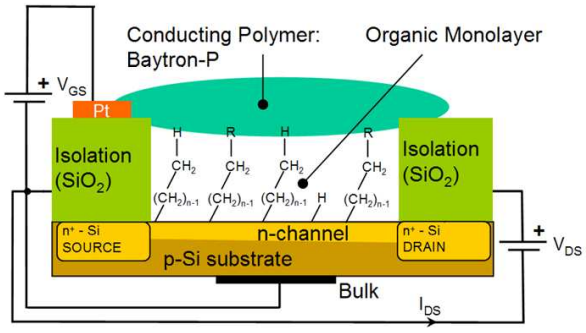

Figure 1. Schematic representation of a hybrid FET.

Apart from the gate insulator and gate contact the FET is made according to a classical, inorganic lay-out.

The organic monolayer in this Figure is an alkyl-monolayer directly linked to the silicon surface without any intermediate oxide [4-6]. Physically, such monolayer offers advantages such as a precisely tunable thickness via the chain length *n* (Figure 1) and a well known surface profile since the monolayer follows the underlying silicon surface profile. Electrically, the monolayer offers good surface passivation (i.e. low amount of surface states) [7-9] and since no intermediate thin oxide layer is present that in most cases is native oxide of poor and uncontrollable quality, capacitive structures of such monolayers are well defined. This is crucial for use in FET based devices with certain desired properties.

The gate contact in this study consists of a PEDOT:PSS conducting polymer [10-11]. This is a commercially available, conducting polymer and offers easy processability and flexibility since it can be applied via spincoating or titration. Furthermore, it shows a simple tunability of the conductivity, of which the mechanism has been investigated recently in detail [12]. The material has found its way as electronic conductor in for instance organic thin film transistors [11, 13-14] and as electrode material on metal-insulator-metal (MIM) structures like Au - organic thiol-monolayer – PEDOT:PSS/Au [15].

EXPERIMENTAL

Electrical characterization of PEDOT:PSS.

Several wafers (4", p-type, 5-10Ωcm, Okmetic Inc.) were thermally oxidized with 233nm of SiO_2. Hereafter, PEDOT:PSS layers were spincoated on the wafers using different rotation speeds (500, 1000, and 2000 rpm). The PEDOT:PSS was prepared according to the Baytron-P CPP 105D formulation using commercial available chemicals [16] and was applied to the wafers via a 800nm sieve. The layers were cured on a hotplate for 10 minutes at 120° C. The thicknesses of all layers were checked via a profilometre (Veeco Dektak 8) and were 215nm, 111nm, and 69.0nm for the layers spun at 500rpm, 1000rpm, and 2000rpm, respectively. Electrical contact was made via silver paint electrodes (EPO-TEK H20E) placed at several distance from each other (2, 4, 8, 16, and 32 mm, respectively) as illustrated in Figure 2. As a reference, electrodes were mounted on a wafer without PEDOT:PSS on it.

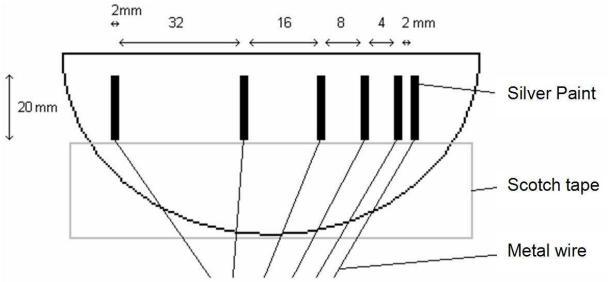

Figure 2. Schematic drawing of wafer connections for resistivity measurements.

Subsequently, electrical impedance measurements were performed on a HP4194A Impedance Analyzer using frequency sweeps from 100Hz to 1 MHz. DC measurements were performed using a HP34401A multimeter.

The hybrid field effect transistor.
Chips with FETs were made using a standard FET process [17]. The channel width *W* of the FETs is 500 µm and the channel length *L* is 15 µm. The wafers were sawed into pieces of 18mm x 24 mm. A single piece contained 24 FETs. Next, the gate area was etched open and the 1.8 nm thick, Si-C linked monolayer (Si-$C_{16}H_{33}$) was attached [18]. Hereafter, a drop of aqueous dispersion of conducting polymer PEDOT:PSS was placed on top of the gate area and cured, all according to the same recipe as mentioned above. As a reference, FETs (Si-H FETs) were used from which the gate area was etched open using 1% HF after which directly a drop of PEDOT:PSS was placed and cured. The resulting FETs (see Figure 1 for a schematic representation) were characterized using a HP4156C Semiconductor Parametric Analyzer. In the first measurement I_{DS} and I_{GS} were measured as a function of V_{DS}, which was swept from 0V to 3V in 101 steps. V_{GS} was increased after each sweep and varied from 0V to 2V in steps of 0.25V. In the second measurement I_{DS} and I_{GS} were measured as a function of V_{GS}, which was swept from 0V to 2V in 101 steps. V_{DS} was increased after each sweep and varied from 0V to 3V in steps of 0.5V.

RESULTS AND DISCUSSION

Electrical characterization of PEDOT:PSS.
In Figure 3 the Bode diagram of the impedance measurements is plotted for the different test wafers; shown is the data for the electrode distance of 8mm.

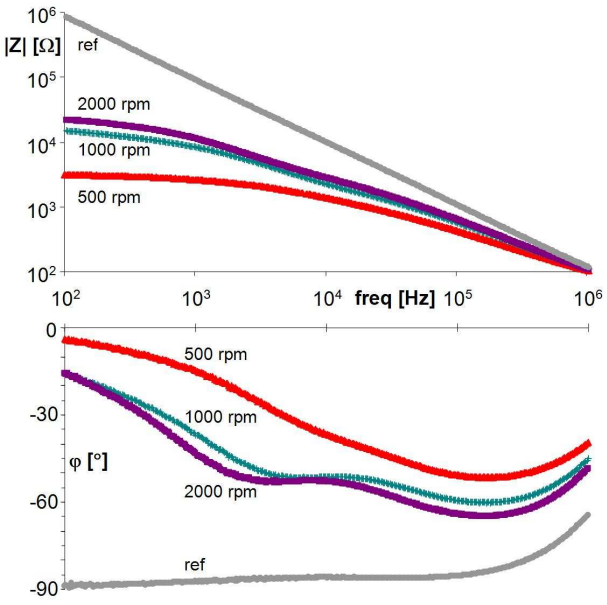

Figure 3. Bode diagram for wafers with different PEDOT:PSS thicknesses and 8mm electrode distance.

As can be expected the measured resistance drops for thicker films. Even at the lowest measured frequency of 100Hz the film did not behave purely resistive as can be seen in the phase diagram. We think that that in the frequency range from 100Hz – 2kHz the film behavior shows a transition from resistive to capacitive behavior. In this regime the film resistance can then be simply extrapolated using a RC parallel model. The thus derived AC film resistance is compared with the measured DC resistance. The resistivities, averaged over all distances and film thicknesses, were 0.32 ± 0.13 Ωcm and 0.38 ± 0.15 Ωcm for the 100Hz and DC data, respectively and thus showed a good match. These values are in agreement with the data of the supplier [16]. We found that the resistivity did increase for decreased film thickness with a factor of 2 between the 500rpm (215nm) and 2000rpm (69.0nm) data. The resistivity is nonetheless even for thin layers low enough to serve as a proper gate contact. At the frequency range between approximately 2kHz – 20kHz the phase becomes constant for the thinner layers at approximately -50° resembling Constant Phase Element (CPE) behavior [19]. This indicates that charge transport through the layer becomes diffusion limited. However, since the polymer is used here as a contact gate material operated at DC or very low frequencies this behavior and behavior at even higher frequencies are not further investigated and are expected not to interfere with the purpose of this study.

The hybrid field effect transistor.
In Figure 4 typical I_{DS} – V_{DS} curves are shown for the FETs with a Si-$C_{16}H_{33}$ organic monolayer as insulator.

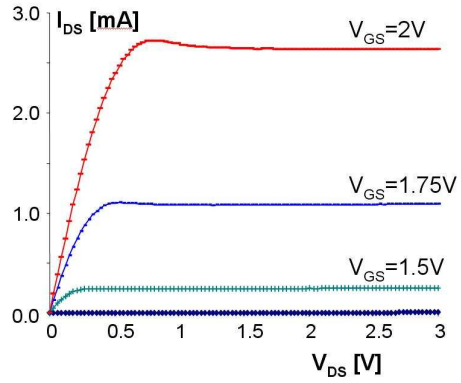

Figure 4. Typical I_{DS} – V_{DS} curves of a hybrid FET.

Typical FET characteristics were obtained. A clear distinction can be made between the triode region and the saturation region. The FETs with organic monolayers had an average threshold voltage V_{th} ~ 1.2 V, which is in the normal operating regime. In Figure 5 the corresponding I_{GS} – V_{GS} curves are shown.

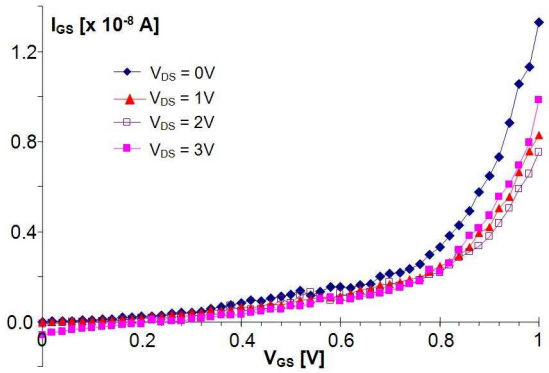

Figure 5. Typical I_{GS} – V_{GS} curves of a hybrid FET.

The current increases exponentially with the voltage. The maximum insulator leakage current density $J_{GS,max}$ at V_{GS} = 1 V and V_{DS} = 0 V was 27mA·cm^{-2} which can be considered low for such thin, wet-bench-made organic layers as compared to SiO_2 insulators of similar thickness [3].
Remarkably enough the Si-H reference FETs even showed lower leakage currents than the hybrid FETs as can be seen in Figure 6.

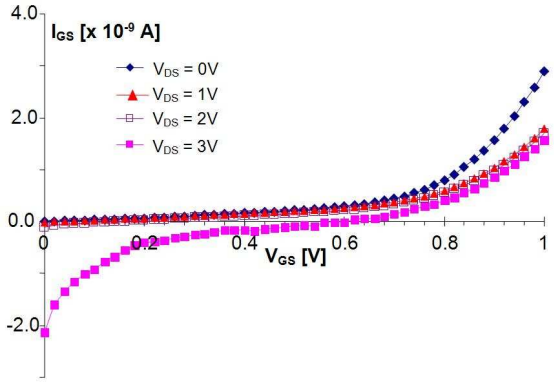

Figure 6. Typical I_{GS} – V_{GS} curves of a Si-H FET.

The leakage currents in the reference FETs were one order of magnitude lower than the FETs with organic monolayers. We expect that during curing of the PEDOT:PSS gate contact a native, wet oxide was grown. The PEDOT:PSS solution is an aqueous dispersion and is cured at 120° C for 10 minutes. We expect that the water and dissolved oxygen in the film are able to oxidize the silicon surface and form an insulating layer, especially at this elevated temperature. The fact that leakage currents are a tenfold higher for the hybrid FETs indicates that such reoxidation did not occur (to such a large scale) as on the Si-H FETs. This is also not expected since the monolayer is hydrophobic and water repellent [4-5]. This assumption is also supported by a recent, electrochemical study on the pH sensitivity of such monolayers. Measurements and simulations showed that only few oxide groups were formed in contact with water [20].

CONCLUSIONS

A hybrid FET was proposed that combines the conventional lay-out of the silicon substrate (channel and source and drain connections) with a Si-C linked organic gate insulator contacted via an organic, conducting polymer PEDOT:PSS. PEDOT:PSS was investigated for its suitability as low-ohmic gate contact and at low-frequency operating conditions (< 1 kHz) it was found to be low ohmic and mainly resistive with an average resistivity of about 0.3 - 0.4 Ωcm. The resistivity did show a dependence on the film thickness. The resulting hybrid FET devices showed classical FET behavior combined with relatively low gate leakage currents as compared to inorganic insulators of similar thickness. The threshold voltages were all in a moderate range of about 1.2V. The electrical properties can thus be regarded as good given the simple, low-temperature preparation methods of the organic layers. In this hybrid FET device the excellent properties of the silicon substrate are maintained with the combination of easy-to-apply organic gate insulators and a gate contact. Furthermore, we expect that for the future a large variety of desired FET characteristics can be obtained via the chemical tuning of the organic layer (length and polar behavior).

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