FABRICATION SCHEME FOR DENSE AQUATIC FLOW SENSOR ARRAYS

N. Izadi, M. J. de Boer, J. W. Berenschot, R. J. Wiegerink, T. S. J. Lammerink, H. V. Jansen and G. J. M. Krijnen

Transducers Science & Technology group, MESA+ and Impact Research Institutes
University of Twente, P.O. Box 217, 7500 AE Enschede, The Netherlands
*Corresponding author: N. Izadi, phone: +31 53 4894438, email: n.izadi@ewi.utwente.nl

Abstract: A fabrication scheme to realize dense arrays of flexible, closed membranes with a small gap separating them from the substrate is presented. These membranes are the first step towards aquatic hair based flow sensors biomimicking fish lateral line. Electrodes are integrated underneath the membrane to avoid contact with the liquid. Arrays of membranes with a diameter of 100 µm, gap height of 3 µm, and mutual distance of 200 µm have been successfully fabricated.
Keywords: Biomimetic, Closed membrane, Flow sensor, SU-8

INTRODUCTION

In fish the lateral line is a sensory organ used to perceive water movement in the surrounding environment to localize prey or predators, avoid obstacles, for schooling and more [1]. The lateral line consists of many mechanoreceptors called neuromast, which are groups of hair cells covered by a jelly-like cupula. There are two types of neuromasts: superficial neuromasts which are situated on the skin, and canal neuromasts which are located in canals that are connected to the water through a series of pores [2] as shown in Figure 1.
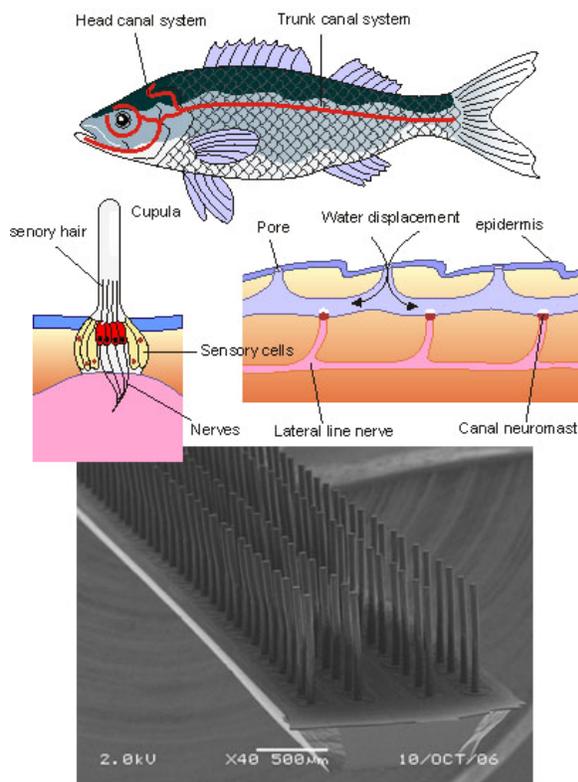

Figure 1. Top: Schematic drawing of fish lateral line, Bottom: Artificial hair sensor for operation in air

In recent years, exploiting information gained from nature, engineers biomimic these neuromasts to build a system that allows study of hydrodynamic mechanical interactions in complex noisy environments [3]. Capacitive flow sensors for operation in air biomimicking the mechanosensory hairs of crickets have been presented in [4]. Figure 1 shows a photograph of these sensors. To adapt these sensors for an aquatic environment we need to consider the differences in medium properties. The goal is to make a dense array of hair sensors in a channel or on a surface which eases readout, increases signal to noise ratio and enhances object observation capability. To keep the advantages of differential capacitive readout [5], we have designed a process for fabrication of thin, fully supported, flexible membranes with electrodes beneath them, on top of a substrate. This prevents electrode/liquid contact which may cause electrolysis and strong damping effects associated with liquid filling the gap between the capacitor electrodes (Figure 2).

The process flow not only allows for a highly controllable distance between counter electrodes but also provides the possibility to use either SU-8 or low stress silicon rich silicon nitride (SiRN) membranes. The scheme can also be used as a platform for fabrication of other devices which need sacrificial layer etching from the backside of the wafer.
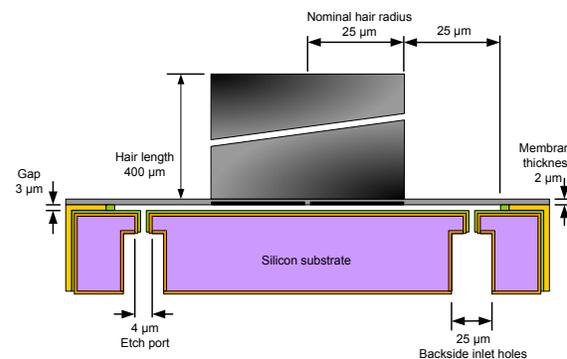

Figure 2. Schematic drawing of the sensor

Figure 2 shows a schematic drawing of the sensor structure. Fluid flow produces a drag force on the hair shaft resulting in a torque around the base of the hair which deforms the membrane asymmetrically.

The readout part consists of two separate electrodes sitting at the bottom side of the membrane and a common electrode which is actually the highly doped silicon substrate. The membrane deflection increases the gap between substrate and one electrode whilst decreasing the gap for the other, allowing a differential readout.

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FABRICATION

Figure 3 shows an overview of the fabrication process. The process starts with low resistivity (0.010-0.019 Ωcm) 4 inch silicon wafers. Double side polished (DSP) wafers are used for better control of the backside etching process (see below). Low resistivity is essential since the substrate is used as common electrode for the flow sensors' capacitance.
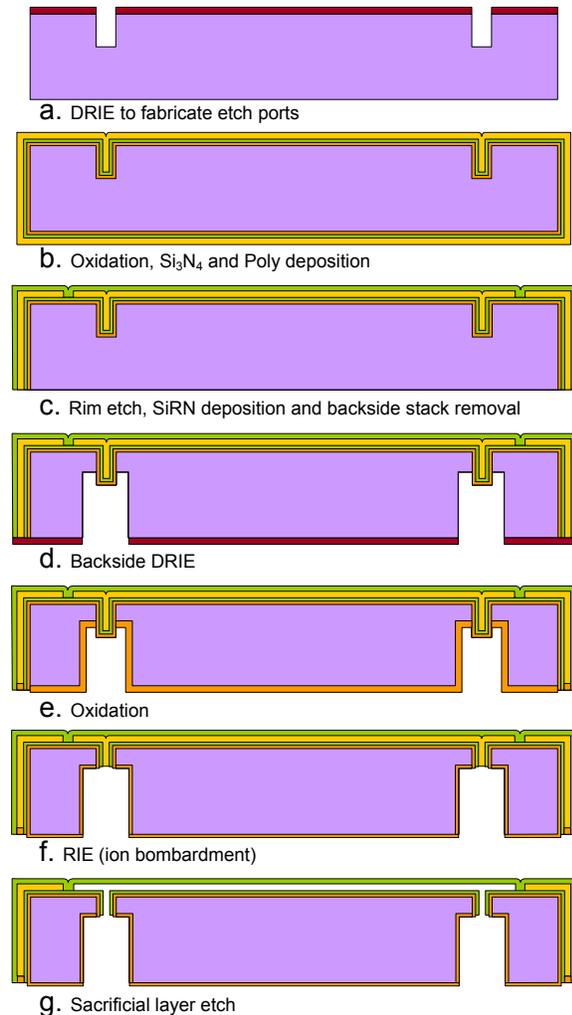

a. DRIE to fabricate etch ports

b. Oxidation, Si_3N_4 and Poly deposition

c. Rim etch, SiRN deposition and backside stack removal

d. Backside DRIE

e. Oxidation

f. RIE (ion bombardment)

g. Sacrificial layer etch

Figure 3. Outline of the fabrication process for membrane fabrication

First step after cleaning and lithography is a front side etch, using high aspect ratio Deep Reactive Ion Etching (DRIE) to make etch trenches (etch ports). Figure 3a shows a schematic cross section of the wafer. Figure 4 shows the arrangement of the ports for a single device. The depth of the ports is important. Very deep ports will slow down sacrificial layer etching by hindering diffusion of etch species. On the other hand, shallow ports need deeper backside holes to reach them. It means higher aspect ratio etch which is critical and the wafer becomes more fragile after that. Also, wide ports consume more surface of the silicon under the membrane, which decreases the common electrode area and results in a smaller capacitance. Moreover, they need thicker polysilicon deposition to close them. Experimentally, we found out that 60 μm deep and 4 μm wide port suits the application.

After this, photoresist is stripped in oxygen plasma. Figure 3b shows the next three steps: a dry oxidation to form a 100 nm oxide layer and deposition of a 30 nm layer of stoichiometric silicon nitride (Si_3N_4). The silicon oxide layer is needed to have a good connection with the sidewall oxide on the backside inlet holes (see below). The silicon nitride layer protects the sacrificial layer from being oxidized later. Both layers need to withstand the backside etch process as we shall see later. In addition, they should be removed partly before sacrificial layer etch with ion bombardment with ease. Their thickness is critical because of these contradictory requirements and has been determined experimentally (see above). Subsequently a 3 μm thick polysilicon layer is deposited. This layer will serve as the sacrificial layer under the membrane and, outside the membranes, as support for metal interconnects. After deposition of the layer stack, the wafers are annealed in N_2 at 1050 °C for an hour to lower the stress.

To define membranes and to separate the part of the polysilicon that acts as sacrificial layer from the part that should remain, we use a 2 μm wide rim filled with silicon nitride, see Figure 3c. After an etch process to delineate the rim a layer of SiRN is deposited. This layer completely fills the rim trench and protects the front side polysilicon from being oxidized in the later steps. The former is very important since metal interconnects will pass this rim to connect the electrodes to contact pads. As the rim width is ~2 μm we have to deposit >1.2 μm SiRN [6].
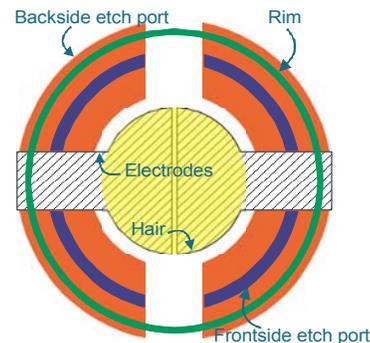

Figure 4. Mask layout of a single hair sensor

Next, the stack of layers formed on the backside of the wafer is removed and a back side etch step [7] is done using photoresist as a mask. Photoresist should be about 1.7 μm thick and must be baked at 120 °C for about an hour. Deep Reactive Ion Etching (DRIE) at cryogenic temperature (see process recipe in table 1) is done (see Figure 3d).

The process continues by stripping photoresist in oxygen plasma followed by a wet oxidation step (Figure 3e). This will create a protection layer during sacrificial layer isotropic etch.

The next step is to open the protection stack at the etch ports and expose the sacrificial polysilicon layer using a directional SF_6 based DRIE plasma with ion bombardment (Figure 3f). During this process also some of the protective oxide formed in the previous step is removed. Therefore the relative thickness of this protective oxide layer and the SiO_2/Si_3N_4 etch port protective stack should be chosen carefully (see above).

Finally, the sacrificial layer is etched to release the membranes (Figure 3g). In this step a selective SF_6

based high density plasma without self bias is used (see table 2).

RESULTS AND DISCUSSION

Figure 6 shows a close up of a fabricated circular membrane where the etch ports are clearly visible through the transparent silicon nitride.

The polysilicon sacrificial layer (Figure 3b) should be thick enough to close the etch ports, but at the same time its thickness determines the electrode separation which affect capacitance readout directly. Using 4 µm wide etch ports requires a poly silicon layer that is at least 2 µm thick. Figure 6 shows a SEM photograph of a cross section of an etch port.

Downward deflection in the membrane due to a static pressure difference is another factor affecting the gap size. The gap can be tuned to even less than 2 µm while keeping the etch ports closed by thinning the polysilicon layer after deposition by oxidation to desired depth and removing the oxide in HF.
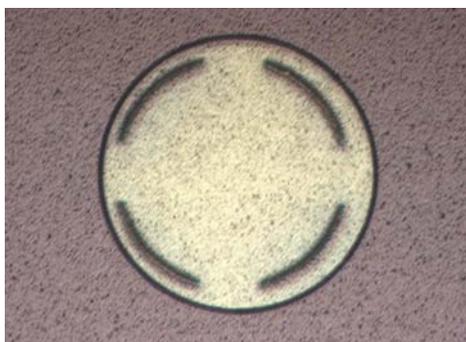

Figure 5. Photograph of a membrane with a diameter of 100 µm. The etch ports are clearly visible through the transparent silicon nitride.
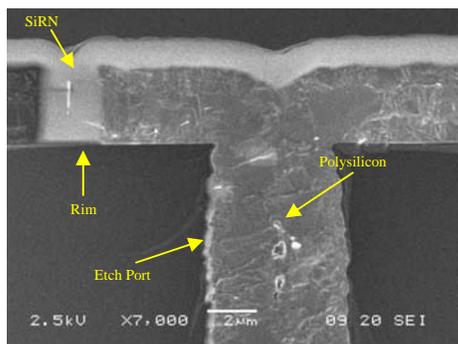

Figure 6. SEM photograph showing a cross section of the rim of a membrane and an etch port before etching of the poly silicon sacrificial layer.

The width of the protection rim around the membranes determines the minimum thickness of the silicon rich silicon nitride (SiRN) layer which also forms the membranes (Figure 3c). Therefore, this rim should be as narrow as possible considering normal mask making and lithography ability as discussed in previous section. The etch process is selected in a way to have enough selectivity and stops on Si_3N_4 layer underneath.

The backside etch is the most critical step (Figure 3d). Firstly, the etch process should be selective enough over silicon oxide and/or silicon nitride to preserve the ports. Secondly, the bottom of the etched holes

should be as flat as possible otherwise because of small misalignment it might miss the port as indicated in Figure 7. Thirdly, the etch time and selectivity should be such that photoresist can be used as etch mask, and fourth, the uniformity of etch rate over the entire wafer should be acceptable. This means while the etch process should be done so that ports are well exposed, but over-etch can remove the protecting SiO_2/Si_3N_4 stack. Besides, under-etch results in closed ports and the membrane cannot be etched free.
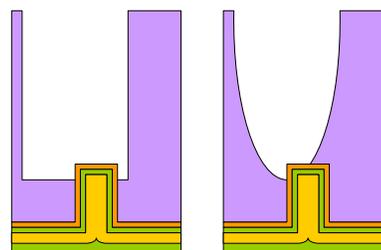

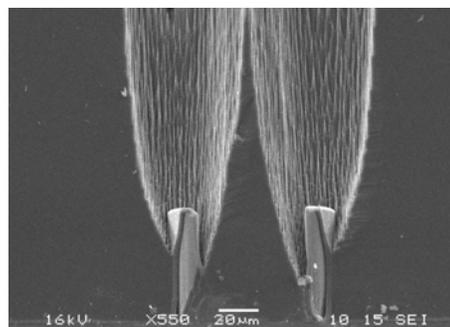*Figure 7. Detail on backside etch profile*

Figure 8. SEM of not optimized etch profile

To fulfill these requirements a new DRIE process for high aspect ratio etching of silicon was developed [7] to make a flat bottom with vertical sidewalls. This new process uses CHF_3 as inhibitor. Inlet holes with an aspect ratio of 22.5 are uniformly (±2 %) etched over the wafer, with an etch rate of 10 µm/min. Selectivity over SiO_2/Si_3N_4 stack is sufficient to stop on it: the etch rate of oxide is smaller than 10 nm/min. Etch rate for photo resist is 15 nm/min. Sidewall profile (taper) and shape of the bottom is mainly controlled by the electrode temperature and on/off time and power of CCP. In figure 8, electrode temperature was -60 °C and CCP 18 W, which was too low to create a flat bottom.

Parameters	Etch	Deposition
Gas	SF_6	CHF_3
Flow (sccm)	400	200
Time (s)	4	0.5
Priority	2	1
APC %	15	15
ICP (W)	2500	2500
CCP(W) [LF]	20	20
Pulsed (LF) ms.	20on/180off	20on/180off
He (mBar)	10	10
SH (mm)	110	110
Temperature (°C)	-120	-120

Table 1. Backside etch recipe for Alcatel Adixen SE100

In the oxidation step (Figure 3e), the thickness is determined by the selectivity of the required etch

recipe for sacrificial layer etch as well as stress considerations. Short oxidation times will not provide thick enough oxide layer. Experiments have shown that the minimum thickness of the oxide is 1 µm.

Table 2 summarizes the etch recipe for opening etch ports and sacrificial layer etch (Figure 3f and g).

Parameters	Anisotropic	Isotropic
SF_6 (sccm)	50	150
He (mTorr)	20	20
ICP (W)	600	600
CCP (W)	50	0
Temperature (°C)	20	20

Table 2. Sacrificial layer etch recipe for Oxford Plasma Lab 100

In the anisotropic process ion bombardment will remove SiO_2/Si_3N_4 protection stack and then isotropic process will selectively remove sacrificial polysilicon within rim boundaries (See Figure 9). Figure 10 shows a complete array of released membranes. It shows that the process is completely uniform and reliable.
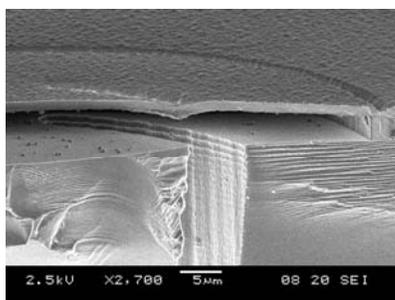

Figure 9. Cross section of a SiRN membrane after etching of the sacrificial poly silicon layer.
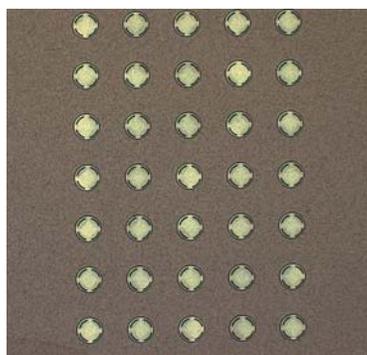

Figure 10. Uniformly released membrane array

INTEGRATION OF ELECTRODES AND HAIRS

For fabrication of complete aquatic artificial hair sensors, the sacrificial layer etch (step g in Figure 3) is replaced by the sequence shown in Figure 11. The silicon nitride membrane layer is removed and aluminum is deposited and patterned to form electrodes under the membrane and interconnects. Next, a thin layer of SU-8 is spun and selectively exposed to form the membranes and bottom of the channels. This is followed by a thick SU-8 spinning and exposure to form hairs and possibly the wall of the channels. Finally, the SU-8 is developed and the sacrificial layer is etched to release the membranes.
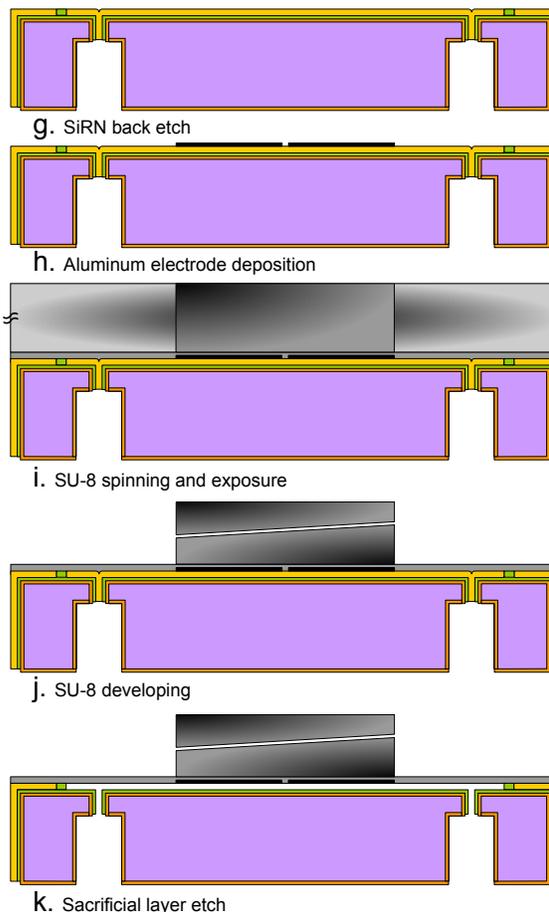

g. SiRN back etch

h. Aluminum electrode deposition

i. SU-8 spinning and exposure

j. SU-8 developing

k. Sacrificial layer etch

Figure 11. Electrodes and hair fabrication

CONCLUSION

A fabrication process was presented that allowed us to successfully realize dense arrays of fully supported SiRN membranes with full yield on 4 inch wafer. Current research focuses on replacing the SiRN membranes by more flexible SU-8 membranes. This also allows the electrodes to be integrated underneath the membranes, thus preventing electrical contact with the liquid. These structures will be used as an artificial lateral line sensor.

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