Partitioning of a DRM Receiver

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***Abstract*— In this article we present the results of partitioning the OFDM baseband processing of a DRM receiver into smaller independent processes. Furthermore, we give a short introduction into the relevant parts of the DRM standard. Based on the number of multiplications and additions we can map individual processes on a heterogeneous multi-tile architecture. This architecture can meet both the computational demands as well as the restricted energy budget.**

***Index Terms*— Digital Radio Mondial (DRM), OFDM, coarse-grain reconfigurable, Montium, energy efficiency**

I. Introduction

In the Smart chipS for Smart Surroundings (4S) project we propose a heterogeneous multi-tile hardware architecture with run-time software and tools, which determines a near optimal mapping of applications to the heterogeneous architecture at run-time. This hardware architecture contains small processing tiles interconnected by a Network on Chip (NoC) as depicted in Fig. 1. The architecture can replace inflexible ASICs as the energy-efficient solution for flexible and computational intensive applications. The processes of an application will be mapped on the tiles that can execute it efficiently or the next best alternative in case of resource shortage. Furthermore, it can support future standards, as the functionality of the chip can be reconfigured.

Such a tiled architecture has many advantages: a) tiles of the same type can be duplicated when the number of transistors grow in the next technology step, b) replication of tiles eases the verification process, c) tiles do not grow in complexity with a new technology, d) relative small tiles allow extensive optimization, e) computational performance scales about linearly with the number of tiles, f) unused tiles can be switched off to reduce the energy consumption of the chip, g) locality of reference is exploited, h) it is possible to have individual clock domains per tile, and i) for reconfigurable it is possible to do partial dynamic reconfiguration on a per tile basis.

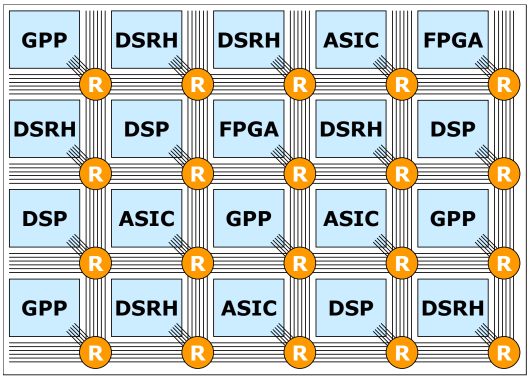

Fig. 1. An example of a heterogeneous System on Chip (SoC). DSRH = Domain Specific Reconfigurable Hardware

In the 4S project the main driver application used to validate this heterogeneous architecture is Digital Radio Mondial (DRM) [1]. DRM is the upcoming successor of AM radio and it is based on Orthogonal Frequency Division Multiplexing (OFDM) and MPEG-4 audio.

In the baseband processing of a DRM receiver several demodulation schemes have to be supported, each with their own characteristics and processing needs. Because of the semi-static switching between the schemes (in general a user will listen to a radio station for more than 1 second), we can map the processes on a combination of (reconfigurable) processors of different granularity to obtain the most energy-efficient solution. The control oriented processes with less computational intensive demands will be mapped on a flexible general purpose processor (GPP). The computational intensive processes will be mapped on an energy-efficient coarse-grain domain specific reconfigurable processor, the MONTIUM [2].

Section two of this paper describes related work to the partitioning of a DRM receiver. Next, section three explains the relevant parts of the DRM standard. In section four we describe the partitioning of the baseband processing in a DRM receiver and give the computational load of the processes. The paper ends with conclusions and future work.

II. Related Work

DRM is a relatively new standard, so there are only a few available products and papers for the receiver side. The open source project DREAM [3] develops a real-time software implementation of a DRM-receiver on a PC platform; it uses the sound card as an input and output device. The open source implementation can be used for evaluation of different algorithms, however, it is primarily designed for a GPP architecture.

Another OFDM based communication standard is HiperLAN/2. This standard has already been partitioned and mapped on a heterogeneous tiled architecture. The baseband processing can be performed in real-time using three Montiums and a GPP [4].

III. Digital Radio Mondial

DRM is the upcoming successor of AM radio and provides a flexible and efficient audio and data broadcasting standard. The intention of the DRM standard is to combine FM-like sound-quality on the AM frequency bands with a large national or international coverage area by a small number of transmitting sites. DRM is seen as a complementary system to Digital Audio Broadcasting (DAB) [5] and Digital Video Broadcasting Terrestrial (DVB-T) [6].

Compared to analogue AM the main advantages of DRM are: a) robustness in fading channels, b) better audio quality because of source coding, c) power savings at the transmitting side, d) higher capacity for service related data, and e) availability of data services [7].

A. Channel Assignment

In the current analogue broadcast systems, every radio channel contains one audio service and maybe some service data via Radio Data System (RDS). The DRM channels conveys a so-called DRM multiplex which comprises three channels, which are grouped in a DRM super frame (see Fig. 2 [1]).

The first channel, the Fast Access Channel (FAC) provides information about the physical layer to enable a receiver to decode the two other channels. The second channel, the Service Description Channel (SDC) contains detailed information about the multiplex configuration, the extra service information and some additional DRM features. The third channel, the Main Service Channel (MSC) conveys the actual service content that can contain up to four streams containing audio or data.

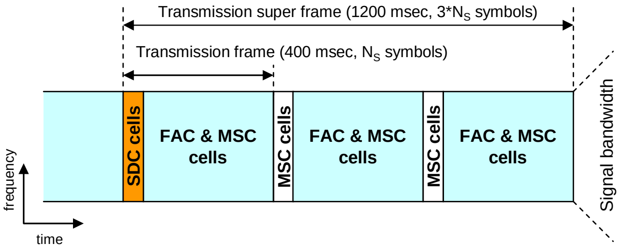

Fig. 2. DRM transmission frame format

The transmitter can choose between different configurations for the SDC and MSC channel. These different configurations are necessary to deal with the different conditions of the radio transmission channel and error protection requirements of the input. Because of this dynamic changing transmission configuration, a flexible receiver system is necessary.

B. System Architecture

Fig. 3 [1] describes the general encoding (transmitter) side of the DRM system. Different audio encoders can be used to encode the audio input stream, depending of the transmission capacity and content (audio/speech). These audio encoders, Advanced Audio Coding (AAC) extended by Spectral Band Replication (SBR), Code Excited Linear Prediction (CELP) and Harmonic Vector eXcitation Coding (HVXC), are part of the MPEG-4 audio standard [8].

After the pre-encoding the data stream and source encoding the audio stream, the bits are encoded by the Multilevel Coding (MLC) scheme using energy dispersal, convolutional encoding and bit interleaving. The parameters for the MLC encoder depend on the desired error protection levels of the information. The encoded bits are mapped with a 4-QAM, 16-QAM or 64-QAM modulation scheme. The MSC cells are cell interleaved to prevent burst errors at the receiver side.

The encoded and modulated information is combined with reference pilots cells to create the OFDM symbols. The pilot cells are needed for synchronization and channel estimation. After the inverse FFT a guard time is added to prevent inter symbol interference and perform time synchronization at the receiver. After the modulator, the OFDM symbol is ready to be transmitted on the desired carrier frequency (f_c).

Because of the different and varying channel propagation conditions over the different frequencies below 30 MHz, four different OFDM modes are supported (see Table I). These modes vary from a high

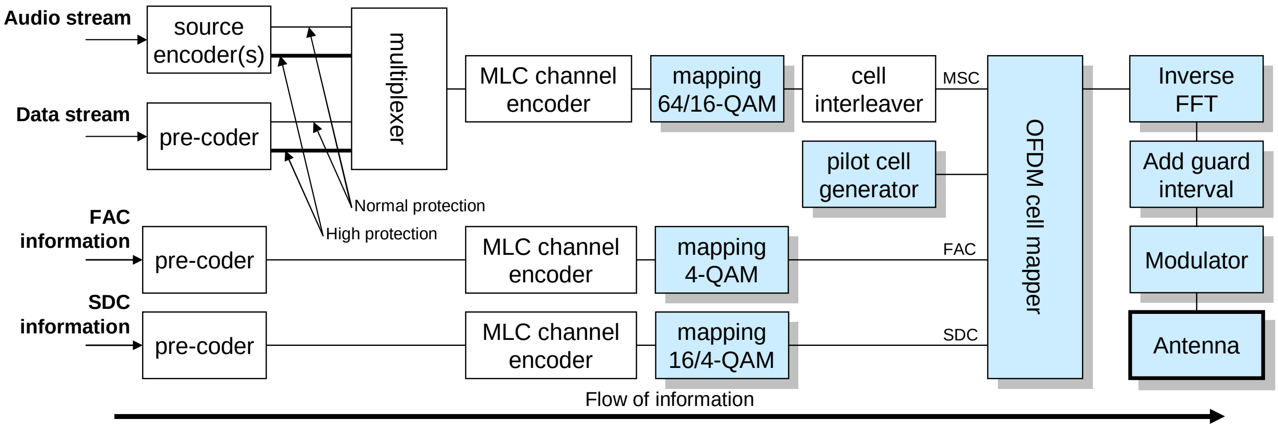

Fig. 3. The dataflow in a DRM transmitter

Parameter		Mode			
		A	B	C	D
Symbol time (T_U) [ms]		24	21 1/3	14 2/3	9 1/3
Guard time (T_G) [ms]		2 2/3	5 1/3	5 1/3	7 1/3
FFT Size (N_U)		288	256	176	112
# Symbols/frame (N_s)		15	15	20	24
Datarate [kbps]	max	72.0	56.1	45.5	30.6
	min	6.3	4.8	9.2	6.1

TABLE I
THE DIFFERENT OFDM MODES IN DRM

capacity but low robustness (mode A) to low capacity but high robustness (mode D). The data rate depends on the coding scheme, modulation scheme and spectrum occupancy.

C. *Receiver*

Fig. 4 depicts a DRM receiver. The receiver will be used in new multi-band radio receivers, car-audio and handheld devices. These receiver implementations have to be efficient, because of the limited energy budget of these devices.

Between the Radio Frequency (RF) reception and the OFDM demodulation, the signal is converted from the analogue to the digital domain. Depending on the frequency position of the desired channel (RF, Intermediate frequency (IF) or baseband) the signal is sampled with a different sample frequency (f_s). In case of RF and IF a Digital Down Converter (DDC) is necessary to move the signal to baseband and to reduce the number of samples for the baseband processing. Compared to the baseband case, RF and IF require more digital processing, but it gives a more flexible receiver due to an easier adjustment of the digital filters.

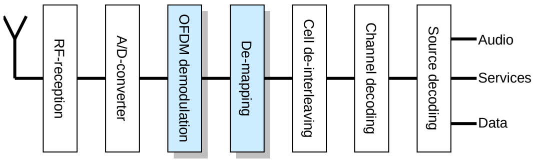

Fig. 4. The DRM receiver

The DDC is not used in our implementation, but this is a very computational intensive part of the processing, because of the necessary (FIR)-filtering before the decimation. For a four times oversampled system this can already be at least the same amount of processing as the FFT block. In [9] they have chosen to place this block in a reconfigurable hardwired module based on profiling their existing software implementations.

In our implementation we assume a near baseband position (center frequency at 12 kHz), because we have to sample the signal with the soundcard of a PC (f_s = 48 kHz). This requires only a digital mixer to shift the DRM-band from near baseband to baseband (see block A in Fig. 5).

In the next section we will specify the OFDM blocks in more detail, because this is in our opinion the most computational intensive part of the DRM receiver.

IV. IMPLEMENTATION AND SIMULATION

As a first start we partitioned a DRM system (transmitter, channel and receiver) in conformance with the DRM specification [1] in three parts:

1) OFDM modulation and demodulation, which is often referred to the baseband processing.
2) Channel encoding and decoding, which contains the interleavers and forward error correction.
3) Source encoding and decoding, which is the MPEG-4 audio standard for the audio stream.

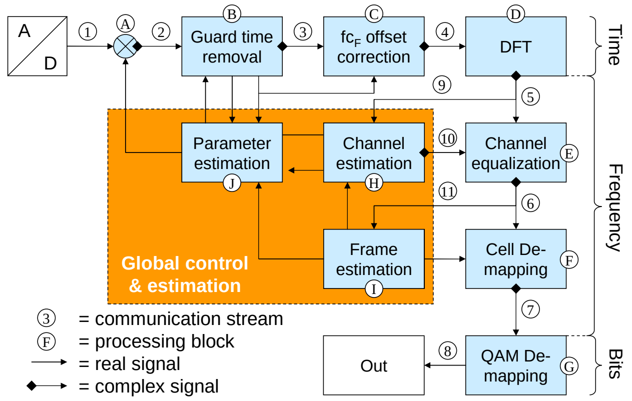

Fig. 5. The DRM receiver (baseband processing)

The three parts can be seen in Fig. 3 for the transmitter side and in Fig. 4 for the receiver side.

We implemented a detailed partitioned OFDM part (see Fig. 5 and indicated by the non-white blocks in Fig. 3 and 4) and the transmission channel. This implementation allows to transfer a specific bit-stream over different standardized transmission channels [1]. The Matlab implementation can be used to analyze and visualize the effects of different algorithms for the individual baseband processes.

A. *Baseband Processing*

Fig. 5 depicts a schematic picture of a part of a DRM receiver, which covers the OFDM demodulation and de-mapping of Fig. 4. The different blocks are partitioned based on their functionality. Starting from the A/D-converter we assume an input signal at a near baseband position. Because of the already low sample rate of the A/D-converter a DDC to reduce the number of samples is not necessary, but only a mixer (*block A*) to shift the f_c of the received DRM spectrum back to zero. If the input sampling rate is much higher, which is necessary for RF and IF front-ends, the mixer has to be replaced by a DDC.

With a DRM signal at the baseband position the time synchronization (*block B*) is used to find the start of a new OFDM symbol. Finding the start of a new symbol is performed by correlation (see Eq. (1)) of the normalized input $x[n]$ with a time delayed ($N_U = T_U \cdot f_s$) version of that input over a window equal to the guard time ($N_G = T_G \cdot f_s$). The correlation is maximal at the start of a new symbol (estimated by $\hat{n}_\epsilon$).

$$\hat{n}_\epsilon = \arg\max_{n_{tr}} \left| \sum_{i=n_{tr}}^{n_{tr}+N_G-1} \frac{x^*[i]}{|x[i]|} \cdot \frac{x[i+N_U]}{|x[i+N_U]|} \right| \qquad (1)$$

The index n_{tr} is the trial position for the correlation window. Because OFDM relies heavily on the orthogonality, *block C* corrects the minor frequency offsets caused by the analogue and digital mixers. The value of this offset can be estimated at the start of a new symbol. The angle instead of the absolute value in Eq. (1) at $n_{tr} = \hat{n}_\epsilon$ is linear related to this minor frequency offset [7].

Next, an 4xN_U-point FFT (because of 4x oversampling) is performed to transform the time domain samples back to the individual cells in an OFDM symbol. As listed in Table I, the FFT size is not always a power of two. Therefore, the FFT-block will require extra attention during the implementation for mode A,C and D, because it needs the Prime Factor Algorithm, which is less regular compared to the radix-2 FFT algorithm.

Before continuing processing the OFDM cells, *block H* estimates the channel transfer function using the known transmitted gain pilot pattern. The OFDM-cells are then corrected by a multiplication with the inverse of this channel transfer function. After the channel equalization the start of the DRM frame can be found (*block I*) using the time, gain and frequency pilot pairs as described by the DREAM software [3]. Using this information *block F* separates the cells into the three information channels and *block G* transform the complex values to bits.

B. *Computational load*

Based on the algorithms used in our implementation we determined the number of multiplications and additions of every process (see Tables II and III). This gives an indication of the required computational requirements for the hardware tiles. Furthermore, every block generates an amount of samples/sec (see Table IV), which might have to be transported over the Network on Chip. This gives an indication of the necessary bandwidth requirement of the Network on Chip. We only indicated the large communication streams of Fig. 5. The rest is less then 1kbit/s.

For both tables we assumed a critically sampled system (f_s = 24 kHz) without a DDC and a spectrum occupancy of 10 kHz. The DDC is not used, although decimation with a factor 2 is possible after the mixer. For a complex multiplication we took 4 real multiplications and 2 additions. For the data types we took 16 bit fixed point for a real sample (only stream 1 in Fig. 5) and 32 bit for complex samples. For channel modulation we assumed 64-QAM, which results in an upper-bound for edge 8 in Fig. 5. For all four possi-

Baseband process	#	Mode			
		A	B	C	D
Mixer	A	72k			
Time synchr.	B	144k			
Frequency corr.	C	108k	96k	88k	67k
FFT	D	396k	346k	298k	210k
Channel eq.	E	43k	38k	35k	27k
Channel est.	H	17k	16k	14k	11k
Other		< 10k	< 10k	< 10k	< 10k
Total		**784k**	**716k**	**656k**	**541k**

TABLE II

THE REQUIRED NUMBER OF REAL MULTIPLICATIONS / SEC

Baseband process	#	Mode			
		A	B	C	D
Mixer	A	24k			
Time synchr.	B	168k			
Frequency corr.	C	43k	38k	35k	27k
FFT	D	396k	346k	298k	210k
Channel eq.	E	22k	19k	18k	13k
Channel est.	H	34k	31k	28k	21k
Other		< 10k	< 10k	< 10k	< 10k
Total		**689k**	**528k**	**573k**	**468k**

TABLE III

THE REQUIRED NUMBER OF REAL ADDITIONS / SEC

ble modes the exact numbers are given in Table II, III and IV.

V. Conclusion

Partitioning a DRM receiver into smaller independent blocks is useful, because then you are able to map them on different hardware tiles. Compared to the partitioning of a HiperLAN/2 implementation [4] the baseband processing of DRM has many similarities. However the amount of processing per second is less intensive. The processing block with the most computations is the FFT.

For processing the DRM frames we estimate that the intensive processing blocks (A,B,C,D,E) can be implemented on 3 MONTIUM-tiles. The rest is better suited for a GPP. For processing the DRM-frames, the system clock has to run at frequencies less than 1 MHz. When the different hardware tiles are connected via a Network on Chip the maximum network load does not exceed 1 MB/s.

Edge	#	Mode			
		A	B	C	D
A/D Conv. → A	1	375k			
A → B	2	750k			
B → D	3/4	675k	600k	550k	420k
D → E	5	338k	300k	276k	210k
E → F	6	268k	242k	216k	162k
F → G	7	254k	201k	162k	108k
G → Out	8	60k	47k	39k	26k
D → H	9	13k	40k	54k	54k
H → E	10	268k	242k	216k	162k
G → J	11	13k	40k	54k	54k

TABLE IV

THE REQUIRED COMMUNICATION BETWEEN BLOCKS [BIT/S]

VI. Future work

Currently, we aim at implementing the OFDM-baseband processing of DRM onto several MONTIUM-tiles. With this implementation we can show the flexibility of these tiles, because of the different requirements for the various receiver modes in DRM. Furthermore, we will use the concurrent communication streams between the processes as a test-case for our Network on Chip.

Acknowledgement

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