Testable Design and Testing of High-Speed Superconductor Microelectronics

Hans G. Kerkhoff, Arun A. Joseph and Sander Heuvelmans
MESA+ Research Institute, CADTES, Testable Design & Testing of Microsystems Group
7500 AE Enschede, The Netherlands

Abstract

True software-defined radio cellular base stations require extremely fast data converters, which can currently not be implemented in semiconductor technology. Superconductor Niobium-based delta ADCs have shown to be able to perform this task. The problem of testing these devices is a severe task, as still very little is known about possible defects in this technology. This paper shows an approach for gaining information on these defects and it is illustrated how BIST can be a solution of detecting these defects in ADCs under extreme conditions.

1. Introduction

Software-Defined Radio [1] is an advanced concept to be used by wireless communication companies, where the complete transceiver operation in a cellular base station can be realized in software. This has the advantage that whenever the system has to be upgraded, there is no need for hardware replacement. Unfortunately, the required data converters for this approach cannot be implemented in the medium future in semiconductor technologies. As presented in e.g. reference [2], superconductor (4 K) delta ADCs in a Niobium-based (Nb) process [3] can fulfill this task. A cross-section of such a process is shown in Fig. 1.

Essential element is the Josephson junction, consisting of a $Nb/Al_2O_3/Nb$ tri-layer. A delta ADC in such a process requires around 2500 Josephson junctions. The testing of such devices is still in its infancy and restricted to functional approaches. We have started to investigate to which extent defect-oriented testing is feasible and advantageous [4]. For this purpose, detailed defect information on the processing is required and Inductive Fault Analysis (IFA) principles can be used subsequently. An investigation has been carried out to locate possible defects in the JeSEF Niobium process [5] and moreover test structures have been designed to obtain statistical defect data. As test structures for Josephson junctions have been designed in the past and data is available on this subject, our research has been focused on other possible defects.

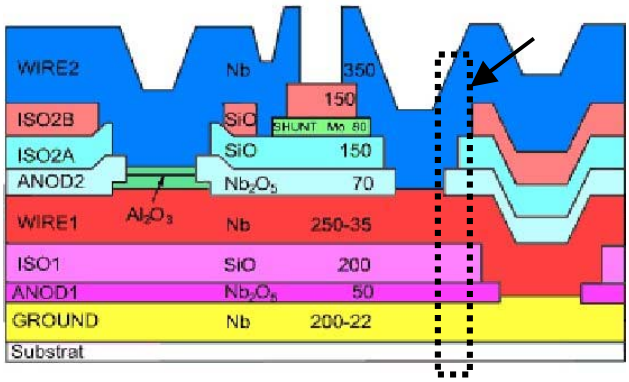


Figure 1: Cross-section of a Niobium (Nb) process [3]. The dashed box shows the area of interest in this paper.

As an example, cracks in WIRE 2 (Fig.1) over a WIRE2-WIRE1 via resulting from step-coverage problems have been investigated. Next, the influence of this effect has been investigated in an 8-bit delta ADC at Josephson-junction level, and subsequently it is shown that BIST is able to detect this defect.

2. Defects and test structures in a Niobium-based process

As Niobium-based processes are far less developed than silicon-based processes, very little is known in literature on defects in them. We have investigated [5], which defects can occur in the JeSEF Nb process [3] as shown in Fig. 1. At this moment, 27 possible defects have been theoretically established. The most important defect is a bridge in the tri-layer, effectively disabling the junction, by shorting metal layers. We will confine ourselves to the following seven defects as they occur in WIRE1 and WIRE2 (Fig.1).

Proceedings of the First IEEE International Workshop on Electronic Design, Test and Applications (DELTA'02)
0-7695-1453-7/02 $17.00 © 2002 IEEE

The defects are categorized into cracks and bridges. A crack is a (parametric) resistive open in layers. If its value is very large, it can be approximated by a classic open. Likewise, a bridge is a (parametric) resistive short between layers. Small values result in shorts between layers.

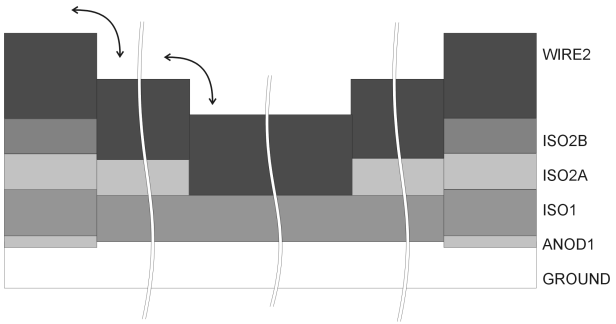


Figure 2: Detailed cross-section of (symmetrical) crack-sensitive structure (not on scale). Arrows indicate potential step-coverage problems.

Cracks can occur in WIRE2 above vias from WIRE2 to other metal layers. Similarly, a crack in WIRE1 is also possible over a via from WIRE1 to GROUND. These result from step-coverage problems. A crack in WIRE2 can also occur above a Josephson junction (tri-layer). In this paper, a crack in WIRE2 above the WIRE2-WIRE1 via is subject of research. The cause of this possible crack is a result of two subsequent steps (double arrow in Fig. 2). The developed associated test structure is slightly different from the structure of the via in Fig. 1. WIRE1 has been removed from the test structure in order to avoid a second conducting path.

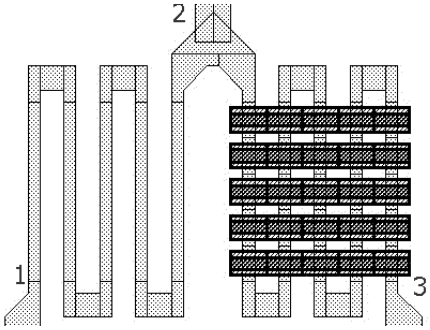


Figure 3: Test structure to detect cracks in WIRE2 due to step-coverage problems over a WIRE2-WIRE1 via.

Bridges between WIRE1 and WIRE2 also form a category of defects [5]. They can occur next to a junction in ANOD2, above a via between WIRE1 and GROUND, and next to a shunt (Fig. 1) or next to a junction in ANOD2 and ISO2A.

In order to obtain defect densities, to be used later on for IFA purposes, special test structures have been designed [6] in the JeSEF process. In Figure 3, a detail is shown of the test structure optimized for detecting cracks in WIRE2 due to step-coverage problems.

The light-gray tracks in Figure 3 are WIRE2 Nb material. Minimum feature size of this material is 5µm. The shown structure measures 180µm by 130µm. The dark areas crossing this material is basically the structure as shown in Figure 2. Hence, each WIRE2 crosses 4 steps per element. Consequently, the structure in Figure 3 incorporates 100 steps. The left section is the reference WIRE2 part, required for this so-called "v/d Pol" structure [7].

The method described in [7] consists of taking the ratio of the resistance of the "stepped" wire and that of the reference (non-stepped) wire. This ratio is used as a measure for the presence of defects near the steps. The measurement procedure forces voltages to wires and measures the current at *fixed* power dissipation. In this way, it eliminates possible inaccuracies due to variations because of self-heating in the wires, which occurs when resistances vary while voltage or current is fixed.

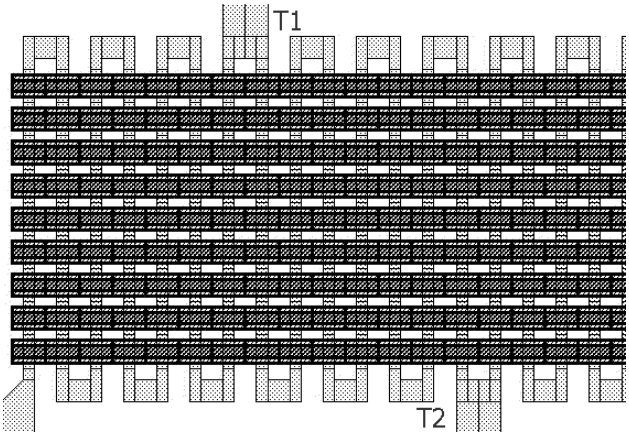


Figure 4: Part of the 2016-step test structure. Notice the intermediate taps (T1, T2 etc.)

In the test chip, 8 of these structures have been incorporated, as well as one 2016-step structure (Fig. 4) and accompanying reference structure (1920µm by 420µm). These numbers were derived from assuming to be able to manufacture a 16-bit delta ADC with acceptable yield [6]. In order to investigate the influence of orientation, orthogonal structures were included too.

For other (high-ranking) defects, dedicated test structures have been designed, as well as associated test procedures. Measurement results and statistics will be available in a following paper.

3. BIST Defect Detection in a Delta ADC

The defect described in detail in the previous section is considered one of the highest-ranking defects in terms of occurrence. This data can be subsequently used in combination with the layout of a logic Josephson-junction block, like the confluence buffer shown in Fig. 5 [8]. The box in Fig. 5 shows a possible location of a crack in WIRE2, above a WIRE2-WIRE1 via.

The confluence buffer, together with the pulse splitter, are the basic building blocks of the *flux amplifier* in the superconductive delta ADC for software radio as shown in Fig. 6 [2, 10]. Essentially, the confluence buffer accepts two pulses at its two inputs, and merges them after each other in the single output with a short delay in between.

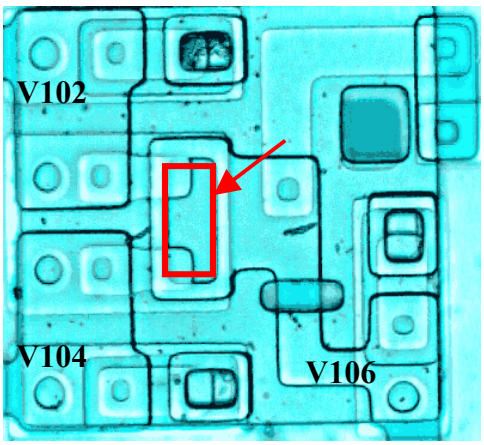


Figure 5: A confluence buffer [8], part of a flux amplifier, and a possible location in the layout of a crack in WIRE2 (box). (Courtesy SUNY)

The information regarding the crack is used to insert a resistor (0.6 Ω) in the proper interconnection line in the Josephson-junction netlist. Next, fault simulations in JSIM (a Josephson-junction based Spice derivative) have been carried out, using a similar approach as published in reference [4], in order to investigate the influence of this defect on the circuit behavior. The fault-free and faulty circuit results are shown in Figures 7a and 7b respectively. Figure 7a shows the V102 and V104 input SFQ pulses (converted flux quanta into voltages) applied to the confluence buffer. These pulses have duration of around 20 ps. In the fault-free case, after a short delay, the two merged SFQ pulses appear (V106). As Fig. 7b illustrates, the confluence buffer is very sensitive to cracks. A resistance equal or in small excess of 0.6Ω will cause immediately a total failure of the confluence buffer, and no merged pulses appear at the output. The reason for this is that the circuit operates in the superconducting state, and hence involved resistances are almost zero.

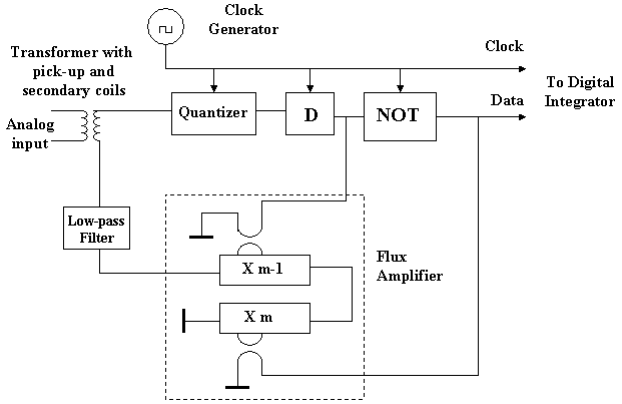
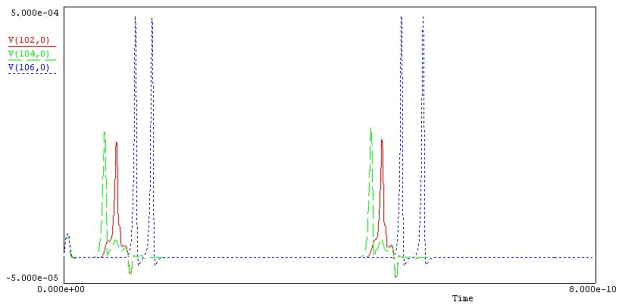
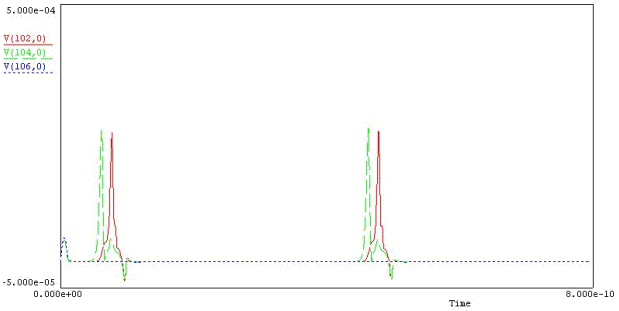


Figure 6: Diagram of a superconductor delta ADC, including the flux amplifier, which partly consists of confluence buffers [2].



a)



b)

Figure 7: Crack in WIRE2 in the confluence buffer. a) Fault-free circuit simulation (R<0.6 Ω) b) Faulty circuit simulation (R=0.6 Ω).

It is obvious that this fault will cause a total failure of the flux amplifier. Following the previous approach,

many defects and their resulting behavior on a particular layout can be investigated.

The next step that was tackled was to investigate the relations between faults as shown in Fig. 7b and key (specification) parameters of our ADC, like INL and DNL. As a first step, a high-level language (VHDL) was used to model the data converter (Fig. 6). Digital-step approximation was used to describe the analog parts, as the combination Verilog and Verilog-A caused problems. In the future, a combined VHDL/VHDL-AMS mixed-level simulator will be used for this purpose.

Behavioral descriptions of the delta ADC architecture have been derived. For the flux amplifier part, the results of the above fault simulation using JSIM were incorporated in the VHDL model. In case of a WIRE2 crack in the confluence buffer, the feedback mechanism will change some static parameters; it can even result in instability.

The linear histogram BIST approach to detect defects [9] in an 8-bit delta ADC (Fig. 6) has been used in our Modelsim VHDL simulations on an HP-Unix workstation.

All required digital electronics for BIST, like registers, counters etc. can all be designed [10] in the previously described Niobium technology [3] and do not affect the original operation of the converter.

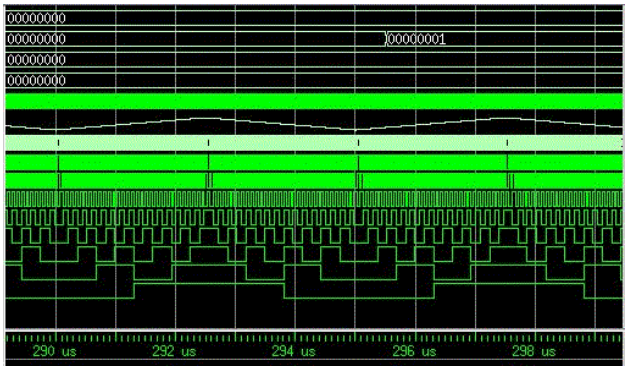


Figure 8: VHDL simulated behaviour of a fault-free super-conducting 8-bit delta ADC including BIST.

In Figure 8, the fault-free simulation is shown of an 8-bit delta ADC *including* the digital histogram BIST hardware, discussed in more detail in [9, 10]. The BIST approach requires a triangular input signal in this case. The top four signals are respectively the offset, gain, DNL and INL. Their output code is showing at the beginning time marker. Next, the clock signal and a triangular-shaped input signal for the converter are seen. The bottom 8 signals are the digital outputs of the converter, the most significant bit being at the bottom. As can be seen in Fig. 8, the digital outputs behave as one would expect when a triangular input is applied.

Figure 9 shows the VHDL simulation after introduction of the resistance in the netlist caused by a crack in WIRE2 (Fig. 6b). The data of the JSIM (fault) simulation at junction level was imported in the VHDL code of the fault-free VHDL simulation (mixed-level simulation). The signal sequence in Figure 9 is the same as in Figure 8. Notice the second vertical time marker in Figure 9, and the different time scales. It shows the digital output codes of offset, gain, DNL and INL 895µs after starting the input signal.

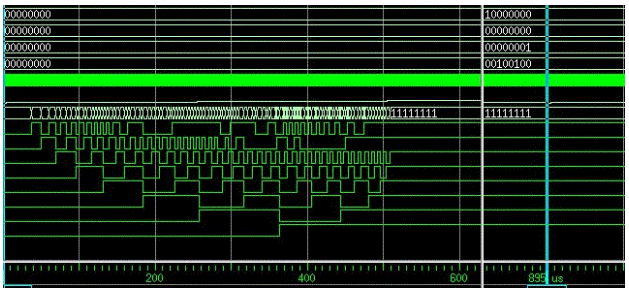


Figure 9: Faulty (WIRE2 crack in confluence buffer) VHDL simulated behaviour of a super-conducting 8-bit ADC including BIST.

As can be seen from Figure 9, after around 500µs, all output bits become one. Hence, the crack in WIRE2 has a major impact on the ADC. This is also reflected in the values for offset, gain, DNL and INL. This data code is seen between the two vertical lines. The figures in 8 and 9 indicate the correct operation and detection of the defect by the BIST structure.

4. Conclusions

In this paper, a number of defects, which can occur in a Niobium-based process that is used for superconductor microelectronics, have been introduced. For one case, a crack in WIRE2 as result of step-coverage problems above a WIRE1 and WIRE2 via, the required test structures for detecting this type of defect and obtaining statistics has been presented.

A mixed-level fault simulation has been carried out based on this defect, for the first time combining JSIM circuit simulations with VHDL descriptions of an 8-bit delta ADC *including* histogram BIST.

The correct operation of this structure is shown, as well as the detection of a crack in WIRE2 of this system

by BIST, thereby linking this defect to data converter parameters like offset, gain, DNL and INL.

References

[1] E.B. Wikborg, V.K. Semenov and K.K. Likharev, "RFSQ Front-End for a Software Radio Receiver", *IEEE Trans. Appl. Supercon*, Vol. 9, June 1999, pp. 3615-3618.

[2] V.K. Semenov, Y.A. Polyakov and T.T. Filippov, "Superconducting ADC with On-Chip Decimation Filter", *IEEE Trans. Appl. Supercon*, Vol. 9, June 1999, pp. 3026-3029.

[3] RFSQ (JeSEF) Design Rules, Nb/Al_2O_3/Nb process, 2000. http://www.cryo-jena.de

[4] H.G. Kerkhoff and H. Speek, "Defect-oriented Testing of Josephson Logic Circuits and Systems", *Physica*, C 350, Elsevier Science, 2001, 261-268.

[5] P. Hendrikse, "Fault Detection in a Complex RFSQ LTS Circuit", *Report # 060-2918*, University of Twente, Enschede, The Netherlands, September 2001.

[6] S. Heuvelmans, "RFSQ Defect Test Structures", *Report # 060-2919*, University of Twente, Enschede, The Netherlands, October 2001.

[7] J.A. van der Pol, " Short Loop Monitoring of Metal Step Coverage by Simple Electrical Measurements", in *Proc. IEEE IRPS*, 2001, pp. 148-155.

[8] The SUNY RFSQ Cell Library Web Designers Manual, http:// gamayun.physics.sunysb.edu/RSFQ/Lib/

[9] S. Bernard et al., "Linear Histogram Test of ADCs – A BIST Implementation", in *Proc. IEEE IMSTW*, Montpellier, France, June 2000, pp. 40-45.

[10] A.A. Joseph, M.H.H. Weusthof and H.G. Kerkhoff, "DfT for a Superconducting Delta ADC for Software-Defined Radio Applications", in *Proc. IEEE IMSTW*, Atlanta, USA, 2001, pp. 47-54.