Degradation of α-Si:H TFTs caused by Electrostatic Discharge

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Abstract— This paper gives results of experimental analysis of impact of electrostatic discharge (ESD) pulse on amorphous silicon thin film transistors (α-Si:H TFT). The development of degradation of the electron mobility and the threshold voltage is presented. Failure analysis has been done and two failure mechanisms have been identified.

I. INTRODUCTION

Hydrogenated-amorphous-silicon thin-film transistors (α-Si:H TFT) were first reported in 1979 [1]. Nowadays, they are widely used in active matrix addressing in liquid crystal display (AM-LCD) or printer heads. Their basic I-V characteristics can be analyzed in the same way as those of crystalline MOS transistors. Comparing them with standard MOS transistors, they have low electron mobility μ (typically 0.3-0.6 cm^2/Vs) and instable threshold voltage (V_T) [2]. A cross section of a TFT used in AM-LCDs is shown in Fig. 1. Note the presence of a lightshield. As α-Si:H is light sensitive, devices are shielded by a metal layer.

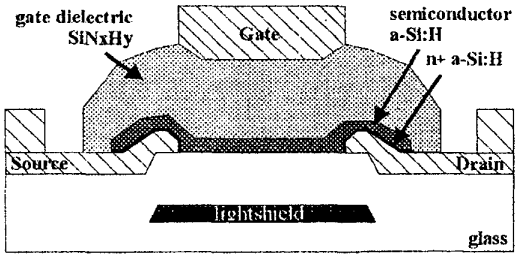

Fig. 1. Cross-section of α-Si:H TFT with a staggered structure.

The subject of this paper is the reliability of active matrix display devices operating with amorphous-silicon thin-film transistors (α-Si:H TFT), when exposed to Electrostatic discharge (ESD). Due to the presence of glass insulating layer, ESD is a very important topic in display manufacturing. To date, a very few papers that treat ESD in TFTs, have been reported, showing some experimental machine model results [3], or display panel (including gate and source bus-lines) defects [4,5].

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II. EXPERIMENTS

The devices used in this work were specially designed for testing, with variations of design parameters (length (L) and width (W) of the channel) (Fig. 1). To test ESD hardness of the TFTs a high voltage pulse (zap) is applied to drain by means of Transmission line model (TLM) [6], of which the electrical circuit is shown in Fig. 2. Charged transmission line produces constant brief (t=2L/v, where v is propagation velocity of wave) voltage pulse of height $V_{in}/2$ (i.e. for transmission line length of 10 m, the pulse length is 100 ns). In c-Si MOS transistors this voltage pulse is transformed into a current pulse. In TFT's however, due to low conductivity of α-Si:H, voltage pulse is applied.

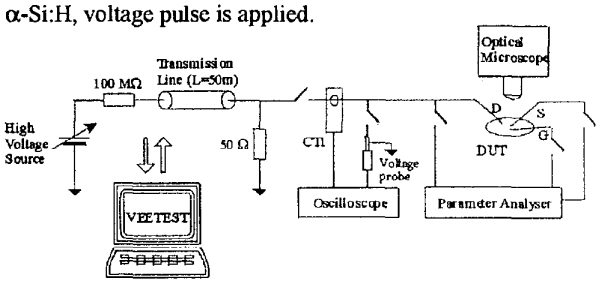

Fig. 2. Set-up of modified Transmission Line Model combining high voltage pulse source and measuring of DC characteristics.

TLM pulses were applied on TFT drain, while gate and source were grounded. In order to follow degradation development, the TLM voltage stress is increased in steps and in between these steps a full set of different DC characteristics is measured by means of Semiconductor Parameter Analyser HP4145. The modified TLM system (Fig. 2.) allows for automatic measurements of DC characteristics in between two TLM voltage pulses. In our analysis, these pause between TLM pulses have been as long as it is needed to do the measurements. TLM voltage was increased up to breakdown. Breakdown criteria was defined by an enormous increasing of TLM current (as it happens at t=317ns in Fig. 3) measured by the digital oscilloscope DSO HP54710A.

In this work three different currents have been monitored between TLM pulses:

1. Transfer characteristics $I_D(V_G)$.
2. Output characteristics $I_D(V_D)$.
3. Sub-threshold current.

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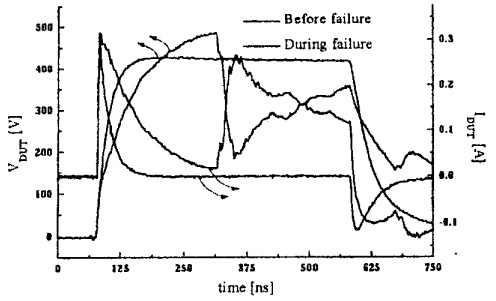

Fig. 3. Shape of current and voltage TLM pulses monitored on the oscilloscope (before and during failing).

III. ANALYSIS OF DEGRADATION

The transfer characteristics ($I_D(V_G)$) have been monitored in linear operational regime (V_D=0.1V). Under the low TLM voltage (50, 100, 150V), there is no change. For the values higher than 200V, it was seen that this characteristic changes. It shifts to the negative side. The slope of the characteristics increases.

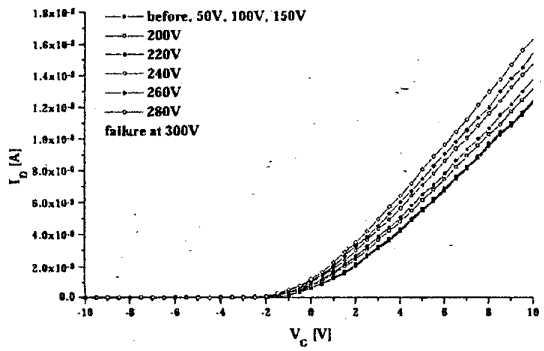

Fig. 4. Transfer characteristics during TLM.

In Fig. 4 a set of monitored $I_D(V_G)$ curves is shown. Drain current increases on applied gate voltage (exponentially for low voltage and linearly for voltage above V_T) is described by (1):

$$I_D = \frac{W}{L}\mu_n C_i\left[\left(V_g - V_t\right)V_d - \frac{V_d^2}{2}\right] \quad (1)$$

For the higher gate voltages it becomes:

$$I_D = \frac{W}{L}\mu_n C_i\left(V_g - V_t\right)V_d \quad (2)$$

Two mechanisms have been found to contribute to degradation effects in α-Si:H TFTs: trapping of charge in the gate dielectric and change in the density of states (DOS) of the α-Si:H itself.

The electron mobility μ_n is thermally activated with an energy given by the width of the tail states, not by E_C-E_F [7]:

$$\mu_n = \mu_0 N_c \frac{kT}{n} e^{-\frac{E_a}{kT}} \quad (3)$$

where μ_0 is the extended state electron mobility, N_C is the density of states at the mobility edge, n is the total electron density, and E_a is the activation energy which reflects the tail state distribution of the α-Si:H.

The μ_n was derived from the slope of the curve in linear part (2). How the electron mobility is changing during TLM is shown in Fig. 5. It is also shown that calculated values can be fitted by exponential function given in Fig. 5. Unexpectedly, the electron mobility increases after applying TLM pulses.

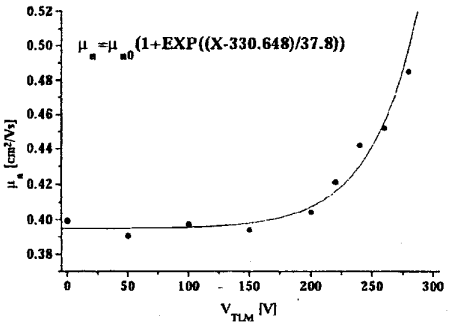

Fig. 5. Electron mobility behavior under TLM.

Next, the threshold voltage is derived from the transfer characteristics. Calculated values showed that there is a decreasing of the threshold voltage value during TLM stressing. V_T is given by $V_T = \frac{-qtn_0}{C_i}$ where C_i is the gate capacitance per unit area ($=\varepsilon_i/d$), t is the α-Si:H thickness and n_0 is the initial charge density in the α-Si:H.

Threshold voltage shift can be induced by charge trapping in the gate dielectric [8]. During TLM, the positive voltage pulse is applied on drain. It can induce two possible processes: (1) holes trapping in the gate dielectrics or (2) de-trapping of a negative charge (Fig. 6). Process of holes trapping would consequently have the electron mobility decreasing (scattering increased). Process of electrons de-trapping would increase the electron mobility (higher electron concentration), and therefore can be accepted. After every TLM pulse applied, the amount of stored negative charge at the gate dielectric/amorphous silicon interface is bigger. The question is how these de-trapped electrons will influence the concentration of electrons in the channel. The possible explanation can be that de-trapped electrons are mobile and that they can take a part in current conducting. It also explains that after applying TLM pulses the V_T is lower.

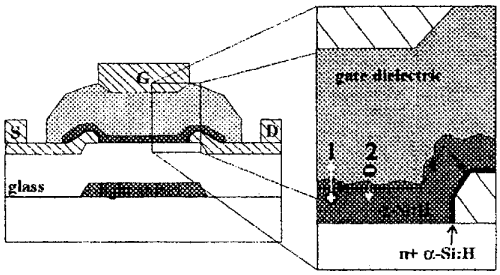

Fig. 6. Charge induced by TLM at the interface.

In Fig. 7 is shown how the threshold voltage is changing during TLM. It is also shown that it can be fitted by an exponential function.

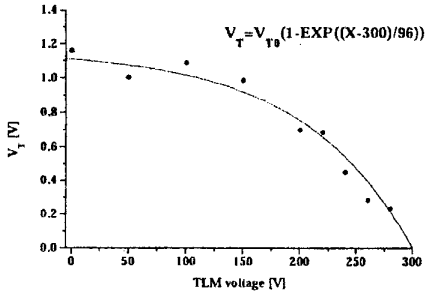

Fig. 7. Threshold voltage shift during TLM.

In the next analysis, the output characteristics $I_D(V_D)$ was measured between TLM pulses. The saturation current is given by:

$$I_D = \frac{1}{2}\mu_n C_i \frac{W}{L}(V_G - V_t)^2 \qquad (4)$$

Knowing from the previous analysis that μ_n increases and V_T decreases during TLM, it is predicted that saturation drain current will increase, which is indeed proven by measurements presented in Fig. 8.

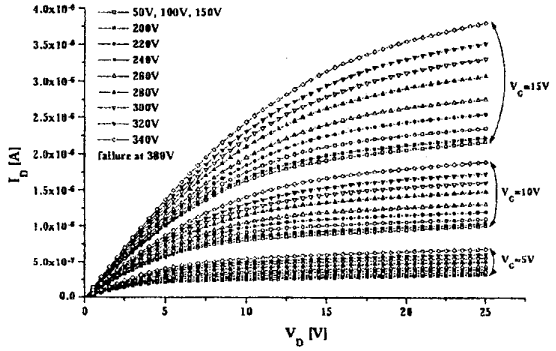

Fig. 8. Output characteristics monitored during TLM.

In the next analysis the sub-threshold current I_{DSUB}, which is very sensitive on V_T change, was measured between TLM pulses. The sub-threshold current has been measured at V_G=V_S=0V. The sub-threshold current can be used to measure the density of states in the upper band-gap region of α-Si:H [8].

All set of measured I_{DSUB} is given in Fig. 9. It is found a very fast increasing of sub-threshold current after every applied TLM pulse higher than 200V. For the clarity, these results are also represented in more conventional way (Fig. 10). It is also shown that it is possible to fit this behaviour with exponential fitting curve.

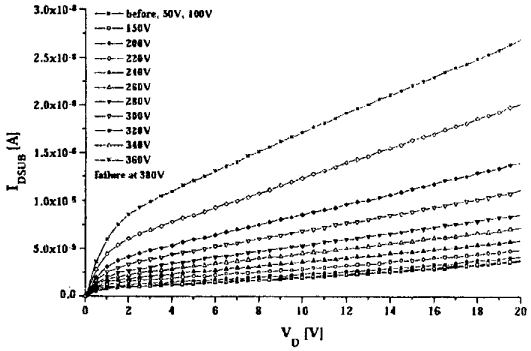

Fig. 9. Sub-threshold current monitored between TLM pulses.

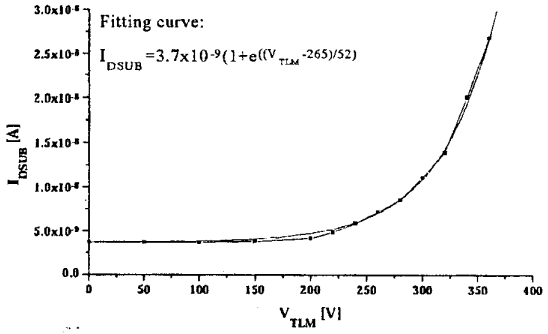

Fig. 10. Conventional representation of the sub-threshold current during TLM with fitting curve.

IV. FAILURE ANALYSIS

It was found that breakdown voltage (V_{BR}) depends on design parameters (L, W). For a given width of the TFT, V_{BR} increases with channel length. Comparison of V_{BR} between TFTs with L=100μm and L=4 μm is given in Fig. 11.

On the other hand, for that values of the breakdown voltage, electrical field (given as $E=V_D/t_{ox}$) across the gate dielectric has value ~ 10 MV/cm, which is enough to cause dielectric breakdown.

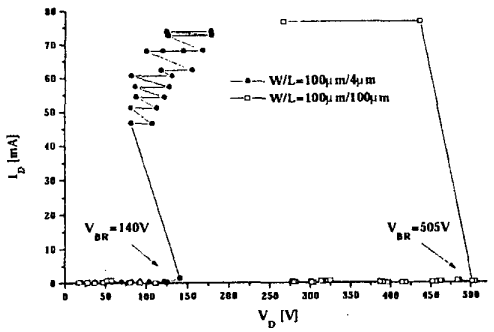

Fig. 11. TLM characteristics of two tested TFTs.

Further, failed devices were de-processed and inspected by means of scanning electron microscopy (SEM). Detailed analysis showed that there are two failure modes:

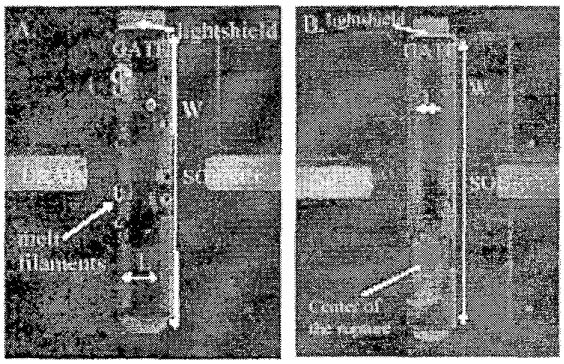

Fig. 12. SEM photos showing different modes of failure.

- breakdown via lightshield. A number of melt filaments was found at both drain/gate and source/gate edges (Fig. 12a). This failure mode was identified in two out of twenty devices inspected.
- gate dielectric breakdown. It was manifested like proportionally big rupture of gate dielectric. This is the often-found failure mode. Center of the rupture was found at the edge of drain under the gate electrode (Fig 12b).

The fact that two failure modes are responsible for the catastrophic failure was interesting for deeper analysis. In that order, electrical simulations of α-Si:H TFT were performed, using Silvaco simulation software. If we look at the simulation of electrical field under given stress conditions (Fig. 13), we can see that peak of electrical field is localized at the drain/gate edge. It explains why the center of the rupture is localized at the gate/drain overlapping area. Due to the fact that thickness of the glass substrate layer between α-Si:H layer and lightshield is similar size as the thickness of the gate insulator layer, the second smaller peak of electrical field appears close to the edges of the lightshield. In some cases it can lead to creation of melt filaments.

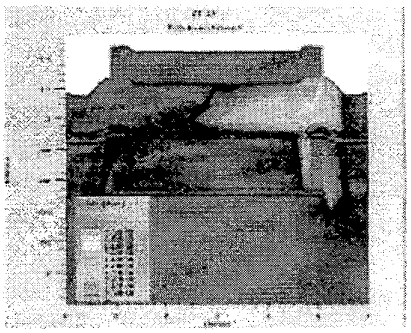

Fig. 13. Simulation of the static electrical field under stress on drain (gate and source are grounded).

V. CONCLUSION

In this paper, behavior of TFTs under TLM stress was investigated. First results are obtained. For stress voltage exceeding 200V, it was shown that in a stepped stress, each stress level increases the degradation until catastrophic failure occurs. Degradation can be described by an exponential function. Very fast decreasing and increasing of mobility happens in parallel. There are two catastrophic failure modes. The current path is created in the first case from drain via lightshield to source, and in the second case from drain through gate dielectric to gate. The breakdown voltage value varies with the channel length.

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