OPTIMIZATION OF NITRIDATION CONDITIONS FOR HIGH QUALITY INTER-POLYSILICON DIELECTRIC LAYERS

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Abstract
Nitridation of deposited high temperature oxides (HTO) was studied to form high quality inter-polysilicon dielectric layers for embedded non volatile memories. Good quality dielectric layers were obtained earlier by using an optimized deposition of polysilicon and by performing a post-dielectric anneal in a rapid thermal processor. In the present paper the quality is further improved by means of optimization of the post-dielectric anneal. The influence of temperature, time and pressure during annealing on the electrical properties is investigated. Electrical characterization by means of charge-to-breakdown (Q_{bd}) and I-V measurements on simple capacitor structures evaluates the electrical properties of the layers. It is shown that an (optimized) rapid thermal N_2O anneal leads to a very high charge to breakdown ($Q_{bd} \approx 25$ C/cm^2), low charge trapping and low leakage currents.

I. Introduction

The main purpose of this research is to develop a *deposited* dielectric layer which can be used as an inter-polysilicon dielectric in non volatile memories, in particular the VIPMOS EEPROM [1]. By optimizing the texture and morphology of polysilicon layers [2] and by using *deposited* instead of thermally grown dielectrics, a more reliable inter-polysilicon dielectric can be obtained since defects present in the silicon are not incorporated in the deposited layer and the surface of the polysilicon layer is not roughened (no silicon consumption). Since as-deposited oxides are not as dense as thermally grown oxides, after treatments like rapid thermal N_2O annealing are necessary to obtain the desired electrical characteristics [3]. In [3] and [4] it is shown that N_2O annealing leads to large improvements of oxide layers, which is thought to derive from its incorporation of nitrogen at the oxide-silicon interface.

Our application, the VIPMOS EEPROM cell, is well applicable as analog or multi-level storage device. The write process is based on bulk hot electron injection [1],

while erasing is performed by inter-poly tunneling. Conflicting demands exist for the inter-poly dielectric, i.e. good data retention (low leakage currents) for low and moderate applied control voltages and good tunneling characteristics with very low charge trapping, in particular when analog applications are concerned, for high applied voltages (good endurance). So a *combination* of a high Q_{bd} and low ΔV (low charge trapping) is required. For the investigation simple capacitor structures were realized, in which the temperature, time and pressure during annealing were varied.

II. Experimental

After a standard HNO_3 cleaning p-type wafers were thermally oxidized in dry O_2 at 1100°C to a thickness of 100 nm. Then a 300 nm silicon film (poly 1) with a very flat surface [2] was deposited by means of LPCVD at 550°C and a pressure of 1 mbar. This layer was doped by means of ion implantation (Phosphorus, $8x10^{15}$ cm^{-2}, 50 keV). The wafers were annealed for 30 minutes at 800°C in N_2 ambient to activate the dopant. Then a 25 nm thick dielectric layer was deposited, which consisted of HTO from SiH_2Cl_2 and N_2O at 800°C. This layer simultaneously serves as gate and inter-poly dielectric. It was additionally annealed in a rapid thermal processor in N_2O ambient at different temperatures ($800 < T < 1000$°C), times ($5 < t < 35$ min) and pressures ($17 < P < 25$ Torr). For comparison also dielectric layers without annealing were processed (further referred to as control oxide). Then a second silicon layer (poly 2) of 300 nm was deposited by means of LPCVD at 625°C. This film was doped by means of ion implantation (Arsenic, $6x10^{15}$ cm^{-2}, 100 keV). After defining poly 2 all samples received a 200 nm thick CVD oxide as a passivation layer. Contact holes were opened and Al was deposited and patterned to contact the capacitor structures. Finally, all devices were sintered at 400°C for 30 minutes in wet N_2 ambient.

III. Results and Discussion

Due to the rapid thermal N_2O annealing, the dielectric thickness of the inter-poly dielectrics increased by about 5-10% (depending on the anneal variant, measured by ellipsometry). In fig 1 four Weibull distributions are shown of Q_{bd} for layers annealed at 850, 925 and 1000°C for 20 minutes at a pressure of 25 Torr and one control oxide without anneal. The capacitor area was $1*10^{-4}$ cm^2 and the stress was 2.5 mA/cm^2 constant current injection for positive bias, i.e. electrons are injected from the bottom electrode while the voltage is monitored on the upper electrode. From the Weibull plots it is obvious that the annealing step is necessary to obtain high Q_{bd}-values. However, only slight differences are observed as a function of anneal temperature. The amount of trapped charge does differ: annealing at 925°C yields the lowest charge trap density (measured as ΔV) per Q_{bd}, see fig 2. $\Delta V/Q_{bd}$ is an important parameter when multi-level storage or analog applications are

considered, since the threshold voltage window (defined as $V_{T,\ prog.\text{-}state}$-$V_{T,\ erased\text{-}state}$) needs to remain constant as long as possible during repeatedly programming and erasing. A very high Q_{bd} (15 C/cm^2) and a very low ΔV (<1V) are obtained. In fig 3 the corresponding I-V curves are shown. The layer annealed at 850°C starts conducting at the highest voltage, but has a lower breakdown field (E_{bd}). However, all layers fulfil the requirements. The best combination of properties is obtained with the layer annealed at 925°C. Therefore this anneal temperature is used for further optimization of the dielectric layer.

The second process variable was the anneal time at a constant temperature of 925°C and pressure of 25 Torr. The Weibull distribution of all layers is shown in fig 4. The best combination of Q_{bd} and ΔV, shown in fig 5, is obtained for layers annealed for 5 minutes. Further investigations indicated no improvements upon further lowering of anneal time. In fig 6 the corresponding I-V curves are shown. The 5 minutes anneal starts conducting at the highest voltage and also has the highest E_{bd}. Concluding: the 5 min anneal was the optimum anneal time.

The third process variable was the pressure during annealing at a constant temperature of 925°C for 5 minutes. The Weibull distribution of all layers is shown in fig 7. The best combination of Q_{bd} and ΔV, shown in fig 8, is obtained for layers, annealed at a pressure of 21 and 25 Torr. Although the layer, annealed at 21 Torr, shows a better distribution, the layer annealed at 25 Torr results in the highest Q_{bd}-value (25 C/cm^2). In fig 9 the corresponding I-V curves are shown. Hardly any differences are found between the anneal variants. So the optimal combination of electrical properties is obtained for annealing at 925°C, at a pressure of 25 Torr for 5 minutes. A possible explanation is that longer anneal times and higher temperatures may result in a re-oxidation which leads to silicon consumption and consequently decreasing oxide quality. Lower pressures may result in a lower amount of reactive components and subsequently lower quality dielectric layers.

IV. Conclusion

In conclusion, the above results show that deposited oxides with additional N_2O anneal are a very attractive alternative for replacing poly-oxides as inter-poly dielectric for non volatile memory application. Due to the low thermal budget they are very attractive for embedded applications. In particular it has been shown that optimization of the N_2O anneal conditions results in further improvements of the dielectric layers, without being very critical. The best dielectric layers are obtained at 925°C, 5 minutes and P = 25 Torr. It has desirable low leakage currents and high E_{bd} for bottom electrode electron injection, reduced electron trapping (due to the nitrogen incorporation and densification) and a much larger charge to breakdown ($Q_{bd} \approx 25$ C/cm^2) than the as deposited variant.

Acknowledgements

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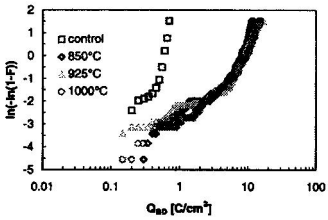

Fig 1: Weibull plot of Q_{bd} as a function of anneal temperature. Electrons are injected from the bottom electrode. A constant current density of 2.5 mA/cm² was applied to capacitor structures with an area of $1*10^{-4}$ cm².

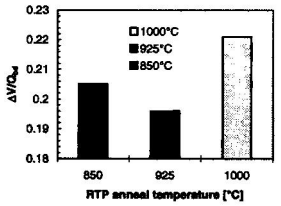

Fig 2: $\Delta V/Q_{bd}$ as a function of anneal temperature. The control oxide is not shown as a consequence of the scalability ($\Delta V/Q_{bd}$=5.5).

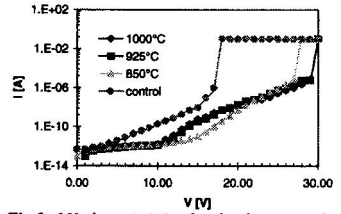

Fig 3: I-V characteristics for the three anneal temperatures and the control oxide. The dielectric thickness of all capacitor structures was 25 nm.

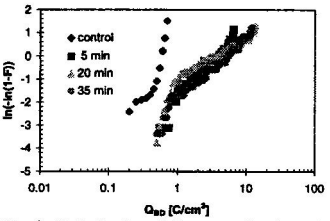

Fig 4: Weibull plot of Q_{bd} as a function of anneal time. Electrons are injected from the bottom electrode. A constant current density of 2.5 mA/cm² was applied to capacitor structures with an area of $1*10^{-4}$ cm².

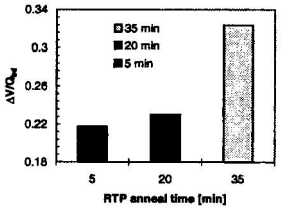

Fig 5: $\Delta V/Q_{bd}$ as a function of anneal time. The control oxide is not shown as a consequence of the scalability ($\Delta V/Q_{bd}$=5.5).

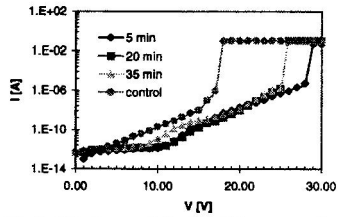

Fig 6: I-V characteristics for different anneal times and the control oxide. The dielectric thickness of all capacitor structures was 25 nm.

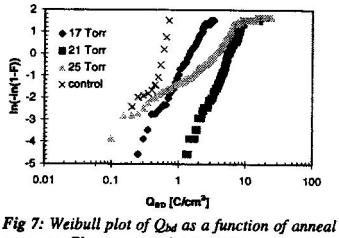

Fig 7: Weibull plot of Q_{bd} as a function of anneal pressure. Electrons are injected from the bottom electrode. A constant current density of 2.5 mA/cm² was applied to capacitor structures with an area of $1*10^{-4}$ cm².

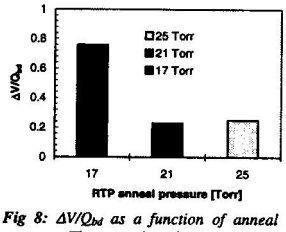

Fig 8: $\Delta V/Q_{bd}$ as a function of anneal pressure. The control oxide is not shown as a consequence of the scalability ($\Delta V/Q_{bd}$=5.5).

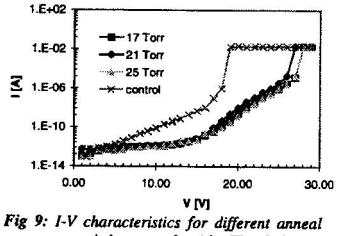

Fig 9: I-V characteristics for different anneal pressures and the control oxide. The dielectric thickness of all capacitor structures was 25 nm.

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