A 5.5MHZ CMOS LOW-PASS FILTER USING A 'SOFT-SWITCHED' TRANSCONDUCTOR.

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ABSTRACT

A new transconductor has been used to implement a third-order 5.5MHz low-pass Bessel filter with extra notch. The filter was realised in 0.5µm double poly N-well CMOS process. At a 3.3V supply voltage the filter dissipates 12mW and the dynamic range equals 62dB where the THD is -50dB for an input voltage of 1Vpp. The continuously tuneable transconductor is based on 'soft-switching' of resistors. The converter performance is only determined by the first order characteristics of the transistor. Due to reduced sensitivity for the second order effects of the transistors the converter is well suitable in modern and future sub-micron CMOS processes.

INTRODUCTION

Nowadays a lot of signal processing, for example in video applications, is implemented by digital VLSI realised in a sub-micron CMOS processes. Before sampling an analogue video signal with an A/D converter an anti-aliasing filter with a relatively constant group delay in the pass-band is needed. A filter for this purpose is described here. The cut-off frequency is ±30% tuneable to correct for temperature and process variations, however an automatic tuning is not yet applied here. The filter has been realised using the transconductance-C technique which is suitable for high frequency filters in CMOS [1,2,3]. In a sub-micron CMOS process the transistors suffer from second-order effects such as mobility reduction and velocity saturation. This results usually in relatively high distortion figures and a decreasing tuning range for most transconductor concepts relying on the MOS transistor characteristics. The proposed transconductor relies in first order on resistors. The resistors are 'soft-switched' by means of transistors in order to make the transconductance continuously tuneable. In this way the *first* order characteristics of the transistors affect only the *second* order effects of the transconductor whereas the *second* order effects of the transistor are hardly of interest, making the transconductor suitable for implementation in a sub-micron CMOS process. The transconductor is continuously tuneable, the tuning mechanism will be described in the next section.

THE TRANSCONDUCTOR

The transconductor schematic is given in figure 1. The core consists of a differential pair M1a,b, degeneration resistors R2a,b through R5a,b and the 'soft-switches' M2 through M5. The tuning mechanism is based on the gradual 'short-circuiting' of the degeneration resistors by means of the 'soft-switches' where V_{tune} is the tuning voltage. For increasing values of V_{tune}, M2 conducts first and M5 will conduct last due to the differences in the effective gate source voltages.

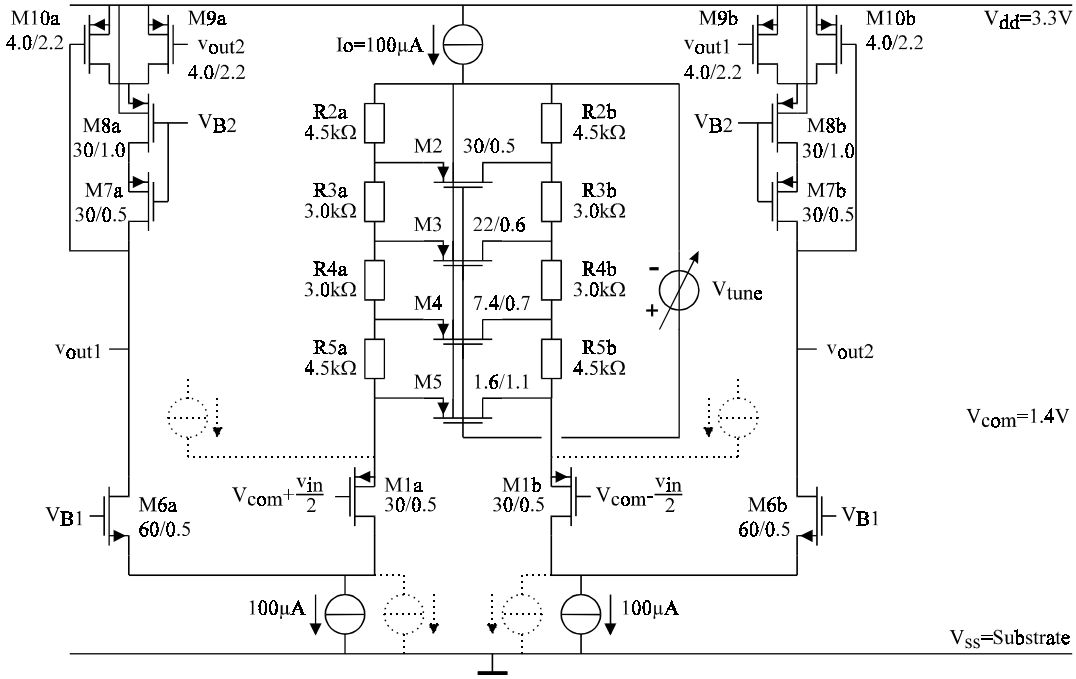

Figure 1: Schematic of the complete transconductor.

The gates of all the 'soft-switches' are connected to the same node. Because of the DC-voltage drop over the resistors R3a,b through R5a,b the effective gate source voltages differ:

$$\left|V_{GSeff_2}\right| > \left|V_{GSeff_3}\right| > \left|V_{GSeff_4}\right| > \left|V_{GSeff_5}\right| \qquad (1)$$

This condition is always valid thanks to the topology of the circuit. The body-effect of the 'soft-switches' further increases the differences of the effective gate source voltages and therefore improves the 'switching' performance.

Thus by increasing the voltage V_{tune}, the transconductance can be tuned to a higher value: M2 is switched on while M3 through M5 are off. Due to the resistive divider the drain-source voltage of M2 is only a fraction of the input voltage, resulting in a low distortion contribution of M2. Moreover, if M2 conducts the drain-source voltage of M3 decreases and therefore the distortion of M3 decreases if M3 is switched on softly. The same mechanism is valid for M4 and M5. Consequently, the distortion of the complete transconductor is low and hardly dependent on the second order effects of the transistors.

The implementation of the voltage source V_{tune} is given in figure 2. The tuning is realised via I_{tune}. The tail current I_O is compensated for I_{tune} so that the biasing of the circuit does not change. The output of the transconductor is terminated with an NMOS folded cascode and a PMOS common mode feedback circuit is applied. For increasing transconductance values, the current modulation of the input transistors M1a,b increases. Without extra measures these transistors will dominant the overall distortion figures. Therefore extra DC currents, equal to the tune current, are injected in the sources of the input transistors. The four extra current sources (dashed lines in figure 1) are copies of I_{tune} and have a maximum value of 50µA.

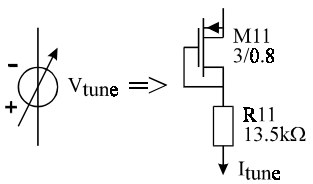

Figure 2: V_{tune} Implementation.

In this design the noise of the transconductor is mainly determined by the current sources of the folded cascodes and the common mode circuit. The noise current of the core of the transconductor is relatively low. The 'soft-switches' produce only thermal noise and no 1/f noise since the DC current is zero. If $v_{in} \neq 0$ the voltage noise at the gates of the 'soft-switches' introduce some current noise in the signal path.

The transconductance was measured versus v_{in}, the measurement results are given in figure 3. For high and low transconductance values the curve is convex. In these situations the circuit behaves similar as a degenerated differential pair. For intermediate values transconductance values the curves are concave. The 'soft-switches' are forced into saturation by the input signal which leads to an increase of the transconductance. The transconductance is tuneable with tune current I_{tune}. The worst case THD of the transconductor for an input voltage of $1V_{ppdiff}$ and a frequency of 1kHz is -50dB.

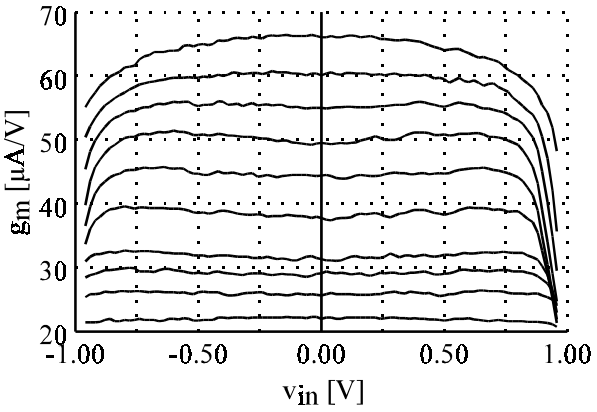

Figure 3: Measured transconductance versus v_{in}, parameter I_{tune} (max. 50µA)

A 5.5MHZ LOW-PASS FILTER

A third-order 5.5MHz low-pass Bessel filter with extra notch for improved stop-band damping and small group delay variation has been realised using the described transconductor in a 0.5µm double poly N-well CMOS process. A passive prototype circuit is given in figure 4, a balanced active implementation in given in figure 5. The filter topology is similar as in [1,3]. A chip photo of the complete filter is given in figure 6, the required area is $0.15mm^2$.

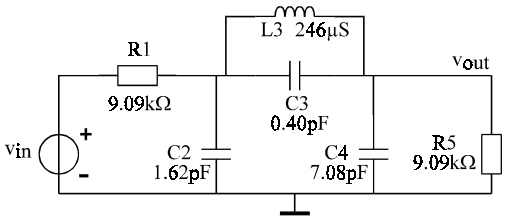

Figure 4: Passive filter prototype.

The gain of the filter was measured and the results are shown in figure 7. The -3dB cut-off frequency can be tuned manually from 2.2 to 6.7MHz by means of the tune current. The depth of the notch depends on the tuning due to the varying phase-shift of the transconductor, which is less than 0.4° at 5.5MHz for the nominal transconductance value. Table 1 shows the list of experimental results.

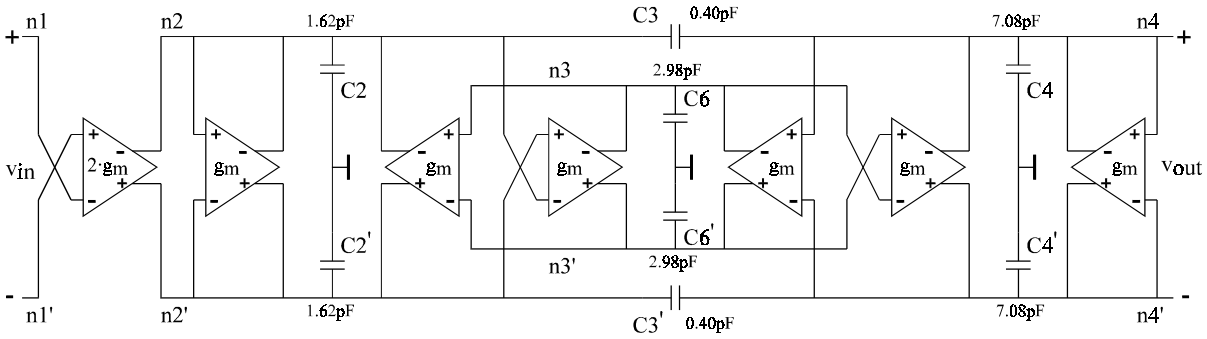

Figure 5: Active gm-C filter implementation, g_m=55µS.

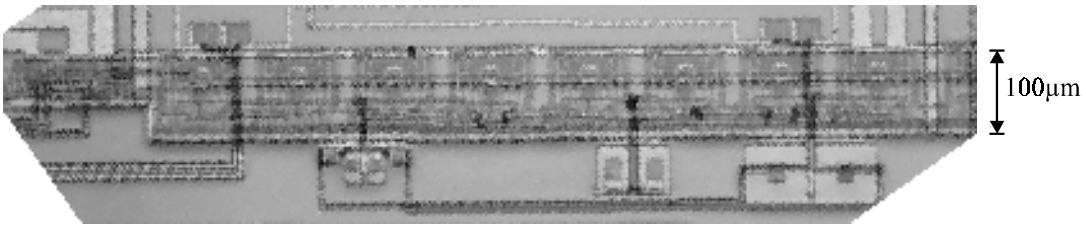

Figure 6: Chip photo of realised filter.

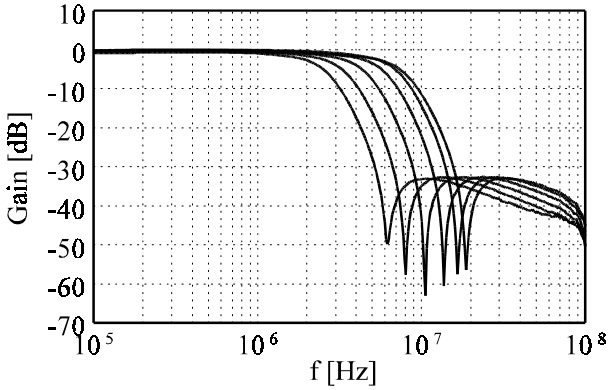

Figure 7: Measured filter gain, parameter I_{tune}.

Parameter	Value
f_{-3dB} nominal	5.5MHz
f_{-3dB} tuning range	2.2-6.7MHz
Output noise, 0-5.5MHz	$268\mu V_{RMS}$
v_{inmax}, THD≤-50dB, 0-5.5MHz	$1V_{ppdiff}$
Dyn. Range, THD≤-50dB	62dB
CMMR, v_{in}=0V	-50dB
Power dissipation (Vdd=3.3V)	12mW
Chip area, (0.5µm CMOS)	$0.15mm^2$

Table 1: Experimental filter results.

CONCLUSIONS

A third-order 5.5MHz continuous-time low-pass filter using a new transconductor design has been realised in a 0.5µm double poly CMOS process. The input voltage of the filter can be $1V_{ppdiff}$ whereas the THD is less than -50dB in the whole pass-band. The filter consumes 12mW on a 3.3V supply voltage. The *second* order effects of the continuously tuneable 'soft-switched' resistor based transconductor are determined by the *first* order transistor characteristics. The *second* order effects of the transistor hardly affect the transconductor performance which makes the circuit also suitable for future CMOS technologies. The transconductor has been designed for mixed mode VLSI designs implemented in a modern sub-micron CMOS process.

ACKNOWLEDGEMENTS

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