A Nonvolatile Analog Programmable Voltage Source using the VIPMOS EEPROM structure

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Abstract
A programmable voltage source using the Vertical Injection Punch-through based MOS EEPROM structure has been developed. The circuit operates at a single 5 V supply and the output voltage is continuously available also during programming. The effect of programming is linearly dependent on the programming time.

1. Introduction

In recent years several attempts have been made for nonvolatile analog data storage on EEPROMs. Examples of applications are offset compensation in opamps [1], analog weight storage for neural networks [2] and analog recording of speech [3]. High voltage pulses are needed for both programming and erasing, so the floating gate potential changes dramatically during programming and erasing. An iterating process is necessary for establishing the desired charge on the floating gate. If the Vertical Injection Punch-through based MOS EEPROM structure is used, programming can be very well controlled without cross-talk of pulses. In section 2 the VIPMOS structure is explained. A programmable voltage source using the VIPMOS structure is presented in section 3. This voltage source can, for instance, be used to set the multiplication factor of a multiplier in a programmable filter. Section 4 describes the operation of the circuit and measurement results are given in section 5. In section 6 some conclusions are given.

2. The VIPMOS EEPROM

The VIPMOS EEPROM structure is given in figure 1 and has been described in [4, 5]. A N-type buried injector is formed under the floating gate of an EEPROM by high energy ion implantation. If the potential difference between the drain and injector exceeds the so called punch-through voltage a punch-through current I_{pt} flows according to

$$I_{pt} = I_0 \exp \frac{q(V_d - V_{inj} - V_{pt})}{nkT} \qquad n = \text{non-ideality factor} \qquad (1)$$

and can be very well controlled by means of a controlled current source connected to the injector. Some of the electrons, flowing from the injector towards the channel, will be injected into the floating gate, the others are collected by the drain. The ratio between the gate current and the punch-through current is called the injection probability P_{inj}. This probability depends on the floating gate potential [6] and the injector current. Connecting the injector to the supply voltage disables programming.

A channel must be present under the floating gate, so the floating gate potential must exceed the threshold voltage. A high voltage, applied to the erase gate, removes the electrons by tunnelling and erases the VIPMOS.

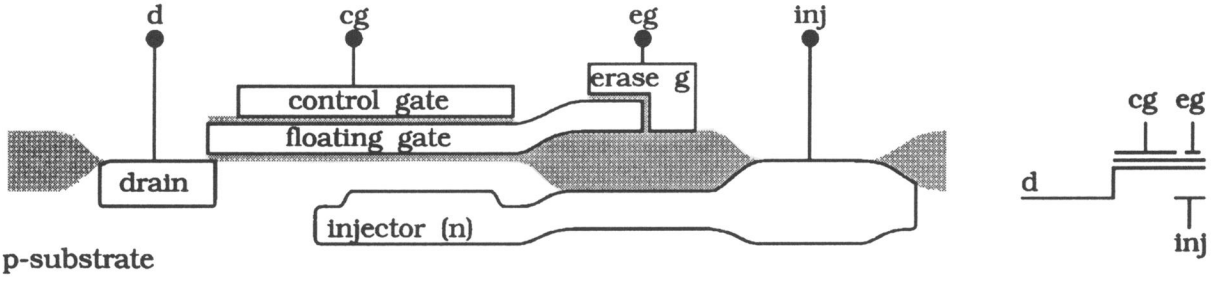

figure 1 The VIPMOS EEPROM structure and circuit scheme

3. The programmable voltage source

The floating gate can only be connected to other gates to prevent charge leakage. To sense the potential of the floating gate a separate sense transistor can be used. If a channel is present under both the VIPMOS structure and this sense transistor the potential of the floating gate is

$$V_{fg} = V_{cg}\frac{C_{cg}}{C_{tot}} + V_{eg}\frac{C_{eg}}{C_{tot}} + V_{ch}\frac{C_{ch}}{C_{tot}} + V_{chs}\frac{C_{chs}}{C_{tot}} + \frac{Q_{fg}}{C_{tot}} \qquad (2)$$

$$C_{tot} = C_{cg} + C_{eg} + C_{ch} + C_{chs}.$$

It is a function of the potentials of the control gate V_{cg} and erase gate V_{eg}, the channel potentials of the VIPMOS structure V_{ch} and the sense transistor V_{chs}, the capacitances of the erase gate C_{eg}, the control gate C_{cg} and the channels C_{ch}, C_{chs} with respect to the floating gate and the stored charge Q_{fg}. The potentials are referred to the substrate.

For a constant potential of the erase gate and the channels, the floating gate potential is only dependent on the control gate potential and the stored charge. If the floating gate potential is kept constant, for instance by a feed-back loop, the control gate potential is linearly dependent on the charge. A constant floating gate potential implies a constant injection probability, so changes in the control gate potential are linearly dependent on the program current I_{prog} and program time t_{prog} according to

$$\Delta V_{cg} = \frac{I_{prog}\, t_{prog}\, P_{inj}}{C_{cg}}. \qquad (3)$$

Parasitic capacitances, such as overlap capacitances, do not influence the program behaviour.

Figure 2 shows a circuit keeping the potential of the VIPMOS channel constant and providing a constant biasing for the sense transistor N6. The biasing for N6 is provided by P1 and P5. P1-P2 and N3-N4 compare the current flowing through the sense transistor and a reference current and eliminates differences between these currents by changing the control gate potential. A constant current

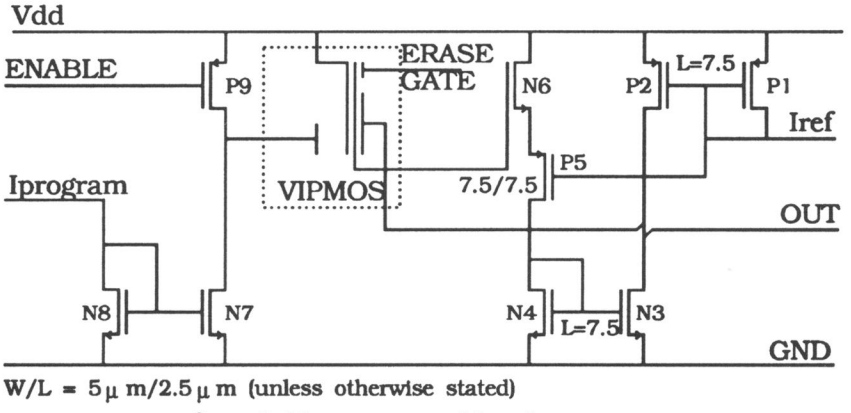

figure 2 The programmable voltage source

through the sense transistor implies a constant floating gate potential and ensures a channel under the VIPMOS structure. The control gate potential is the output of the circuit. The parallel output impedances of P2 and N3 form the output impedance of the circuit. If the output must deliver a current, a buffer [7] is necessary, but if the output is only connected to gates, the circuit of figure 2 can be used directly. Current mirror N7-N8 mirrors the program current into the injector and the enable transistor P9 connects the injector to the supply voltage if programming is disabled.

The minimum supply voltage for the circuit is dependent on the V_{pt} of the VIPMOS. The minimum injector potential is equal to the saturation voltage of N7. From equation (1) the minimum drain voltage can be calculated. The minimum and maximum output voltages are determined by the saturation voltages of N3 and P2. For erasing a high voltage is needed. This voltage can be provided by an on-chip charge pump circuit, since the erase voltage is only connected to the high impedant erase gate.

4. Circuit operation

During normal operation only the supply voltage and the reference current have to be applied to the circuit and the ENABLE input must be connected to ground. For programming the ENABLE input must be connected to the supply voltage and a program current must be applied. Before the feed-back loop can become active, erasing is necessary, since a channel must be present under the sense transistor.

The stability of the feedback loop P1-N6 + VIPMOS has been investigated by simulations. The open loop gain is 27.3 dB, the unity gain frequency 6.8 MHz and the phase margin 87°. A capacitive load on the output lowers the first pole, so a capacitive load does not lead to instabilities. For a 100 pF load the simulation results are an unity gain frequency of 71 kHz and a phase margin of 92°.

5. Measurement results

The circuit has been realized in a 2.5 μm CMOS process. The area consumption is 65 . 56 = 3640 μm^2.

In figure 3 the injector potential as a function of the floating gate potential is shown for different injector currents and a constant drain voltage of 5 V. A separate VIPMOS structure with a contacted "floating gate" is used for these measurements. For floating gate potentials below 6 V no punch-through occurs. The injector-substrate junction is forward biased and the injector current flows into the substrate. If V_{fg} exceeds 10 V an inversion layer is present and the injector current flows into this layer. The injector voltage for program conditions is 2 V, if a 5 V supply is used, so a current mirror can be used to control the injector current and the complete circuit can operate at a single 5 V supply.

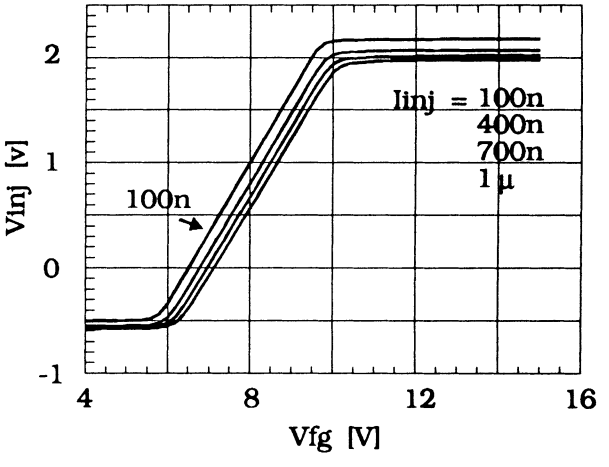

figure 3 Injector potential vs floating gate potential for different injector currents. (Vdrain = 5 V)

Figure 4 shows two different programming characteristics, measured on a complete circuit. The circuit has been erased by an off-chip high voltage of 25 V. A constant program current of 1 μA has been applied to the circuit and the reference current was 10 μA. For curve *a* enable pulses with a pulse length of 250 μs have been applied to the ENABLE input. For curve *b* this pulse length was 1 ms. The figure does not show the actual transient behaviour but only the effect of the program pulses, so the time scale is arbitrary. The average ΔV_{out} for every pulse is 109 mV for curve *a* and 448 mV for curve *b*. The variance in the step size is

2% and measurements for different program currents and times all showed a variance of maximum 2%. Since the program current must discharge the injector-substrate capacitance before programming, the average ΔV_{out} for 1 ms pulses is a little larger compared to four 250 μs pulses. The control gate capacitance is 85 fF which gives, according to equation (3), an injection probability of 37 10^{-6} for a program current of 1 μA.

The transient behaviour of the output voltage during programming is shown in figure 5. At t = 0 ms an enable pulse of 2 ms has been given. The program current was 500 nA. The figure shows that the output voltage can be monitored during programming. At t = 0 ms and t = 2 ms cross-talk is visible at the output. The program current causes a voltage drop over the channel of the VIPMOS structure. According to equation (2) this voltage drop will influence the control gate potential, if the floating gate potential is kept constant. The measured cross-talk is 30 mV at the start and at the end of programming. The voltage drop over the channel is linearly dependent on the program current. Ramping down the program current, in stead of switching the injector, makes the cross talk of the program current to the output negligible. Measurements at a program current of 1 nA showed no measurable cross-talk of the enable signal to the output (< 2 mV).

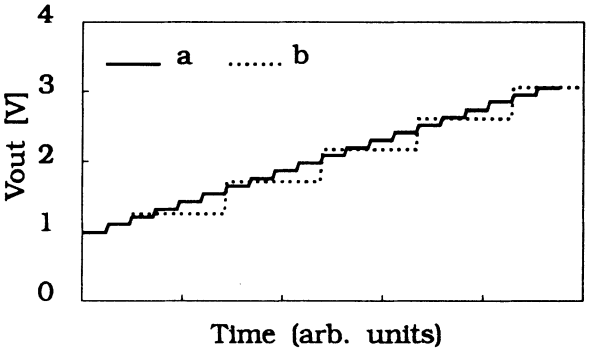

figure 4
programming characteristics

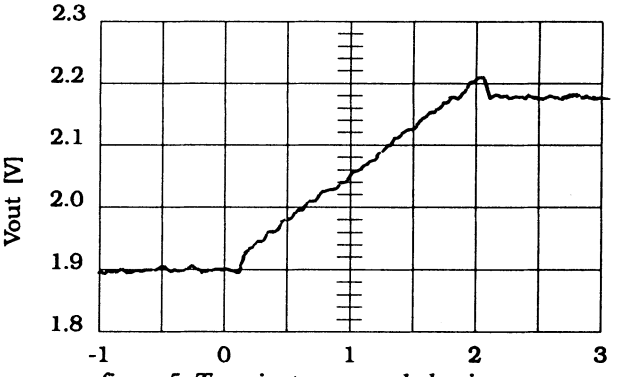

figure 5 Transient program behaviour

6. Conclusions

A 5 V only nonvolatile analog programmable voltage source has been developed. The circuit can be programmed by a current. The output voltage is linearly dependent on the program time. During programming only cross-talk of the program current and not of the enable pulse is measured on the output. This makes it possible to program the circuit by means of a feed-back loop. The program current must be made dependent on the difference of the measured and desired output potential. After the desired output potential is reached, programming can be disabled.

7. References

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