A 110mW, 0.04mm^2, 11GS/s 9-bit interleaved DAC in 28nm FDSOI with >50dB SFDR across Nyquist

Erik Olieman, Anne-Johan Annema, Bram Nauta
University of Twente, Enschede, The Netherlands

Abstract

A 9-bit 11GS/s current-steering (CS) digital-to-analog converter (DAC) is designed in 28nm FDSOI. The DAC uses two-times interleaving to suppress the effects of the main error mechanisms of CS DACs while its clock timing can be tuned by the back gates bias voltage of the multiplexer transistors. The DAC achieves higher than 50dB SFDR and less than -50dBc IM3 over Nyquist at a sampling rate of 11GS/s, occupying only 0.04mm2 and consuming 110mW from a single 1V supply.

Keywords: DAC, interleaving, quad-switching, FDSOI

Introduction

Conventional CS DACs are limited in performance by static and dynamic errors; the latter typically limit high speed performance. The main dynamic errors are due to the output capacitance of the current sources, signal dependent supply and bias loading effects and other switching related errors. Techniques such as additional cascodes with bleeding current sources [1] and return-to-zero switching schemes can suppress some of these errors, but they have their own specific drawbacks. Here quad-switching [2] is combined with interleaving [3] to suppress the dominant dynamic errors in CS DACs.

Interleaved architecture

The architecture of the interleaved CS DAC is shown in Fig. 1; it shows the two parallel sub-DACs (sDACs) that operate out of phase and shows the analog multiplexer that toggles the outputs of each sDAC between the overall DAC output and a dummy output. The sDACs are conventional CS DACs, consisting of many current sources and their accompanying switches (slices) in parallel. During the time an sDAC is connected to the dummy output it switches to its next code. Since the dynamic errors of a CS DAC are centered around the code switching moment, these errors are dumped on the dummy output and hence do not propagate to the overall DAC output. Once these errors are sufficiently stabilized, the analog multiplexer connects the sDAC to the output, after which the second sDAC switches to its next code while being connected to the dummy output. This way each sDACs runs at half the sampling clock, with out-of-phase clocks for the two sDACs. Although interleaved DACs use multiple sub-DACs that all consume power and area, the significantly lower demands on timing and settling in the individual sDACs allows to design overall power and area efficient DACs.

For sufficiently high spurious-free dynamic range (SFDR) , the dynamic effects on the bias and power supply lines also must be sufficiently small and must be code-independent. The interleaving structure already allows for extra settling time, while we also implemented quad-switching [2] to ensure code-independent switching activity. Quad-switching uses four switches for one sDAC slice, two at the positive output and two at the negative output. Of these four switches, only one switch is on in each sample interval. In each new sample interval, another switch will be turned on; the code determines whether that switch is connected to the positive or the negative output. Overall this yields code independent dynamic load on both the power supply and on the bias voltages. In a regular CS DAC employing quad-switching, mismatch in timing and switching behavior of the switches generates additional spurs. In the interleaved architecture these dynamic quad-switching errors are suppressed by the interleaving mechanism, while the advantages of quad-switching are maintained.

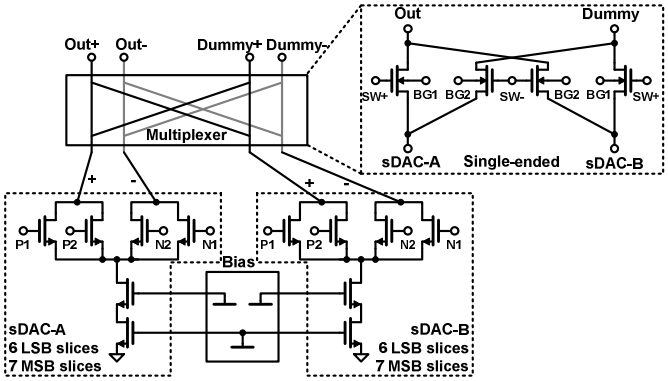

Fig. 1: Interleaved DAC architecture

The interleaved architecture removes most of the settling-related errors occurring in CS DACs, but it also introduces new performance limiting artifacts [3]. Due to interleaving, the current-source matching requirements between all sDAC slices are higher. Furthermore, the analog multiplexer that toggles between the two sDACs has high timing requirements while switching code-dependent currents; this may introduce distortion if not handled correctly. These topics will be addressed below.

The presented DAC uses static matching only, with 6 LSB bits binary implemented, and the 3 MSB bits using thermometer code. All current sources are placed in a common-centroid layout; cascode transistors are used to increase the current sources' output impedance. The current source transistors of both sDACs have a single combined bias source to improve matching; the cascode transistors have combined bias sources per sDAC to decrease crosstalk between the two sDACs. The matching properties of FDSOI transistors result in sufficient static matching between the sDACs for the required SFDR.

The timing of the analog multiplexer is critical for a good SFDR, with timing constraints more stringent than those of a regular current steering DAC. The timing error in the crossing point of the differential output of the multiplexer driver must be less than 180fs to reach 50dB SFDR across Nyquist at 11GS/s. Due to the centralized nature of the driver good matching is realized, however passive matching alone is insufficient to reliably reach the <180fs accuracy. We implemented a quasi-DC timing error estimation [3] which is used to tune the threshold voltage of the transistors in the analog multiplexer. This threshold voltage adjustment is easily done changing the voltage applied to the back gate of the FDSOI transistors. In our design, the back-gate voltages of the multiplexer transistors connected to the positive switch signal and those connected to the negative signal can be tuned

independently, see Fig. 1.

The analog multiplexer switches the total (code dependent) output current of the sDACs to either the overall DAC output or to the dummy output. To ensure low distortion for a wide range of currents, the multiplexer switches operate in triode, where transistor behavior is far less dependent on drain current compared to saturation region. This operation in the triode region requires gate-voltages higher than the power supply voltage which is achieved using a capacitive level shifter.

Measurement results

The DAC utilizes a single clock input of 11GHz; a clock divider generates from this a differential 5.5GHz clock, which is used as sole clock source for all other components of the DAC. Simple inverter-based delays are used to create correct timing relations throughout the DAC. The DAC is produced in a 28nm FDSOI CMOS process and occupies 0.04mm^2; the die micrograph is shown in Fig. 2. A 126 word memory provides the required test signals. The load for both the regular output and the dummy output consists of 50 Ohm on-chip resistors in parallel to 50 Ohm off-chip load. The outputs are biased with a DC-choke, with the DC output voltage at 0.9V. The measurements are done with the chip packaged in a standard QFN32 package using wire bonding.

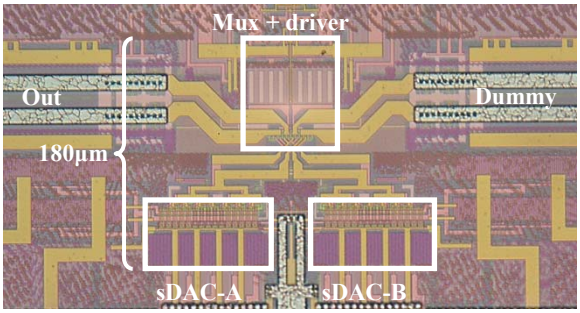

Fig. 2: Die photograph of the DAC core

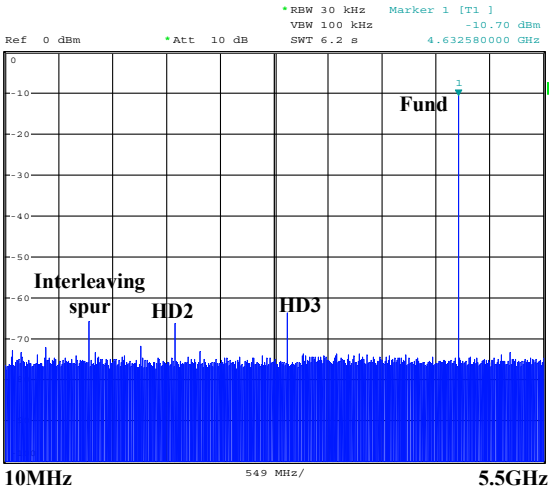

Fig. 3: Measured output spectrum with 4.6GHz full-scale sine output across Nyquist at 11GS/s

The DAC consumes 110mW, excluding memory, from its 1.0V supply, of which 35mW is static power, at its nominal speed of 11GS/s and an output swing of 425mVpp-diff. A plot of the output spectrum is shown in Fig. 3, the interleaving spur due to imperfect matching of the two sDACs is not limiting performance. Fig. 4 shows the SFDR and IM3 performance versus output frequency. Across Nyquist the DAC achieves >51dB SFDR and <-51 dBc IM3 performance. Fig. 5 compares performance against state-of-the-art CMOS DACs. While using more power than [4], it offers similar linearity across a 3.5 times larger bandwidth. Compared to [1,2,5] our design achieves similar or better SFDR at much lower power and area consumption, which shows the advantages that can be obtained by applying interleaving to CS DACs. While our calibrated DAC without quad switching in [3] has a higher SFDR, the current design shows that a much higher bandwidth can be achieved in a small passively matched interleaved DAC using quad-switching. Both regular spurs and quad-switching related spurs are suppressed by the interleaving architecture.

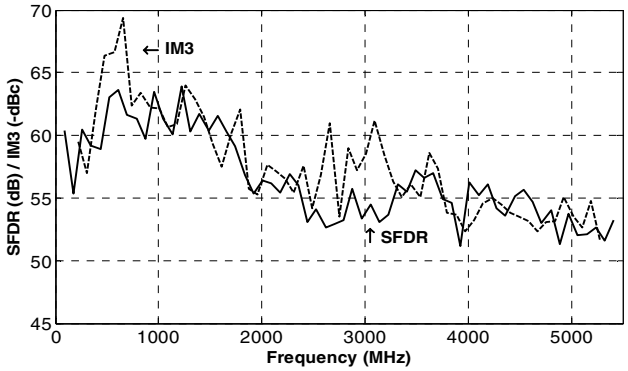

Fig. 4: SFDR and IM3 versus output frequency at 11GS/s

	This	[1]	[2]	[3]	[4]	[5]
Tech	28nm FDSOI	28nm	180nm	65nm	65nm	65nm
Resolution [Bits]	9	13	14	12	9	6
Power [mW]	110	375	>600	70	60	750
V_{supply} [V]	1.0	1.8	-1.5/1.8	1.2	1.2	1.1/2.5
Area [mm^2]	0.04	1.16	4	0.4	0.04	0.24
Swing [$V_{pp\text{-}diff}$]	0.425	N/A[b]	1.0	0.5	0.4	0.6
Fs [GHz]	11	9	6	1.7	3	56
SFDR[a] [dB]	51	-	52	58	49	43
IM3[a] [dBc]	-51	-44	-65	-62.5	-60	-

a) Worst-case reported SFDR/IM3 up to Nyquist/5.5GHz

b) Output power is 13.5dBm at unknown impedance level/voltage swing

Figure 5: Comparison table

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