45° Light Turning Mirrors for Hybrid Integration of Silica Optical Waveguides and Photo-detectors

F.Civitci, G.Sengo, A. Driessen, M. Pollnau, and H.J.W.M. Hoekstra
Integrated Optical MicroSystems Group (MESA+)
University of Twente, Enschede, The Netherlands

A.J. Annema
Integrated Circuit Design Group (CTIT)
University of Twente, Enschede, The Netherlands

***Abstract*—For hybrid integration of an optical chip with an electronic chip with photo diodes and electronic processing, light must be coupled from the optical chip to the electronic chip. This paper presents a method to fabricate metal-free 45° quasi-total internal reflecting mirrors in optical chips that enable 90° out-of-plane light coupling between flip-chip bonded chips. This method is fully compatible with fabrication of conventional optical chips. The mirrors are created using anisotropic etching of 45° facets in a Si substrate followed by fabrication of optical structures. After removal of the mirror-defining Si structures by isotropic etching, the obtained air-optical structure interface directs the output of the waveguides to out-of-plane photo detectors that are mounted flip-chip on the optical chip. Simulations show a reflection efficiency of 72.3 %, while experimentally 47% was measured on a not fully optimized first batch.**

Keywords- light turning mirrors; hybrid integration; silica waveguides; photo-detector arrays; integrated optics

I. INTRODUCTION

In recent years, waveguide (WG) based integrated optic devices have been used in many applications such as tele-communication, optical spectroscopy, biological sensing and signal processing in medical imaging. Usually the WG outputs are measured using photo-diodes (PDs), which are dedicated to certain applications, such as time gating in spectroscopic research or in diagnostics. In particular for (high resolution) spectroscopy a large number of different channel outputs are measured, which can be done most conveniently with 2D arrays of PDs. Monolithic integration of the latter into the Si substrate of an optical chip has several disadvantages: (i) if the PDs and their electronic processing circuitry are fabricated first, the temperature budget to fabricate the optical structures (such as LPCVD and reflow of deposited layers) is severely limited, to about 400 °C, and (ii) fabrication of PDs and their electronic processing circuitry on each optical chip would be far more expensive than processing a CMOS chip that includes PDs and electronics to be flip-chip mounted on an optical die. To enable efficient optical coupling between an optical die and a flip-chip mounted electronics die, low cost high efficiency 45° out-of-plane mirrors in optical chips are favorable. This is the subject of this paper.

A number of techniques have been reported to provide a connection between WGs and PDs of two flip-chip mounted chips. One of these uses a focusing grating coupler on top of a WG to focus the light onto the PD that is placed above the WG [1]. However, this device can only work for a limited wavelength range which is defined by the grating period. In addition, high volume production of such a grating would be very expensive, owing to its relatively small period. Another technique uses focused ion beam (FIB) milling for fabricating total internal reflection (TIR) mirrors at the end of silica WGs [2]. However, this technique is not suitable for high volume production due to the relatively low speed of FIB and the associated high cost. The third technique is based on a metal mirror, at which the desired mirror angle is fabricated by using a superficial layer in the wet etching process of the buffer layer [3]. Although the efficiency of these mirrors is very high (up to 95 %), the thermal budget of the fabrication process is low because the melting temperature of the metal layer used in the mirror is around 650 °C.

In this paper, we propose a new method to fabricate 45° mirrors in optical chips that enable high efficiency 90° out-of-plane light coupling to a flip-chip mounted electronic chip holding 2D PD arrays with their processing electronics. The fabrication process for these mirrors is suitable for batch production and has a thermal budget of 900 °C. The mirror is defined by anisotropic etching of 45° facets in the Si substrate. After optical WG fabrication the mirror is formed, by locally removing the Si facets, at the interface between the optical WG and air.

The paper is organized as follows. Section II reviews the fabrication process steps for realizing the mirror. Section II shows simulation results for estimating the mirror performance; section IV presents some measurement results.

II. FABRICATION PROCESS

The wafer cross-sections corresponding to different steps in the fabrication process flow are shown in figure 1(a)-1(j). The fabrication process starts with 200 nm thermal oxide growth to be used as a mask for the anisotropic Si etching. After that the oxide is patterned by using buffered HF (BHF) etching (1-a). This is followed by 5 µm deep anisotropic etching of Si (1-b). This depth is defined by the required thickness of the buffer layer, which should be 3.5 µm to prevent substrate losses, and by the thickness of the oxide layer above the SiON WG (~1.5 µm) for proper overlap between the diverging WG output and the mirror surface. A TMAH and Triton mixture is used as etchant to form the 45° angled walls [4]. The fabrication process continues with removal of thermal oxide in BHF.

This research is financially supported by the STW Technology Foundation through project 10051.

Then, a 100 nm thick SiN layer is deposited (1-c) just before deposition of the buffer layer in order to prevent molecular diffusion between the latter and the Si substrate. After that a thick Boron Phosphorous Doped Silica Glass (BPSG; index: 1.45) film is grown to form the buffer layer (1-d). BPSG is used in order to get rid of the voids in the as deposited layer by post- deposition annealing [5]. The thickness of the BPSG buffer layer should be at least 5 µm, which is equal to the etch depth defined in the anisotropic Si etching step, in order to be able to obtain a flat surface after the following chemical mechanical polishing (CMP) step. The BPSG layer is annealed just after deposition at 900 °C for 16 hours. The annealing step is followed by CMP step (1-e). Subsequently, the BPSG is thinned in a BHF solution such that a 3.5 µm thick buffer layer will remain between the guiding SiON layer and Si substrate (1-f). This is followed by the deposition and patterning of the core SiON (index: 1.585) layer (1-g). After that the cladding BPSG layer is deposited, annealed and polished (CMP), while using the same process conditions as applied for the buffer BPSG (1-h). Then the isotropic Si etching holes are introduced on top of the elevated Si structures (1-i). Finally, the isotropic Si etching is done through these holes (1-j). In this step XeF2 gas phase etching is used to selectively remove Si. By removing the elevated Si structures, 45° mirrors are created.

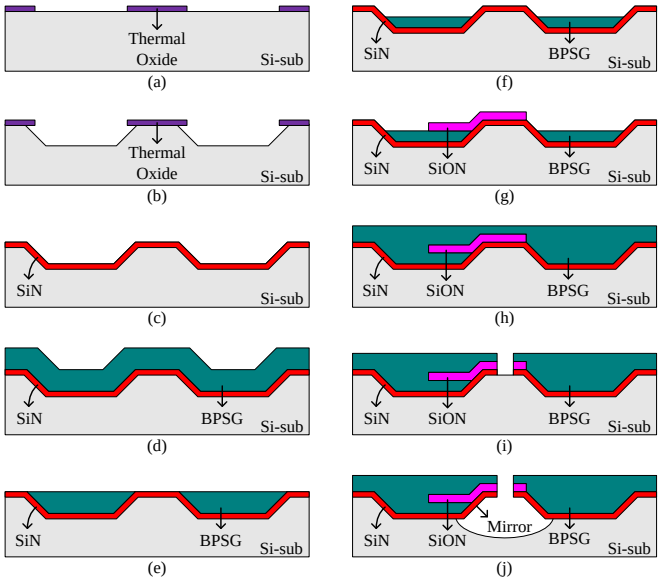

Figure 1. Wafer cross-sections corresponding to different steps in the fabrication process flow.

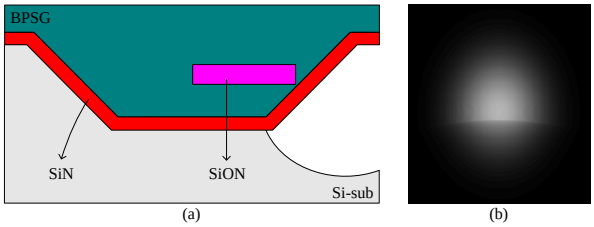

Figure 2. (a) Cross-section of the simplified mirror structure used in the simulation and (b) calculated far field intensity profile.

III. SIMULATIONS

The performance of the proposed mirrors is estimated using a Fourier decomposition of the modal field. The mirror structure used in this simulation is simplified by ignoring the residual SiON layer on the 45° angled wall since the index contrast between BPSG and SiON is very low. Figure 2-(a) shows the cross-section of this (slightly idealized) structure. Figure 2-(b) shows the far field intensity profile. It can be seen from the figure that the intensity profile is not symmetric, which is due to the fact that a part of the Fourier components of the modal field has an angle of incidence on the silica-air interface below the critical angle. For this reason the efficiency of the mirror is calculated to be somewhat below unity, 72.3%.

IV. MEASUREMENTS

The fabricated devices are first characterized by taking the far field intensity patterns of the light reflected from the mirrors. The light of a laser source at 833 nm wavelength is coupled into a single mode optical fiber to excite the WG that is terminated by such a mirror. The light in the WG is reflected from the mirror, hits a diffusive screen 1.5 cm away from the mirror and its image is captured by a camera. The simulated and measured intensity profiles match in size and shape.

The efficiency of the mirror is measured by comparing the mirror output with that of a WG directed to a side facet. Here, differences in the excitation efficiencies of the two corresponding WGs are accounted for by monitoring the light in the WGs with a camera and using the thus measured intensities as a measure for the power in the two WGs. This process is repeated a number of times, to correct for statistical fluctuations. The results show that the efficiency of the fabricated mirror is 47%, which is somewhat lower than the anticipated value (72.3%) due to imperfections in this first batch.

V. CONCLUSIONS

Quasi-TIR based 90° out-of-plane high efficiency light turning mirrors for hybrid flip-chip integration of SiON WGs and CMOS based photodiodes are fabricated. Measurements show an efficiency of 47% while the calculated efficiency is 72.3%; this difference is due to imperfections in fabricating this first batch.

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