LOW-TEMPERATURE PROCESS STEPS for REALIZATION of NON-VOLATILE MEMORY DEVICES

I. Brunets, A. Boogaard, A.A.I. Aarnink, A.I. Kovalgin, R.A.M. Wolters, J. Holleman, J. Schmitz

***Abstract* — In this work, the low-temperature process steps required for the realization of nano-crystal non-volatile memory cells are discussed. An amorphous silicon film, crystallized using a diode pumped solid state green laser irradiating at 532 nm, is proposed as an active layer. The deposition of the subsequent functional layers (e.g., gate oxide) can be done using CVD and ALD reactors in a cluster tool. We show that a high nanocrystal density (Si-NC), required for a good functionality of the memory device, can be obtained by using disilane (Si_2H_6) or trisilane (Si_3H_8, known as Silcore®) as precursors for LPCVD instead of silane, at a deposition temperature of 325 °C. The nanocrystals are encapsulated with an ALD-Al_2O_3 layer (deposited at 300 °C), which serves as oxidation barrier. The passivation of the realized structure is done with an ALD-TiN layer deposited at 425 °C.**

In this work, we realized Al/TiN/Al2O3/Si-NC/SiO2/Si(100) multilayer floating-gate structures, where the crystallized amorphous silicon film was for the time being replaced by a mono-crystalline silicon wafer, and the gate oxide was thermally grown instead of a low-temperature PECVD oxide. The structures were characterized in terms of their performance as memory cells. In addition, the feasibility to use laser crystallization for improving the amorphous silicon films (prior to the gate oxide deposition) was explored.

***Index Terms* — 3-D integration, ALD, CVD, nano-crystal, non-volatile memory, laser crystallization**

I. INTRODUCTION

It is well-known that downsizing of non-volatile memory devices becomes increasingly difficult due to a number of physics-related issues. Therefore, other solutions are to be found such as 3-D integration. Consequently, several new device designs are being investigated as replacements for the traditional floating gate stack, including nanocrystal memory cells [1-4]. Also the targeted 3-D integration strongly increases the demands on process flows with lower thermal budgets, preventing the thermal degradation of underlying device layers [5, 6].

Manuscript received October 1, 2007. This work is supported by the Dutch Technology Foundation (STW). Project number STW-TEL 6358.

I. Brunets, A. Boogaard, A.A.I. Aarnink, A.I. Kovalgin, R.A.M. Wolters, J. Holleman, J. Schmitz are with MESA+ Research Institute, Chair of Semiconductor Components, University of Twente, Hogekamp, P.O. Box 217, 7500 AE Enschede, The Netherlands. Phone: +31 (0)53 489 4394; fax: +31 (0)53 489 1034; e-mail: i.brunets@utwente.nl

Laser crystallization of low-temperature deposited amorphous silicon can provide polysilicon films as active layers at low substrate temperatures, with sufficiently large grains [7-12]. However, inherent to this technique is the random position of grain boundaries, leading to large device-to-device variations. Recently, novel techniques were reported allowing the controlled formation of grain boundaries by the a-Si laser crystallization through air-gap formation [13], two-pass laser crystallization [14], or the introduction of buried crystallization seeds [15]. Bearing manufacturing costs and yield considerations in mind, the most effective solution to the controlled grain formation is still unclear.

In this paper, a novel approach to the controlled grain formation is described. The re-crystallization centers are the amorphous silicon lines fabricated with standard methods. The preformed α-Si lines, patterned prior to the deposition of α-Si, introduce an additional temperature gradient and provide a better controlled lateral crystallization of the molten material. This method can easily be introduced in silicon-compatible process flows and can allow a 3-D integration of devices with significantly improved characteristics.

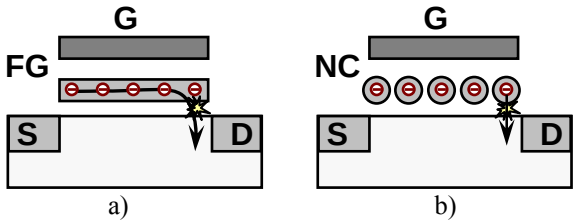

Fig. 1. Possible leakage path in the tunnel oxide in non-volatile memory cell with continuous floating gate (a) and with nano-crystals (b).

The next important step in fabrication of silicon-nanocrystal memory cells is the design and realization of the multilayer gate stack using a low thermal budget (well below 450 °C). The advantage of a discontinuous nanocrystal floating gate over a continuous floating gate is that the charge state is much less dependent on local current leakage through the gate oxide (see Fig. 1a). Having the floating gate, consisting of a large number of nano-crystals, isolated from each other, one can reduce the failure of the devices. The possible leakage current, caused by a defect in the thin low-temperature oxide, will discharge only a single nano-crystal, as shown in Fig. 1b. This allows the use of lower-quality CVD gate oxides instead of

thermally grown oxides.

To investigate the low-temperature process steps, we built our CVD cluster tool, combining ALD of metal oxides and metal nitrides, with IC-plasma deposition of dielectrics. With this tool, all essential deposition steps for the device can be carried out at low temperatures and without vacuum break. Although (100) silicon wafers were used for the first experiments, the complete memory devices would be realized on the re-crystallized amorphous-silicon layers, opening a route to 3-D memory structures compatible to backend processing.

II. Process Steps and Layer Characterization

A. *Laser crystallization of α-Si films*

To realize a controllable crystallization of the amorphous silicon films, we used preformed α-Si lines patterned prior to the deposition of the amorphous films (see Fig. 2). First, a 50 nm thick α-Si film was deposited by LPCVD at 550 °C on top of a 0.7-µm thick thermally grown SiO_2 layer. After patterning the film, the lines with different widths (from 0.4 up to 2.0 µm) were formed. Subsequently, a 100-nm thick α-Si layer was deposited using the same technique, which resulted in an amorphous film with a periodically varied thickness.

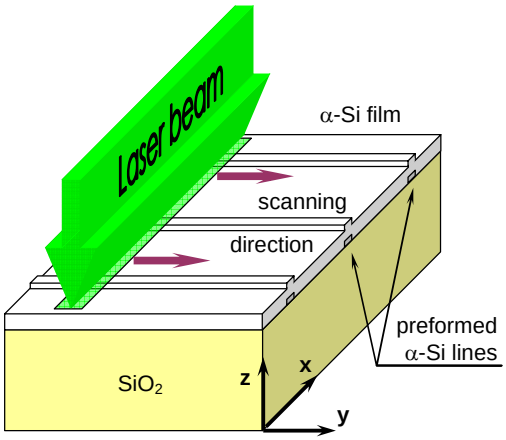

Fig. 2. The laser crystallization process of a silicon film with preformed lines.

The film crystallization was carried out using the laser optical system LAVA available at Innovavent GmbH. The system provided an up to 54 mm wide green laser beam (532 nm). The laser system created a laser beam with a uniform top-hat profile along the x axis and a Gaussian profile along the y axis. The beam's intensity profile was measured on the wafer plane using a beam profiling system equipped with a CCD camera, and a 40× microscope. The applied beam length was 5.15 mm and the width was 5.8 µm, both Full-Width Half-Maximum (FWHM) values. The average energy density in the beam was adjusted by an optical attenuator. The energy densities were calculated by dividing the total pulse energy by the FWHM area of the beam.

We used a frequency doubled Nd:YAG laser (model LDP-100MQG from Lee Laser) irradiating with an average power of 42.5 W at a repetition rate of 8.8 kHz. The pulse duration was 200 ns. The scan velocity was 1 mm/second. The wafer was located on a high accuracy motorized xy-stage.

During the laser crystallization, the periodically varied thickness locally resulted in non-molten regions deeply introduced into the molten silicon. These solid regions influenced the temperature gradient in the lateral direction perpendicular to the laser scan direction and served as the crystallization centers where the super lateral crystal growth could initially start from (see Fig. 3c-d). Thereby the dominant crystal orientation laterally extends to the grain boundaries, with a possible formation of the intragranular ridges and hillocks described in [16].

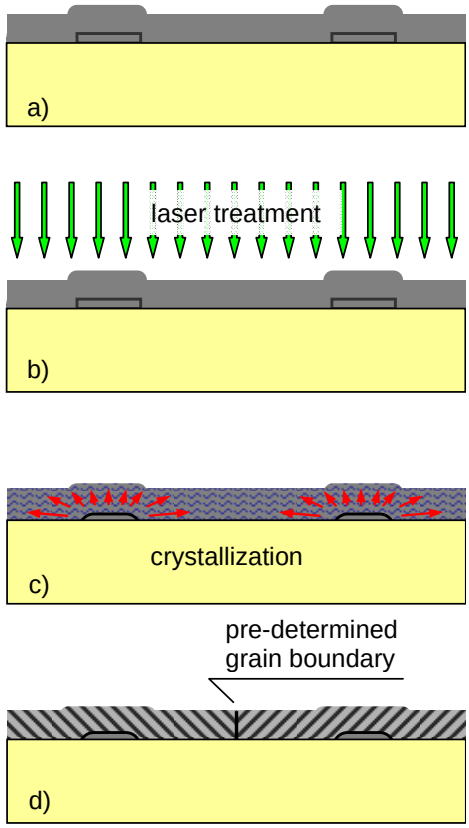

Fig. 3. Crystallization process in silicon film with preformed lines (a) film formation, (b) laser treatment, melting of the silicon film, (c) crystallization process – super lateral growth, (d) finally crystallized film with predefined grain boundaries.

The surface morphology of the silicon films, crystallized with energy densities of 0.6 J/cm^2 and 1 J/cm^2 at a beam overlap of 98%, is shown in Fig. 4a-b. The presence of the laterally grown large grains is confirmed by the micro texture electron backscatter diffraction (EBSD) analysis. Fig. 4 (c-d) shows the inverse pole figure (IPF) maps of the same samples. The grain boundaries in the films crystallized with 0.6 J/cm^2 are oriented mostly parallel to the preformed α-Si lines, *i.e.* in the laser scanning direction, providing a good control over their location (see Fig. 4b and 4d).

The irradiation with lower energies (0.6 J/cm^2 at 98%

overlapping) resulted in partial melting of the film. Therefore, only a part of the film was crystallized, giving the fine-grain structured silicon film (Fig. 4a and 4c).

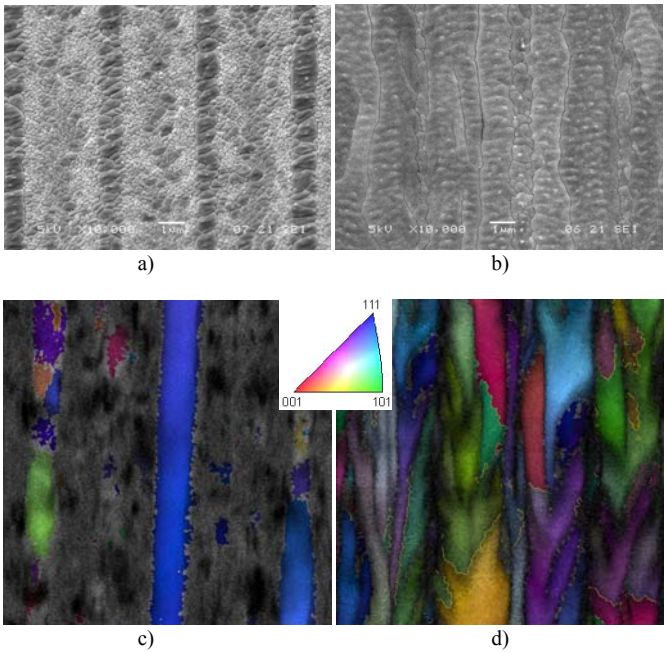

Fig. 4. SEM images and inverse pole figure (IPF) maps of α-Si films crystallized with energy densities 0.6 J/cm^2 (a, c) and 1.0 J/cm^2 (b, d) at 98% laser beam overlapping.

B. Formation of the multilayer structure

A number of multilayer Al/TiN/Al_2O_3/Si-nano-crystals/Al_2O_3/SiO_2/Si(100) structures was realized. For the time being, to exclude the influence of the laser-crystallized silicon films, the multilayer stack was deposited on p-type silicon wafers with (100) orientation.

1) Growing of tunneling oxide

After the standard cleaning procedure, the substrates were oxidized at 800°C in a dry N_2/O_2 ambient during 30 min. This resulted in a 2.6-nm thick SiO_2 layer. The results of this research are reported by us elsewhere [17]. To have the entire low-temperature process flow, this high-temperature step is to be replaced by a low-temperature ICPECVD process, in a later stage.

2) LPCVD of Si-nanocrystals

The deposition of Si requires reactive surface sites. Therefore to achieve the surface termination by OH groups (which is more active as Si-O terminated surface) and to avoid the metal contaminations, the wafers were shortly (around 1 minute) dipped in a solution of 0.3% HF and 0.3% HCl.

Immediately after this dip, the wafers were placed into the loadlock of the cluster system (shown in Fig. 5). Further, the deposition of the functional layer stack (TiN/Al_2O_3/Si-nanocrystals) was done at temperatures ranging from 300 to 425 °C, without vacuum break.

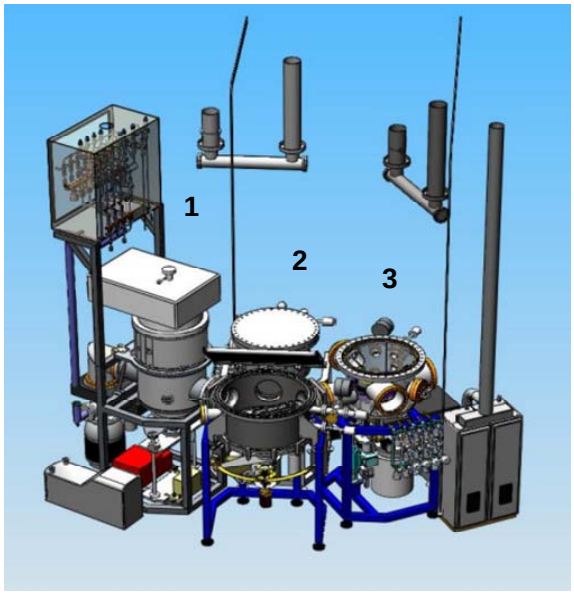

Fig. 5. Cluster System.
Reactor 1: ICPECVD for low-temperature deposition.
Reactor 2: Deposition of metals and silicon in ALD and CVD modes.
Reactor 3: Deposition of high-k dielectrics.

The layer with silicon nanocrystals was formed during LPCVD (in reactor 2) at 325 °C, using disilane (Si_2H_6) or trisilane (Si_3H_8, known as Silcore®) as the source gases. The deposition pressure ranged between 0.1 and 10 mbar. The dramatic increase of silicon nucleation and growth rate, when using Si_3H_8 as a precursor, was reported for deposition temperatures between 410-500 °C [18] and higher. Therefore, we expected to obtain a significantly higher Si-nanocrystal density using Si_3H_8 instead of Si_2H_6 also at low temperatures.

Though the direct surface reactions from Si_2H_6 and Si_3H_8 are limited by rather slow surface dehydrogenation, at sufficient gas pressures the following bimolecular gas-phase reactions sequences can occur [19] during CVD from disilane (1) and from silcore (2):

$$Si_2H_6 + M \Leftrightarrow SiH_4 + SiH_2 + M \Leftrightarrow 2SiH_2 + H_2 + M \quad (1)$$

$$Si_3H_8 + M \Leftrightarrow Si_2H_6 + SiH_2 + M \Leftrightarrow SiH_4 + 2SiH_2 + M \Leftrightarrow 3SiH_2 + H_2 + M\,, \quad (2)$$

where M denotes any other gas molecule.

As a result, highly reactive species such as SiH_2 (i.e., silylene) with a reactive sticking coefficient close to unity are generated [19-22]. These reactive species can react with the surface $[SiH]_s$ sites according to the reaction

$$SiH_2 + [SiH]_s \Rightarrow [Si]_b + [SiH_3]_s \Rightarrow [Si]_b + [SiH]_s + H_2 \quad (3)$$

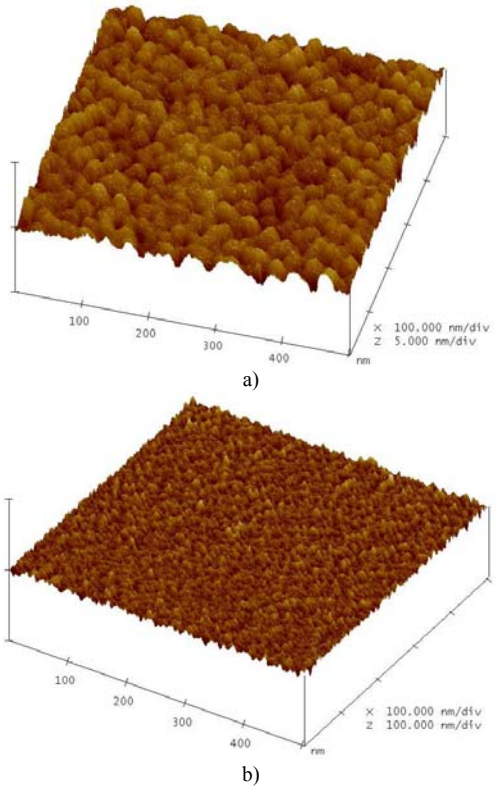

Fig. 6. AFM images of oxidized Si-NC layers deposited at 325°C from disilane at 10 mbar (a) and from trisilane at 1 mbar (b). To enable the observation of the nano-crystals, no upper protection layer was deposited.

The use of trisilane, according to (2), assures a higher concentration of silylene. Due to the very high reactivity of silylene, it is expected that a higher concentration of silylene will result in a higher nucleation rate, providing a higher number of silicon nanocrystals even on a SiO_2 surface. This expectation is confirmed by the AFM measurements (see Fig. 6), where the concentration on nanocrystals deposited from Silcore (~1.9×10^{12} cm^{-2}) is higher in contrast to that deposited from disilane (~0.2×10^{12} cm^{-2}).

3) ALD of Al_2O_3

Directly after the formation of silicon nanocrystals, the wafer was transferred to reactor 3 and covered with an 11.8-nm thick Al_2O_3 layer (blocking oxide) grown by ALD at a temperature of 300 °C. The wafer was consequently exposed to $Al(CH_3)_3$ (Trimethylaluminum, or TMA) and H_2O, with a purge cycle in between [23, 24].

4) ALD of TiN

To prevent both the oxygen and water diffusion into the blocking Al_2O_3 layer, the wafer was transferred to reactor 2, where an 8-nm thick ALD layer of TiN was deposited at 425 °C. The wafer was consequently exposed to $TiCl_4$, followed by the N_2-purge, and to NH_3, followed by the same purge [25, 26].

Finally, the wafer was unloaded from the cluster system and both the front- and back-side metallizations were done by sputtering a 1-µm thick aluminum layer. Circular MOS capacitors were finally realized by patterning the Al and TiN layers. A schematic cross-sectional overview of the realized structure is shown in Fig. 7.

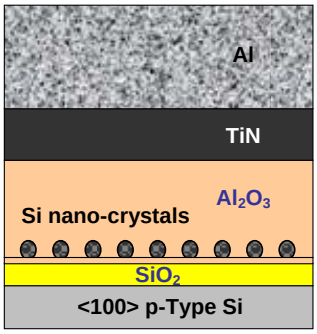

Fig. 7. The schematic cross-section of the multilayer structure with encapsulated silicon nano-crystals.

C. Electrical measurements of the multilayer stack

The encapsulated silicon nanocrystals are expected to act as charge trapping centers. During programming and erasing cycles, due to the different dielectric material of the tunnel and blocking oxides, there is a much higher electric field induced across the thin SiO_2 film. That ensures the Fowler-Nordheim tunneling mechanism to dominate during the charge carrier transport between the substrate and the nanocrystals, and at the same time prevents tunneling through the blocking oxide. As the charge is stored in the nanocrystals, i.e. between the substrate and the control gate, it dramatically influences the C-V characteristics of the MOS capacitors. Fig. 8 shows the typical hysteresis curves observed during the QS-CV measurements of the circular (500 µm in diameter) MOS capacitors with embedded nanocrystals. The width of the hysteresis corresponds to the threshold voltage shift (ΔV_T), which is appropriate for a memory cell.

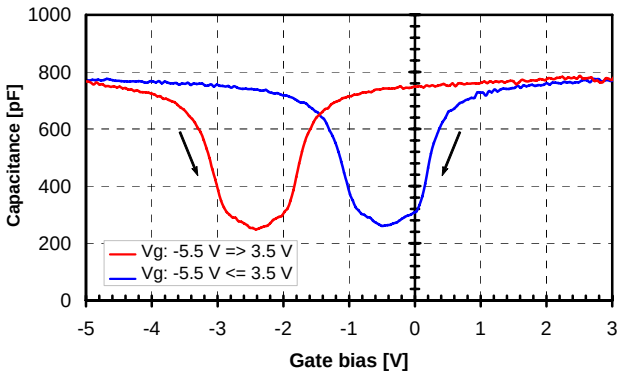

Fig. 8. QS-CV hyteresis curves obtained during programming and erasing cycles for MOS structures with encapsulated silicon nano-crystals. Applied gate-substrate voltages: Vg prog = 3.5 V and Vg erase = -5.5 V.

To characterize the programming and erasing behavior of the MOS capacitors, the endurance (Fig. 9a) and retention (Fig. 9b) tests were carried out. The devices were programmed by biasing the gate at Vg_{prog} = 3.5 V and erased

by biasing the gate at Vg_{erase} = - 5.5 V. Fig. 9a shows a good endurance after 10^5 program/erase cycles, meeting the basic flash memory cell requirement. The realized non-volatile memory cells show a data-retention time longer than 20 hours.

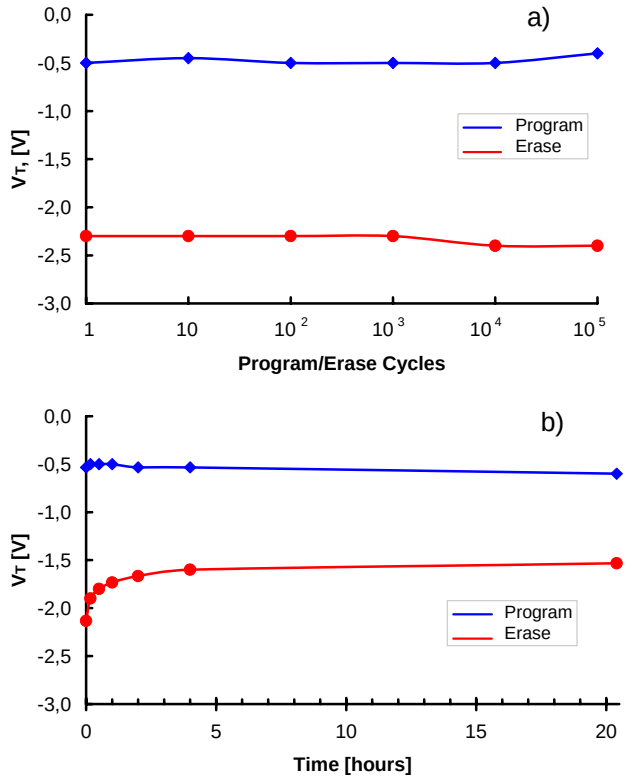

Fig. 9. Endurance (a) and retention (b) measurements of MOS structures with encapsulated silicon nano-crystals.

III. Conclusion

The low-temperature steps (i.e., silicon laser crystallization, CVD and ALD of the functional layers at temperatures below 425 °C) are presented. An increase in the density of silicon nanocrystals deposited using LPCVD with Si_3H_8 (Silcore®) as a precursor gas in comparison to Si_2H_6 is demonstrated. The floating-gate stack module with embedded nano-crystals shows good program and erase behavior, and is suitable for its further integration into low-temperature chip post-processing.

Acknowledgment

This work is supported by the Dutch Technology Foundation (STW). Project number STW-TEL 6358.

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