Test Chip for Detecting Thin Film Cracking Induced by Fast Temperature Cycling and Electromigration in Multilevel Interconnect Systems

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Abstract – Temperature cycling in power IC's is a reliability hazard, even more so when electromigration is playing a role as well. The frequency of the temperature cycling is in the audio domain, which makes it impossible to test in environmental chambers. In the paper, the design and application of a novel test chip to study fast temperature cycling, electromigration and their interaction in multilevel interconnection systems is reported. Incorporated into the test chip are a heating element, a temperature sensor, and extrusion monitors.

Simulation was used to study the initial stress distributions after processing and local temperature distributions in the test chip during the temperature transient. First experimental results have been obtained in the area of fast temperature cycling experiments (by using internal heating only) and electromigration experiments. Failure distributions and failure modes will be discussed. Results indicate that on-chip cycling is a powerful tool to study reliability of power IC's under realistic conditions.

1. Introduction

With decreasing die size and increasing power dissipation, thermal-mechanical and electrical current stresses-induced failures in multilevel interconnects are more likely to become a reliability problem. Temperature cycling was found to be one of the main factors that creates stress cracking in thin films due to the large thermal mismatch among metallic and dielectric materials and the silicon substrate. Predictions of thermal cycling failure rates for integrated circuit (IC) have been widely discussed so far, because the temperature cycling test is extensively used in microelectronic industry to qualify new products [1]. Recent publications have addressed the issue of failures of interconnect system due to temperature cycling [2-6, among others]. It has been shown that temperature cycling can crack the metal films as well as interlayer dielectrics resulting in device failure. For reliability improvements of interconnect systems, the failure mechanism must be understood well enough to create a good failure rate model. However, a very fast thermal transient experiments to mimic temperature cycling in operational conditions cannot be carried out using an environmental chamber. The test condition using the environmental chamber is far from the real operation of IC's working at very high frequency, and possibly masks the failure mechanism more relevant to the field application and may actually prevent detection of failure mechanisms likely occur in application environments. As far as the reliability issue of an interconnect system is concerned, the electromigration problem cannot be neglected, even though the replacement of interconnect material of aluminum for copper which has higher resistance to electromigration will decrease the electromigration problem, one persistent problem remains, namely cracking of interlayer dielectric (ILD) using low-K materials in copper interconnect produced as result of the build-up of electromigration-induced stresses. Furthermore, the coupling of electrical and thermal induced degradation of interconnect systems readily occurs in many applications like for instance power transistors. All results reported on temperature cycling using an environmental chamber. However, experimental data of fast temperature cycling and its coupling with electromigration are still lacking. Therefore, the development of a test chip for studying the fast temperature cycling and a coupling with electromigration experiment is necessary. A clever test structure helps to understand and predict the failure mechanism interconnect systems more realistically.

In this work, a test chip will be presented that can be used to study fast temperature cycling, electromigration and their interaction. The test chip was designed in such a way that resistance change and extrusion can be monitored during the thermal transient stress and the electromigration tests. A reliability testing system for fast temperature cycling using this test chips will be also introduced. The process simulation and device simulation of test chips has been done using commercial software (SILVACO) to get more understanding of the test chip. An initial stress build-up distribution can be obtained after the process simulation. A temperature distribution can be obtained with device simulation, in which a transient current is passed through poly-silicon resistor to be a heat source. The results give an estimation of temperature distribution in the test chip during temperature transients.

2. Experiments and Technique

a) Test chip descriptions

The test chip shown in Figure 3 was designed to include a number of important features. There is a very large 4Ω poly-silicon resistor just below the die surface where a very long meandering metal level 1 (M1) is located. The length and width are about 40000 μm and 3.5μm, respectively. The poly-silicon resistor can be used to generate a high

temperature transient. The temperature can be measured with an integrated diode in the middle of the resistor or with the temperature coefficient of the metal resistor. However, the temperature measurement using a diode is more sensitive than using a resistor. The test line had additional tracks at both sides and a metal level 2 plate covering the whole structure to allow detection of a short circuit due to extrusions. There are 4 point-connectors on a part of the very long meandering metal resistor (about 14Ω) that can be used for standard electromigration testing. The test chip has been processed in a standard two level metallization technology in a bipolar fab.

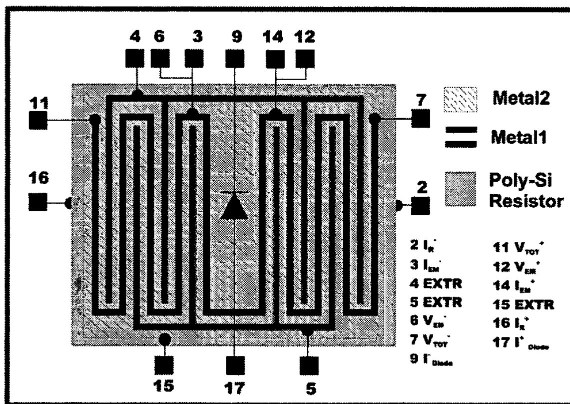


Fig. 1: Test structure on top view with connectors.

b) Experimental set-up

To carry out the fast temperature cycling experiment with the test chip as described above, we engaged a set-up as shown in Figure 2.

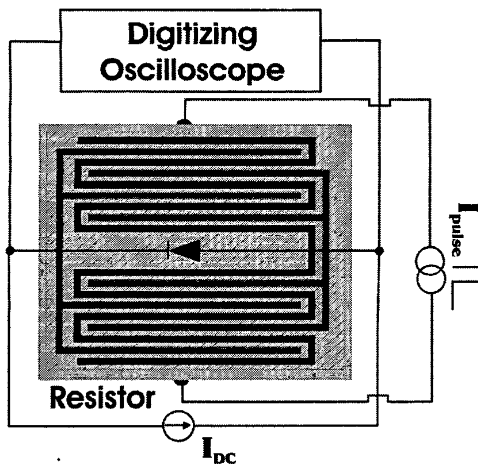


Fig. 2: The scheme for both generating and measuring the temperature cycling with the test chip.

The poly-silicon resistor (heating element) is connected to a pulsed current source. A temperature transient can be generated as the pulsed current is passed through the poly-silicon resistor. More detail about pulsed current source and its functions will be discussed in next section. The integrated diode is connected to a DC current source and a digital oscilloscope. During the temperature cycling, a constant current is passed through the diode. A change of diode voltage is monitored by digitizing oscilloscope, from which the temperature profile can be easily recounted. With this set-up, the temperature cycling experiments can be carried out without using an environmental chamber. The temperature inside the chip can be measured exactly.

c) Reliability testing system descriptions

To carry out a reliability testing with fast temperature cycling using this test chip, a test system shown in Figure 3 was introduced. The test system allows testing with 16 devices in parallel at the same time. The test system consists of four main sections;

- Transient temperature cycling
- Temperature measurement
- Extrusion monitor switching
- Data acquisition system

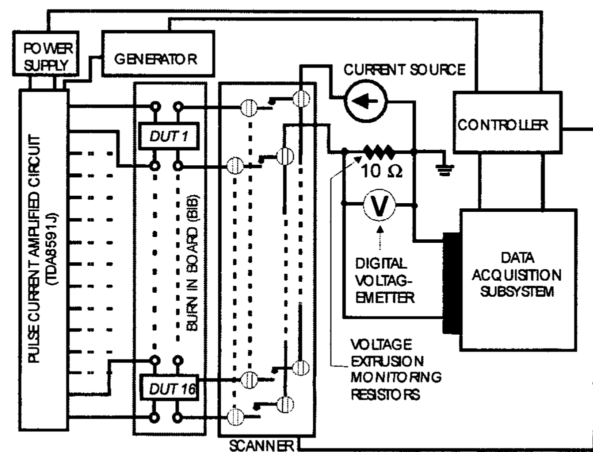


Fig. 3: The reliability test system, only channel 1 and 16 hook-up shown.

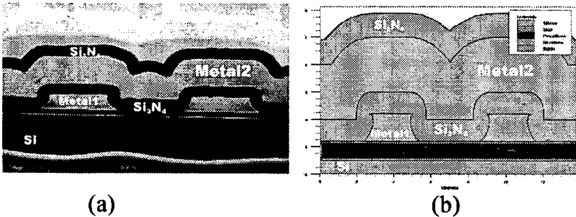
The transient temperature cycling section consists of an amplify circuit designed using a TDA8591J integrated circuit (IC), a generator, and a power supply. Therefore, the pulsed current passed through the poly-silicon resistor to heat up the chip can be varied in frequency and duty cycle by the generator, and its amplitude by the power supply. Consequently, the temperature T_{max}, T_{min}, T_{avg}, ΔT, and frequency can be varied by the power supply and the generator, and many stress conditions can be achieved. In the temperature measurement section, there is a DC current source to pass a constant current through the diode, a digital oscilloscope to monitor the diode voltage change due to the temperature change. The extrusion monitor switching section consists of a DC current source, a digital voltmeter, and a HP 3495A Scanner. The DC current is used to pass a constant current through the metal line, the digital voltmeter

is used to monitor extrusion voltages when extrusion-shorts occurred, and the Scanner is used to switch the connections of current source and digital voltmeter from one device to the others. Consequently, the extrusion can be continuously monitored and recorded. All equipments in this test system were controlled using a computer with a program written in VEETEST version 6.0.

3. Results and Discussion

a) *Test chip with process and device simulations.*

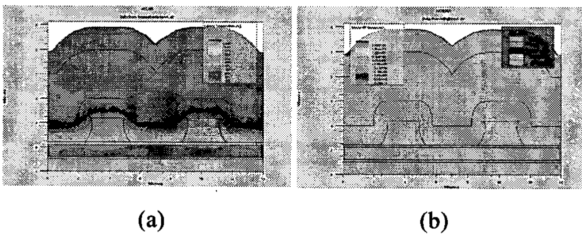
The test structure has been simulated using commercial software for semiconductor process and device simulations (SILVACO). A simulation structure of the test chip has be done using process simulation as shown in Figure 4b, the shape of simulation structure is comparable with cross-section of the test chip shown Figure 4a. The electrical simulation is done with a transient current through the poly-silicon resistor (heating element) for 10ms, and the results of temperature distribution are shown in Figure 5a. It is shown that there is only a slight temperature gradient in the layer and between different layers. The temperature gradient depends on the transient time of current and thermal conductivity of materials.



(a) (b)

Fig. 4: *The cross-section of the test chip by FIB (a), the simulation structure (b).*

The simulation of initial stress build-up in the chip after processing has been done and results are shown in Figure 5b. We found that there are both compressive and a tensile stress present in interlayer dielectric at the corners of metal 1.This may be used to explain the failure mechanism that will be discussed later.



(a) (b)

Fig. 5: *The temperature distribution in the chip with a transient current through the poly-silicon resistor for 10ms (a), the initial stress distribution after chip process (b).*

b) *Fast temperature cycling experiment.*

The first fast temperature cycling experiment has been done with a test condition as shown table I.

This condition can be achieved when a pulsed current with amplitude of 3.5A, duty cycle of 10%, and frequency of 10Hz is forced through the poly-silicon resistor. The temperature generated from the resistor is measured with a DC current of 0.1mA passed through the diode. The diode voltage variation due to temperature cycling was monitored using the digital oscilloscope. An example of the results of diode and resistor voltages is shown in Figure 6.

Table I

T_{min} [°C]	T_{max} [°C]	ΔT [°C]	Period [ms]	Duty Cycle [%]
46	246	200	100	10

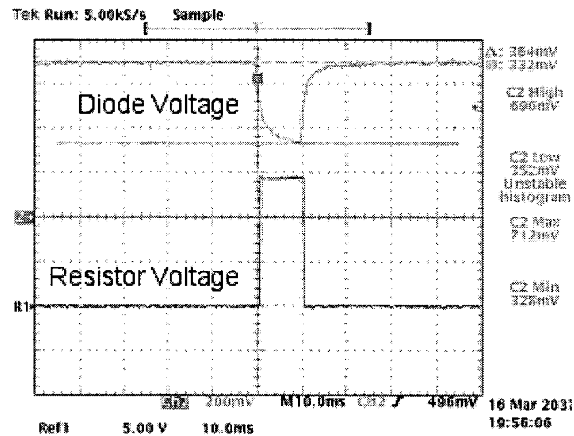


Fig. 6: *The recording of resistor and diode voltages by digitizing oscilloscope.*

A temperature profile can be recounted from diode voltage using the thermal coefficient of the diode (TCD). The TCD can be obtained after some calibration steps of the diode using a highly precise temperature oven, more detail can be found elsewhere [7]. With this test chip, the TCD value of the diode was found out to be about 1.83mV/°C. The temperature profile of this case is shown in Figure 8.

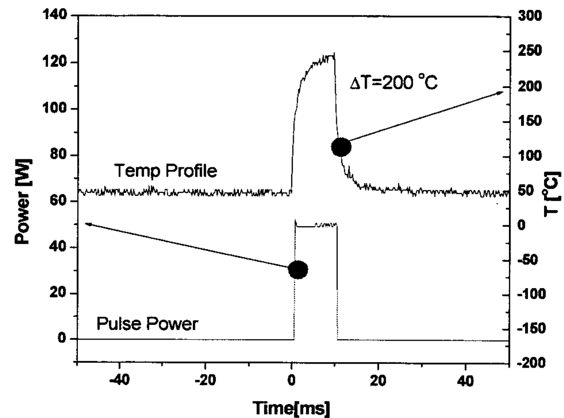


Fig. 7: *The temperature transient in case of temperature range to be about 200 °C.*

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A lifetime test has been done using the reliability test system with this test condition. There are 16 devices that were stressed in this test. The device was considered to have failed when a significant voltage had appeared on any one of the three extrusion monitors. We expect that extrusion failures time would be better fitted with Weibull distribution than lognormal one, because lognormal distributions tend to apply when gradual degradation occurs over time. On the other hand, the Weibull distributions are applicable in case where the weakest link, or the first of many flaws, propagates to failure. The Weibull plot for the results of reliability testing is shown in Figure 9 by using a least square method of fitting a Weibull distribution to time-to-failure data from which the median time to failure, t_{50} and the shape factor, β was respectively found to be ~68 hours and ~1.5. With applying Weibull distribution, the failure rate is calculated by $\lambda(t) = \beta t^{\beta-1}/\alpha^{\beta}$. It showed that the failure rate is increasing in time because the shape parameter value, β is higher than 1.

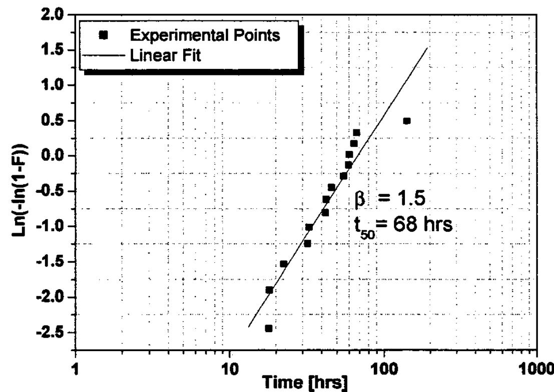
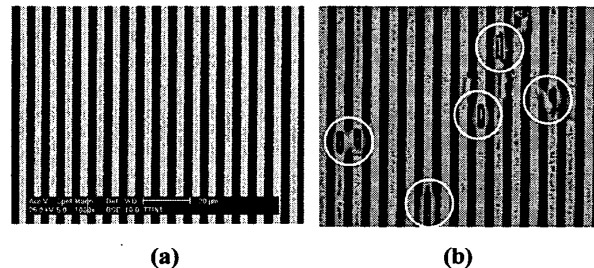


Fig. 8: Weibull failure probability plot for the fast temperature cycling test with temperature range of 200 °C.

The only disadvantage of the measurement set-up is that temperature cycling cannot be carried out with a very high temperature range because the minimum temperature (T_{min}) cannot go down to a below zero value. However, this technique can be carried out with very high frequency so that the number of cycles can be very large in a short time. In addition, it is very easy to record the device failure continuously, while the temperature cycling using the environmental chamber usually record the devices failure at a certain intervals. Consequently, this technique always gets more the cumulative distribution points as compared with the technique using the environmental chamber in a case of the same sample size.

c) Failure analysis

The failed devices were unpackaged, the passivation layer and the top metallization layer (M2) were completely removed. Then the ILD was etched using a plasma etcher with end-point detection. The ILD is etched until 200nm left to avoid the damage of metal line during ILD etching. The surface of M1 is inspected using SEM equipment with a Backscatter Electron (BSE) detector. The BSE detector is used to detect backscattered electrons, which is sensitive to changes in average atomic number. During imaging the light elements will appear as a dark area and heavy elements will appear as a bright area. This means that voids and cracking places will appear dark on the image as shown in figure 9. The electrical measurements have shown that there are also extrusion short between M1 and M2. To understand the failure mechanism, cross-sections have been made by mechanical polishing, and visual inspection by SEM as shown in Figure 10. It showed that the ILD cracking caused the short circuit.



(a) (b)

Fig. 9: The SEM verification of surface of metal level 1; (a) a fresh device; (a) device after stressing.

It has been seen that fast temperature cycling can cause the cracking of thin films in multilevel interconnects and resulted in devices to fail due to extrusion-shorts. The driving force for this cracking is thermal expansion mismatch between silicon substrate and thin films. It has been found that the cracking of ILD readily happens at the top edge cover of the aluminum line (see Figure 10). It may be explained that there are more stresses at the top corner of aluminum line compared the other places after process. As the failure mechanism is not primary purpose of this paper. We will not go into detail here.

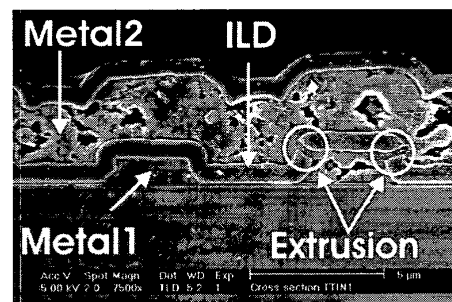


Fig. 10: The cross-session with showing the cracking of interlayer dielectric top edge cover of aluminum.

d) Electromigration tests

As mention above, the test chip can be used for electromigration tests. We have carried out some first electromigration tests with this chip using a commercial equipment for electromigration testing (DESTIN), the tests

are run with current density stress of 2.5 MA/cm², and with two constant temperatures of 125°C and 150°C. During electromigration tests, the resistance of the metal line and extrusion are monitored continuously. The tests were run for 3000 hours. It was found that the devices fail due to extrusion before the resistance of metal line increases. The failure data sets are shown as lognormal distributions (usually used for EM data), from which the t_{50} and σ values may be extracted (see figure 11).

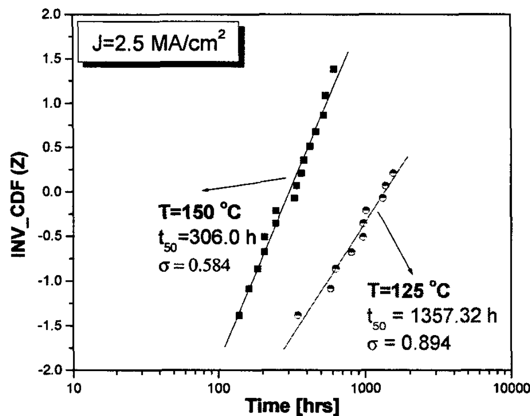


Fig. 11: *Lognormal failure distributions of electromigration experiments. The current stress is 2.5 MA/cm² with two temperatures 150 °C and 125 °C.*

Joule heating of the test chip, as determined using JEDEC Standard JESD33 [8] varied from ~13°C and ~10°C for the current density 2.5MA/cm² and 1.5 MA/cm², respectively.

As mentioned above, the test chip was processed with a standard two level aluminum metallization. An alloy of aluminum with 1% Si and 0.5% Cu has been used. Therefore, which decreasing of resistance of metal line is probably due to the segregation of Cu atoms into Al grain boundary [9]. With this low temperature stress, the decreasing of resistance of metal line would take a long time. In our case, the device failure due to the extrusion-short would be explained that the copper atoms in aluminum-copper films undergoing current stress move faster than aluminum atoms [10]. Consequently, the copper can be mostly accumulated at the anode side and depleted at cathode side [11]. Tensile or compressive stresses at cathodic and anodic ends of the line can cause the extrusion before resistance of metal line increases. However, this is only a rough explanation, a more detail explanation could be done after carrying failure analysis and stress simulation induced by electromigration. This work is in progress.

4. Conclusions and Recommendations

A test chip was designed for fast temperature cycling reliability testing without using the environmental chamber and electromigration testing. The realization and simulation of the test chips are done in parallel. The simulation structure was used to study the initial stress and temperature distribution. A reliability test system was proposed for fast temperature cycling using the test chips. The first result of temperature cycling with delta T of 200 °C and electromigration were successfully done and presented. The test chip is suitable to study two important effects of the multilevel interconnects; electromigration-induced failure accelerated by temperature cycling, and the effect of thermal stress-induced damage on electromigration resistance.

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