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Rise-time effects in ggnMOSt under TLP stress

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Abstract—In this paper the main mechanisms that lead the turn on of the parasitic bipolar transistor of a grounded gate nMOS transistor (ggnMOS) under TLP stress have been analyzed in detail in the sub-nanoseconds range by means of a mixed-mode simulator. We showed that the breakdown voltage of the ggnMOS measured in static conditions would underestimate the maximum voltage across the protection structure obtained by TLP stress, depending on the rise-time of the applied pulse.

I. INTRODUCTION

In CMOS technology the protection against ESD events is usually realized with grounded gate nMOS transistors (ggnMOS) in snapback conduction mode. This mode is reached in this way: when a positive pulse (ESD) is applied to the drain junction (n^+/p substrate), it is forced in reverse biasing until, eventually, it reaches its breakdown. In this condition hole-electron pairs are generated inside the depletion region because of the high value of the electric field: electrons are collected at the drain contact while the holes are collected at the substrate (grounded), increasing its potential with respect to the source junction. When this local potential is high enough to forward biasing the source-substrate junction, electrons are injected from the source to the drain. If this parasitic bipolar structure (Drain=Collector; Substrate=Base; Source=Emitter) has got a forward gain high enough, it can provide its own base current, keeping the structure self-biased. Then, in this condition, the stress current associated to an ESD event is entirely sustained by the parasitic bipolar transistor. The characterizing parameters of this protection structure are:

- V_{T1}, turn-on voltage of the parasitic bipolar transistor associated to the structure;
- $V_{HOLDING}$, corresponding to the minimum clamp voltage across the protection device;
- t_{ON}, switching on time of the protection structure;
- I_{T2}, current at which the protection structure goes in 2nd breakdown ("thermal breakdown") that leads to irreversible damage [1].

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The turn-on voltage V_{T1} is normally identified in the breakdown voltage of the drain/substrate junction and it corresponds to the maximum reachable value, V_{MAX}, across the device to protect before any damage might be caused (for instance, oxide breakdown). It can be obtained by DC characterization or quasi-static measurements like TLP (transmission line pulse) [2]. In TLP a constant high current pulse is forced into the structure under test: with 100 ns. of pulse duration, this test has been proven to be equivalent (i.e., inducing the same kind of failure) to an Human Body Model (HBM) pulse [3], which is the most standardized test for ESD protection structures. The TLP rise-time depends upon the parasitic elements in the measurement set-up and is normally in the order of few nsec. even if it may be much shorter (< 1 nsec.). We investigated on the effects of reducing the rise-time of the TLP on V_{MAX}. As we will show in this paper, this value of V_{MAX} is strongly dependent on the rise-time of the applied TLP, leading to a underestimation of its value in the case of very fast TLM compared with the same value of V_{MAX} obtained by DC characterization.

II. SIMULATIONS

The simulated devices (*Figure 1*) are nMOS with L=0.5μm, W=100μm, lateral bulk contact, medium doped, P-well and t_{OX} =60 nm. The shallow N (n^+) doping profiles are represented by gaussian distributions with x_J =0.1μm.

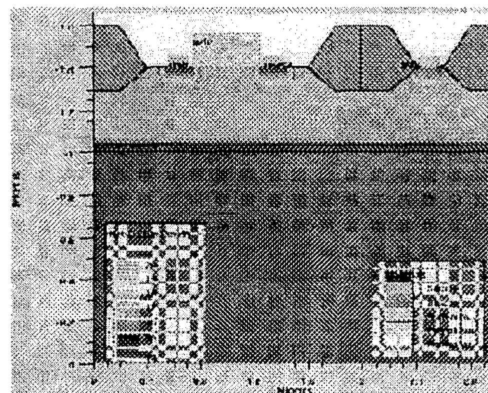

Figure 1: Simulated device.

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On such a device, simulations in transient regime of TL pulses by means of a Mixed-Mode Simulator (circuit + device simulator) implemented in Atlas by Silvaco [4] have been carried out. One of the advantages of such approach consists in setting rise-time pulses experimentally unlikely as order of time (although physically possible) to better understand the physics mechanisms involved.

The simulations have been performed "cold" because from a first non-isothermal approach [5] we obtained a $\Delta T_{LATTICE}$ not larger than 20 °K during the transient that leads to the snapback conduction mode. Therefore, in first approximation, we neglect the thermal production of minority carriers (fundamental mechanism in the neighborhood of the 2nd breakdown [6]).

III. Results and Discussion

By forcing a current pulse of 1.3 A (corresponding to an HBM level of 2KV) with a rise-time of 5 psec., we obtained a behavior of the voltage across the device under study as reported in *Figure 2*.

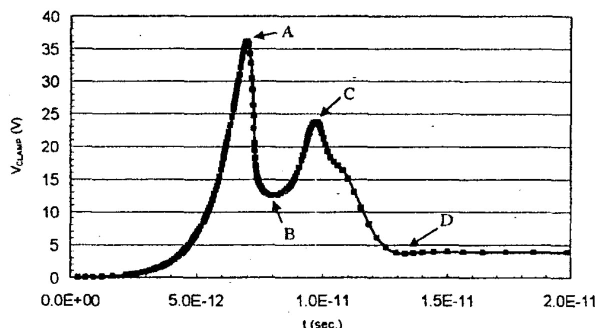

Figure 2: Clamping voltage of the device submitted to a current pulse of 1.3 A with a 5 psec. rise-time.

As it is possible to notice there are two peaks and one minimum before reaching the holding voltage, whose value corresponds to that calculated from the simulation of DC breakdown characteristic (*Figure 3*).

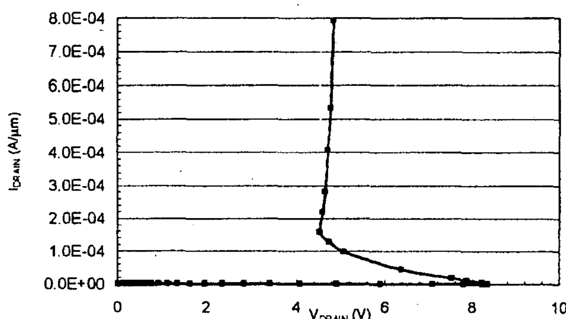

Figure 3: Simulated breakdown characteristic in DC conditions of the device in *Figure 1*.

Notice that the peak voltage exceeds that of static breakdown of the Drain/Substrate junction, considered as the maximum value across the protected device. As it is possible to note there are 4 particular interesting points (marked as A, B, C and D) before the device reaches the holding voltage condition. In *Figure 4* the evolution of the electric field along a cross section through the channel is shown for the above mentioned points.

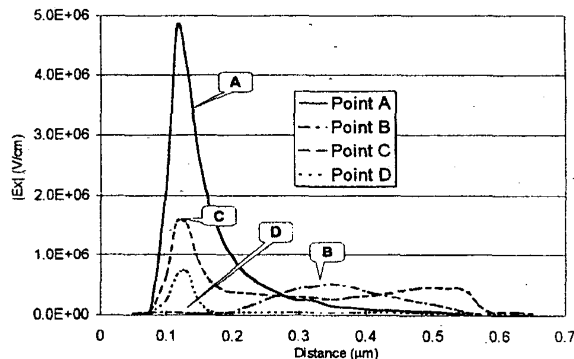

Figure 4: Simulated electric field from the drain junction to the source

From t=0 to $t=t_A$ there is a current of holes displaced for capacitative effect (dV/dt) that loads the overlap capacitance (*Figure 5*) leading a very high electric field in that region. Notice that even before reaching the point A, the electric field might be strong enough to activate impact ionization so as it increases the efficiency of the process.

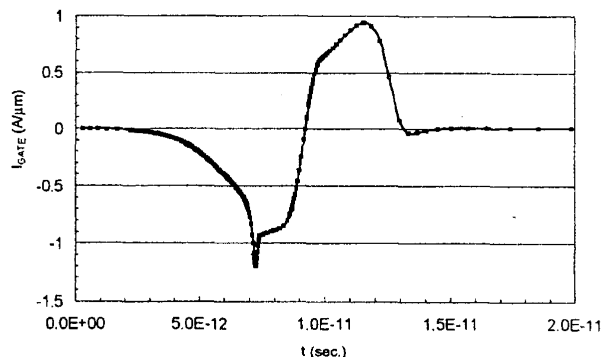

Figure 5: Gate current of the simulated device in *Figure 1*.

Between $t=t_A$ and $t=t_B$ the flow of holes current in the source direction takes place, reducing the electric field. Between $t=t_B$ and $t=t_C$ the holes current starts to be enough near to the source junction to bias the substrate (base) compared to the source (emitter) and, therefore, increasing the electric field. In $t=t_C$ the source/substrate junction (base/emitter) is forward biased and it starts to inject

electrons in the substrate in the direction of the drain. When these electrons reach the drain junction, the parasitic bipolar is virtually switched on (holding voltage). This last mechanism is confirmed from the increase of the time necessary to reach the holding voltage increasing the gate length (increase of the average base transit time, [7], (*Figure 6*).

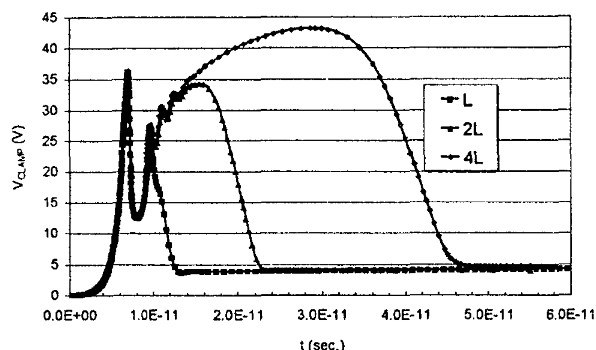

Figure 6: Clamping voltage as function of gate length.

As a confirmation that the main mechanism in the transient behavior is the holes injection for capacitative effect, we noticed that the voltage across the device does not vary significantly with the amplitude of the stress applied (*Figure 7*).

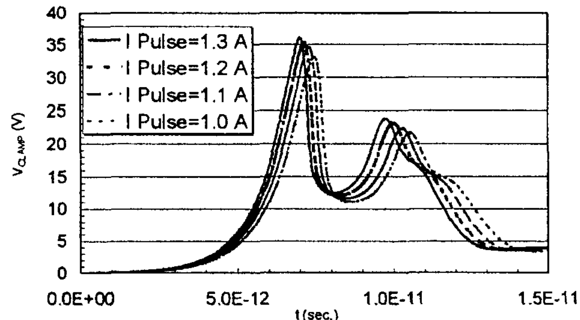

Figure 7: Clamping voltage as function of pulse amplitude.

Another fact confirming the previous hypothesis is the behavior of the maximum voltage across the device as a function of the rise-time of the applied pulse *(Figure 8)*. Note that when the rise-time corresponds to 5 nsec. (i.e., in the range of the nominal TLP test), the maximum voltage is exactly corresponding to the one obtained from the static DC characteristic.

IV. Conclusions

We showed how during the switching on time of the parasitic bipolar transistor it is possible to reach voltages even exceeding the breakdown voltage of the drain/substrate junction measured in DC conditions. This phenomenon has been explained to be caused by the loading of the overlap capacitance with holes displaced by capacitative effect (dV/dt). This is also confirmed by the dependence of the maximum reached voltage on the rise-time of the applied pulse.

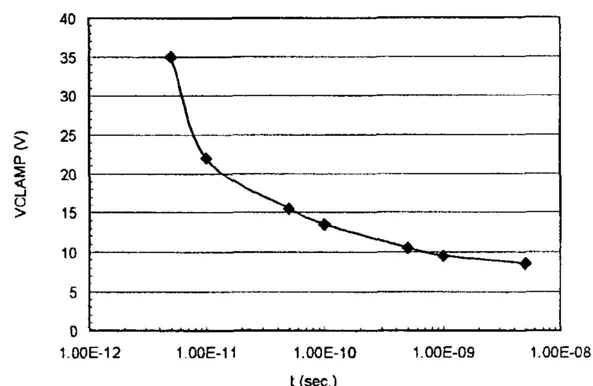

Figure 8: Maximum voltage across the protection device as function of the rise-time for the applied pulse.

V. References

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