Practical Implementation of Defect-Oriented Testing for a Mixed-Signal Class-D Amplifier

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Abstract

This paper describes the flow of defect-oriented testing from beginning to end, based on the industrial test development for a commercial mixed-signal class-D amplifier. A software tool called DOTSS (Defect-Oriented Test Simulation System) was used to perform the fault simulations. The greatest benefit of using defect-oriented testing turns out to be that it gives more insight in the underlying fault mechanisms. This information can be used to generate complementary tests or to take design-for-testability measures to achieve a high fault coverage.

1. Introduction

The class-D amplifier is basically a pulse-width modulation amplifier [1,2]. Compared to other classes of audio amplifiers, the class-D amplifier has the advantage of high output power to power dissipation ratio. This feature makes it very suitable for auto-mobile and portable applications, where a minimum heat generation during operation and long battery life are some of the key performance indicators for high power audio ICs.

Traditionally, analog audio amplifiers are specified and tested on their delivered output power at a given maximum THD (total harmonic distortion). When operating at a supply voltage of +/- 30 V, the amplifier can generate a maximum output power of more than a hundred Watt. This fact leads to a great difficulty in testing this IC according to the specifications in the traditional way. Since in an industrial test environment, the test engineer has to deal with a physical distance between the DUT and the nearest decoupling capacitor. This distance can be several centimeters and causes a parasitic inductance of tens of nano-Henries. This inductance, combined with the high test frequency of about 500 kHz and the low resistive load, causes a huge voltage swing at the supply pins of the IC. This voltage swing not only makes it impossible to measure the THD, but it also creates a very high probability of causing serious damage to the IC. Now the question is: in what alternative way can the IC quality be guaranteed without performing the standard THD test ?

In the past few years, a new test method, the Defect-Oriented Testing (DOT) approach, has emerged for testing mixed-signal ICs [3-5]. Experimental investigations have been carried out on several commercial ICs to verify its industrial applicability [6-11]. Previous investigations showed, that if an IC has a good design-process fit and it is fabricated in a stable process, defects are the major root cause for yield loss and customer rejects [12]. With the defect-oriented testing approach, simple tests can be generated, complementary to the functional tests, to achieve a high defect coverage [8,11].

This paper presents the investigation results and the application of the defect-oriented testing approach on a mixed-signal class-D amplifier. Fault coverage of functional tests will be evaluated. It will be shown that with the defect-oriented testing approach for industrial test development, significant insight in the fault mechanisms in a particular circuit and production process can be gained. Based on the obtained information, dedicated tests can be generated and additional design-for-testability (DFT) measures can be taken to achieve a high fault coverage. Test development with defect-oriented testing will be described for the class-D amplifier step by step. This paper is organized as follows. After the introduction in the first section, the defect-oriented test development flow is described in section 2. To facilitate the fault simulation process, techniques such as behavioral modeling and mixed-signal fault simulation have been carried out, these will be described in section 3. Fault simulation results of functional tests and failure mechanisms of difficult-to-detect faults are evaluated and analyzed in section 4. Finally, conclusions will be drawn in section 5.

2. The Defect-Oriented Test Development Flow

2.1. Deterministic fault extraction

The flow of defect oriented test development starts with the determination of possible defects in the layout. In this case, only the catastrophic faults are examined, as the parametric variations are well under control during the fabrication process and can be considered to be within the preset limits. The design is assumed to be correct and developed within the borders of tolerance.

There are several methods for fault-extraction. One way to approach fault-extraction is based on the Monte Carlo method. In this method, random defects are sprinkled over the layout first. Their number varies from a few thousand to several millions. These defects can be divided into a number of groups and the amount of defects fitting into one group determines the chance a certain type of faults occurs. A fault simulator working by this principle is VLASIC [13]. A drawback of this random-sprinkle method is that it is quite CPU intensive [14].

Another approach which leads to the same results is based on the critical area principle [15,16]. By using this method, the probability of a certain defect to occur is calculated deterministically. The critical area is defined as the layout area that is susceptible to defects. If the central point of a particle lies in this area, the defect will cause a fault in the circuit. See Figure 1.

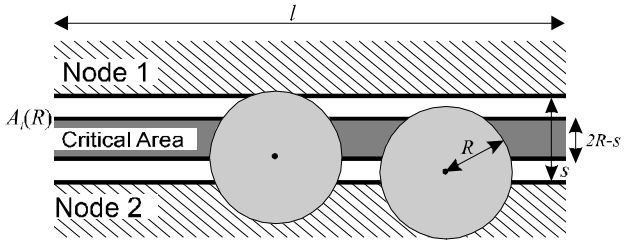

Figure 1. Fault critical area regions

The probability a given fault F_i occurs, $P(F_i)$, can be described by [17]:

$$P(F_i) = D_i \int_0^\infty A_i(R) f(R) dR \qquad (1)$$

where D_i is the spatial density of defects and assumed to be a constant. $A_i(R)$ is the critical area, which can be calculated for the example in Figure 1 as:

$$A_i(R) = \begin{cases} l \cdot (2R - s) & \text{for } 2R > s \\ 0 & \text{for } 2R \le s \end{cases} \qquad (2)$$

An important parameter in this method is the distribution of the size of the particles, $f(R)$. This distribution is shown in Figure 2. Assumed that the value of x_0 is much smaller than the minimum particle size that can cause a failure, the distribution can be described by the following equation [18] :

$$f(R) = \frac{2(p-1)x_0^{(p-1)}}{(p+1)R^p} \qquad \text{for } R \ge x_0 \qquad (3)$$

in which p is a process-dependent constant. In VLASIC, $p=3$ is used. Recent publications [16-18] use $p=4$. Data from two IC waferfabs showed a particle distribution as outlined in Figure 2. Each action in the fabrication process that adds dust-particles shows up as a peak in the curve. At the end of the process, the mean particle size is equivalent to the average of the added faults. This line approximates the linear-power law distribution for the value of $p=3$. With the use of equation (1) to (3), the probability of fault F_i can be calculated:

$$P(F_i) = 2D_i x_0^2 \frac{l}{s} \qquad (4)$$

where l is the length and s is the separation of two nets in parallel. Equation (4) differs from that described in [17], because in this case $p=3$ was used instead of $p=4$. As only the mutual proportions of the faults are of interest, a few constants can be left out, which results in the final equation:

$$P(F_i) \sim \frac{l}{s} \qquad (5)$$

Besides the intralayer defects, interlayer defects exist. These faults can be determined easily by the size of the area of two overlapping layers. To obtain a realistic distribution between vertical and horizontal bridges, the weights of the vertical bridges should be multiplied by a constant, before they are added to the horizontal bridges. Unfortunately, no fixed value can be given for this constant, as it is heavily dependent on the process. Values between 0 and 0.1 are being used in practice. Finally, all possible faults between two nets are being added and saved as the probability a fault occurs between those two nets.

These extraction algorithms can easily be implemented in a Design Rule Check (DRC) of the design-environment by using equation (5). For this purpose, the same functions can be used as for the extraction of parasitic capacities. With these functions, both length and separation of two different nets can be measured. With this simple method an inaccuracy arises if two nets are not exactly parallel, but for example with an angle of 45°. Experiments showed that ignorance of such extremities of nets gave rise to deviations smaller than 1% in the extracted faults for analog ICs. For the extraction, a maximum size for the particle is stated. If the particle would exceed this size, it would be big enough to destroy total parts of the chip. Therefore, particles bigger than the maximum size are ignored during the fault-extraction. A size of ten times the

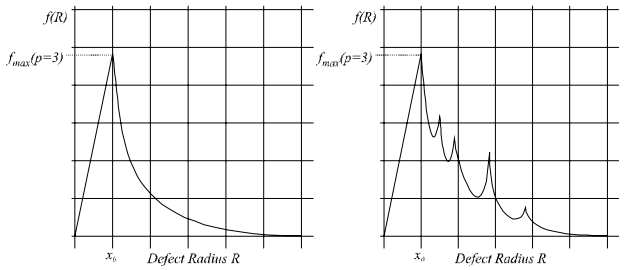

Figure 2. Defect size distribution: theoretical and waferfab data

minimal design distance has experimentally been proven to be a good rule of thumb.

This extraction method is simple and works well for analog and mixed-signal ICs. Extraction never takes longer than several minutes. When the extracted layout has been generated, it is easy to make a raw netlist, in which the faults and their weights are listed as parasitic capacities and their values. A short shell script generates a list with faults and the real circuit netlist from the raw netlist.

2.2. Fault selection

The extraction process generates a number of faults that varies between some tens to many of thousands. The maximum amount which can be simulated is dependent on the available CPU-power and time. In practice the amount of available CPU-power is restricted, so a trade-off has to be made between the duration of the fault simulation and the number of faults.

The faults are sorted on their probability of appearance, in other words on their weight. Then, a percentage of weighed faults, an area-size under the curve as shown in Figure 3, is chosen for the fault simulation. In this figure for example, the line of 70% of the weighed faults has been drawn. To simulate a 100% would take too long, therefore a balance has to be made between accuracy and available time. It is difficult to decide how many faults should be simulated to obtain a reliable result. Previous experiments within Philips

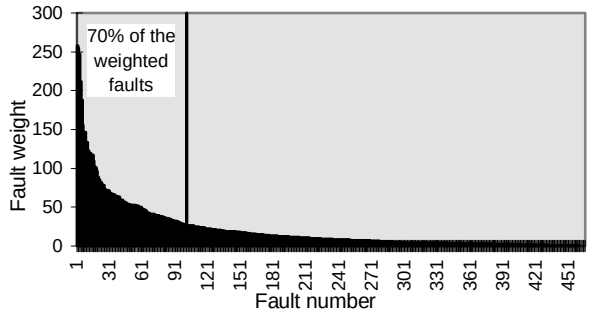

Figure 3 Weighed faults of the VICONVERTER

Semiconductors showed that a minimum of 70% of the weighed faults should be simulated, with a minimum number of 75 faults. This gives a deviation of less than one percent from the value obtained with a full fault set simulation.

Another method often used for CPU time reduction is the divide-and-conquer method. If the design is hierarchical, macro cells can be used and analyzed separately. But by doing so, a part of the interconnect is omitted. And it is the interconnect that contributes most to the fault weights. Therefore it is more correct to take a large part of, or even the complete design, and remove all of the macro-cells except the one that will be simulated. The interconnect is left in the lay-out. In this way, the macro-cells can be simulated one by one within their surrounding interconnect.

2.3. Transistor-level fault simulation

A tool called DOTSS (Defect Oriented Test Simulation System), developed by Philips ED&T, is used for fault simulation. The task of the fault simulator is to sequentially inject each fault from the fault list into the circuit. The circuit with the injected fault is passed to the circuit simulator. In addition to the netlist and the faultlist, the user has to provide a test bench, test stimuli and test limits. The test bench for DOTSS is a simplified description of the tester hardware.

The results of the simulation are stored in a database and will be compared to the results of the defect free (golden) circuit simulation. After the simulation has been run, the user can compose a test set out of the simulated tests. DOTSS automatically performs an optimization and shows the fault coverage of the selected tests as well as of the redundant ones. At this moment, DOTSS can only handle shorts, which are in majority in most processes [19]. The short is modeled by a resistor of which the value can be freely chosen.

To analyze the actual distribution of resistance values of defects, the production defects of a CMOS process have been monitored [20]. The results of this investigation are summarized in Table 1. Although this research has been done on a digital CMOS process, it gives a good impression of the distribution in other processes.

Table 1. Resistance of the shorts

Bridging defect resistance	Portion of bridges
$Rb \leq 0.5\ k\Omega$	69.3 %
$Rb \leq 1\ k\Omega$	95.7 %
$Rb \leq 5\ k\Omega$	98.3 %
$Rb \leq 10\ k\Omega$	99.1 %
$Rb \leq 20\ k\Omega$	100 %

The median value is reached at a resistance value of 200 Ohm, therefore this value was chosen for the fault simulations. It seems not to be very realistic to model a short only at one resistor value. To determine the influence of this value on the final fault coverage, an experiment has been performed with one circuit block of the class-D amplifier. A full set of 469 faults has been simulated twice. First, the circuit was simulated with the faults being modeled by resistors of 200 Ohm. Second, the faults were modeled by 20 Ohm and after that by 2000 Ohm, the average of the outcomes of this second simulations was taken as total fault-coverage of these two modelations. The fault-coverage of the last simulation was less than 0.1% lower than of the first one, but the simulation-time doubled. In a more complex (sub)circuit, simulating so many faults is out of the question, because of the limiting factor of time. Therefore, simulating every fault by two different resistive values would not be worth-while.

Two important input files for DOTSS are the test limits and the input stimuli. Before the testing is started, a good consideration of which tests should be part of the test set is necessary. Leaving a performed test out of the results is easy. But to add a test means all simulations have to be repeated, which takes a lot of time. Good knowledge of the design is indispensable by setting up the test stimuli. The help of the designer is important and can save time, and in addition it stimulates the DFT process.

The effectiveness of a test largely depends on its limits. These limits have to be wide enough to cover the parametric dispersion of the process, but at the same time, they have to be narrow enough to come up to the specifications of the IC. A good way to determine the process tolerance is to perform a Monte Carlo analysis. This is however very CPU intensive and can therefore often hardly be combined with the fault simulation, which does also take a large amount of CPU power. A good alternative is a process tolerance study of parameters effecting a certain test. Again, the designer can be a good help, as he designed the circuit considering the tolerances. If the IC is already in production, the determined test limits can be compared with data logs of the real tests.

3. The Class-D amplifier

3.1. Circuit description

As mentioned before, the class-D amplifier is basically a pulse-width modulation amplifier. In the application, the amplifier is followed by a second order low-pass demodulation filter. A block schematic of the signal path is given in Figure 4. The pulse-width modulation is realized in a feedback loop. The audio signal is buffered in a VI-converter and fed to the loop, which consists of two integrators, a feedback resistor and the POWERPATH. The POWERPATH is basically a comparator which controls two POWERSWITCHES. It is mainly digital and the logic has an equivalent of about 80 gates. The complete design consists of two identical signal paths, a control manager, a clock, voltage and current sources, and protection circuits. The two signal paths cover 95% of the total chip area.

This amplifier has been designed in a new high-voltage BiCMOS/DMOS process and has a symmetric power supply of +/- 30 Volt. It can deliver its power through a demodulation filter to a 8Ω load, configured in Single-Ended or Bridge Tied Load (BTL) mode, whereby the maximum power is 190 Watt. The internal clock and thus the modulation frequency is 500kHz. One of the biggest problems during industrial testing is the stabilization of the power supplies. To make sure the power supply will not swing up too high, a decoupling

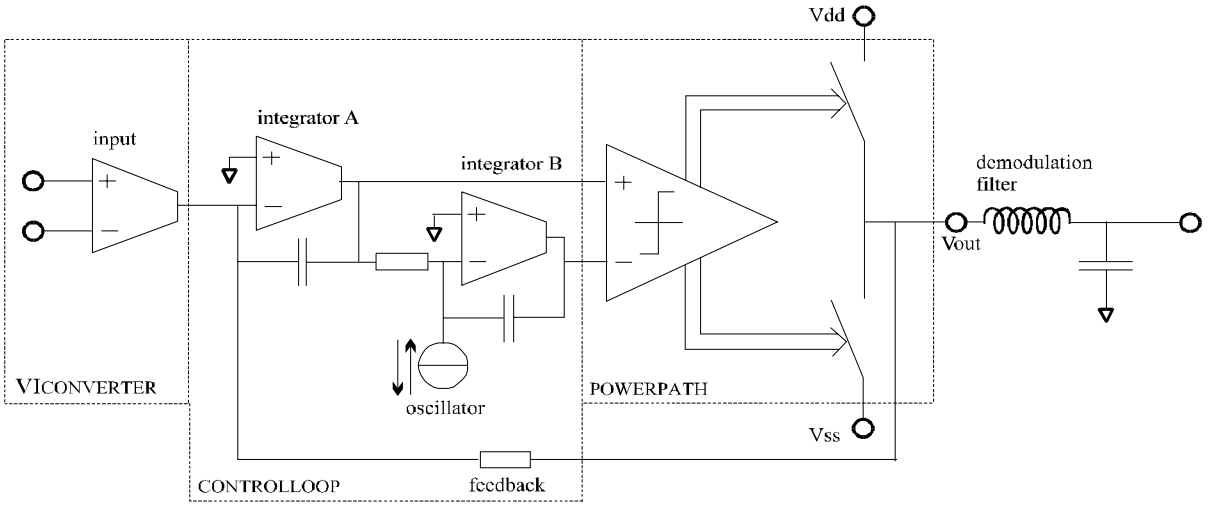

Figure 4 Block schematic of the signal path of the class-D amplifier [2]

capacitor has to be soldered almost directly between the supply pins. During industrial testing with default load, the parasitic inductance in the wires between the supply pins and the decoupling capacitor causes a huge voltage swing, big enough to kill the amplifier. This has a direct impact on the way of testing. Standard functional amplifier tests like distortion and power can not be executed. Because of this, a quest to alternative test methods was started.

3.2. Fault simulation

Since the class-D amplifier is a mixed-signal IC, fault simulation is quite time-consuming. To investigate this, a general attempt was made just to start a simulation run and look how much could be done in some amount of time. The attempt existed of simulating the complete signal path for three periods of a 10kHz sinus. After 15 hours the simulation was stopped. Only two periods of the sinus were done. Extrapolation of these data results in a simulation time of 22½ hours. This means, the simulation of for example 200 faults will take over 6 months. After the analysis of the problems, three areas capable of improvement were found:

- The circuit should be broken down into smaller blocks
- A mixed-signal simulator should be used, or an analog simulator with behaviour models
- A straightforward transient analysis should be avoided by choosing the stimuli in a smart way

Good examples of mixed signal fault simulation can be found in [21]. For the simulation of the class-D amplifier, all three methods were used. The amplifier was divided into three parts, which have been simulated seperatly.

4. Results

First, the class-D amplifier was simulated with the standard functional test set for class-AB amplifiers, without the power and distortion tests. This was done to make a comparison with the new test set possible, and to gain insight in the fault coverage of the specification-oriented test set. This test set was then used as a basis for the further development. Because the power tests could not be performed during industrial testing, a substitute for these tests to guarantee the power performance was anyhow required. The results of the specification-oriented tests are shown in the second column in Table 2. The total chip area in the table is 95.4%, because only the blocks in the signal path were simulated.

Results of the fault simulation with the specification-oriented test set show that some tests were redundant. An example of such a test is the DC gain. Faults covered by this test are already found by the off-set and the maximum input level tests. These two tests are anyhow part of the test set, because they cover faults not covered by other tests.

Some parts of the chip needed more attention. This could be seen by investigating the undetected faults. The most important undetected faults were traced back to the schematics. For these faults, additional tests were developed. A good example can be given for the controlloop. Only a step response at the clock pin was added, which is quite a simple test. The addition of this single test resulted in a significantly higher fault coverage, as can be seen in Table 2.

Not for all the important defects an additional test could be defined, sometimes a change in the design was necessary. An example of such a fault is a short in the driver for the powerswitch. These drivers, implemented as an inverter, are very strong. They can easily handle the extra resistance of 200 Ohm, injected by the fault simulator. However, such a fault could give reliability problems in the application, therefore fault detection is desirable. The most efficient way to solve this problem is to use IDDQ testing for the drivers. A design change was needed to make this possible. Results from the simulation justified the realization of this design change.

Fault simulations with the defect-oriented test set are shown in the third column of Table 2. For this test set, redundant tests were left out and complementary tests were added. A substitute for the power tests was also found and implemented. A design change was realized to make IDDQ testing possible. As can be seen, the fault

Table 2. Fault coverage with different test sets

Block name	FC functional	FC with DOT	% chip area
VICONVERTER	93.1 %	93.1 %	4.5 %
CONTROLLOOP	83.3 %	89.0 %	19.1 %
POWERPATH (excl. switches)	72.6 %	90.5 %	9.1 %
POWERSWITCHES (incl. drivers)	94.0 %	100 %	62.7 %
Total	89.8 %*	96.6 %*	95.4 %

* Total FC is the weighed FC over the 95.4% of the chip area

coverage shows a significant rise.

For the VIconverter, the test set has not been changed. This block only covers a small part of the total chip area, and the fault coverage was already high. Furthermore this block is embedded in the design, so obtaining an even higher fault coverage is very difficult. For the controlloop, only one simple test was added which resulted in an increase of the fault coverage. The fault coverage of the powerswitches and their drivers is very important, because they cover almost 2/3 of the chip area. After the implementation of IDDQ tests, a fault coverage of 100% could be reached.

5. Conclusions

Now that the test development flow with DOT has been explained and put into practice, an evaluation of this testing method can be made. Though it is not commonly used in practice yet, it turned out to be a very manageable way of fault simulation for this class-D amplifier. Fault-extraction from the layout can easily be implemented in the design-environment. As long as the simulation process is executed well-considered, simulation time can be kept within acceptable limits.

What is most valuable about DOT is that it gives a good insight in the underlying defect mechanisms. Based on this information, the test set can be extended on reasonable grounds wherever necessary. Also, design-for-testability measures can be taken. These adjustments can result in a significant increase of the fault-coverage, as has been shown with the case study of a new commercial class-D amplifier. Although distortion and power tests could not be performed on this IC, by means of DOT an alternative test set could be developed to guarantee the quality of the amplifier.

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References

[1] K. Nielsen, “High-Fidelity PWM-Based Amplifier Concept for Active Loudspeaker Systems with Very Low energy Consumption,” J. Audio Eng. Soc. (Papers), vol. 45, pp. 554-570, 1997 July/August.

[2] J.D. Sherman, "Class D amplifiers provide high efficiency for audio systems," EDN, pp. 103-110, May 25, 1995.

[3] M. Soma, “Fault modeling and test generation for sample and hold circuits,” Int. Symposium on circuits and Systems, pp. 2072-2075, 1991.

[4] M. Soma, “An experimental approach to analog fault models,” Custom Integrated Circuits Conference, pp. 13.6.1-13.6.4, 1991.

[5] A. Meixner and W. Maly, “Fault modeling for the testing of mixed integrated circuits,” Proc. of Int. Test Conference, pp. 564-572, 1991.

[6] M. Sachdev, “A realistic defect oriented testability methodology for analog circuits,” J. of Electronic Testing, Theory and Applications, pp. 265-276, 1995.

[7] M. Sachdev, “Catastrophic defect oriented testability analysis of a Class AB Amplifier,” Proc. of Defect and Fault tolerance in VLSI Systems, pp. 319-326, 1993.

[8] M. Sachdev, “Defect oriented analog testing: strengths and weakness,” Proc. of 20th European Solid State Circuits Conference, pp. 224-227, 1994.

[9] M. Sachdev and B. Atzema, “Industrial relevance of analog IFA: a fact or a fiction,” Proc. of Int. Test Conference, pp. 61-70, 1995.

[10] B. Atzema and T. Zwemstra, “Exploit analog IFA to improve specification based tests,” European Design Automation and Test Conf., pp. 312-320, 1995.

[11] Y. Xing, “Defect-Oriented Testing of Mixed-Signal ICs: Some Industrial Experience,” Proc. of Int. Test Conference, pp. 678-687, 1998.

[12] J. van der Pol, F.G. Kuper and E.R. Ooms, “Relation between yield and reliability of integrated circuits and application to failure rate assessment and reduction in the one digit FIT and PPM reliability era,” Microelectron. Reliab., Vol. 36, no.11/12, pp. 1603-1611, 1996.

[13] H. Walker and S.W. Director, “VLASIC: A catastrophic fault yield simulator for integrated circuits,” IEEE Trans. on CAD of Integrated Circuits and Systems, Vol.5, pp. 541-556, 1986.

[14] G.A. Allan and A.J. Walton, “Efficient Critical Area Measurements of IC Layout Applied to Quality and Reliability Enhancement,” Microelectronics Reliability, Vol. 37, No. 12, pp. 1825-1833, 1997.

[15] José Pineda de Gyvez, “IC defect sensitivity”, Ph.D. Thesis, University of Eindhoven, the Netherlands, 1991.

[16] F.M. Gonçalves, I.C. Teixeira, J.P. Teixeira, “Realistic Fault Extraction for High-Quality Design and Test of VLSI Systems,” IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems, pp. 29-37, 1997.

[17] F.M. Gonçalves, I.C. Teixeira, J.P. Teixeira, “Integrated Approach for Circuit and Fault Extraction of VLSI Circuits,” IEEE Int. Symp. on Defect and Fault Tolerance in VLSI Systems, pp. 96-104, 1996.

[18] T. Zanon, “CODEF 1.1: Contamination-Defect-Fault-Simulator for 0.5 μm CMOS Technology,” Msc. Thesis, Technische Universität München, November 1996.

[19] R.C. Aitken, “A comparison of defect models for fault location with IDDQ measurements,” Proc. of Int. Test Conference, pp.1051-1060, 1993.

[20] R. Rodriguez-Montanes, E.M.J.G. Bruls, and J. Figueras, “Bridging defects resistance measurements in a CMOS process,” Proc. of Int. Test Conference, pp.892-899, 1992.

[21] R.G.J. Arendsen, “Defect based test selection for large mixed-signal circuits,” Ph.D. Thesis, University of Twente, the Netherlands, April 1997.