SYSTEMATIC GENERATION OF TRANSCONDUCTANCE BASED VARIABLE GAIN AMPLIFIER TOPOLOGIES

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ABSTRACT

A systematic method for the generation of variable gain amplifier topologies is proposed. The generation is based on voltage controlled current sources (VCCSs) modelling saturated MOS transistors, resistors or combinations of these elements. It is shown that many alternative circuit topologies can be generated, that would not easily have been found in an intuitive way. Simulation results shown that significant differences in performance occur, with various mixes of specific strong and weak points. The set of alternative topologies can be used as a circuit topology database for analogue CAD systems.

1. INTRODUCTION

Transistor level analogue circuit design is still largely done by human designers. Although numerical circuit simulation tools are routinely used, and tools for circuit optimisation and symbolic analysis are becoming accepted, these tools mainly aid in the analysis and optimisation of a given circuit topology. The choice of the circuit topology, i.e. the set of components and their interconnection, is still mainly done by designers. Although some CAD frameworks with topology selection exist [1,2], these only cover a very limited set of topologies.

Topological circuit design is difficult due to the huge amount of different possible circuit topologies. Using graph theory it can be shown that hundreds of different circuits are already possible with a handful of components. To cope with this complexity, designers use their experience to select one or few promising circuit topologies for further analysis [3]. However, the risk of overlooking interesting design options is high. As a result, the quality of a design is very dependent on the experience of the designer and can be far from optimal. Moreover, if a selected circuit fails to satisfy the specifications, it is not obvious how to find alternative circuits. It is concluded that a more systematic method for circuit topology synthesis is desirable.

Systematic circuit topology generation for circuits with transconductors and capacitors has been done, e.g. for filters [4]. However, the author is not aware of publications on exhaustively transistor level circuit topology generation. This subject is addressed in a recently published PhD Thesis entitled "Transconductance Based CMOS Circuits: Circuit Generation, Classification and Analysis" [5]. In this thesis a Voltage Controlled Current Source (VCCS) or Transconductor plays a crucial role as an abstraction for the function of a MOS transistor, resistor or a combination of these components (see also Figure 1). All linear two-ports with two VCCSs have been generated using graph theory. The two-port parameters of the resulting circuits are determined by the transconductance of the VCCSs (hence "Transconductance Based").

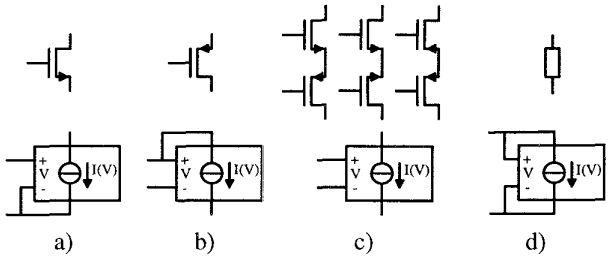

Figure 1: An NMOST (a), PMOST (b) or a common source pair of MOSTs (c) can be used as a VCCS. A resistor can also be modelled as a VCCS (d).

The current paper has two aims: 1) to present the design philosophy behind Transconductance Based Circuits; 2) to present an example of the design of a transconductance based variable gain amplifier to demonstrate the usefulness of systematic circuit topology generation. It will be shown that many different circuit topologies are found, that would not easily have been found in an intuitive way. The performance of the circuits has been evaluated by simulations. It appears that significant differences in performance occur, with various mixes of specific strong and weak points. This makes the availability of alternative circuits very useful to be able to choose the one that fits best to a specific set of requirements.

The paper is organised as follows. In section 2 the design philosophy of Transconductance Based CMOS Circuits is introduced. Then 14 alternative basic topologies with 2 VCCSs implementing an impedance matching variable gain amplifier are generated in section 3. In section 4 the performance of alternative circuit topologies is simulated and discussed, while conclusions are drawn in section 5.

2. TRANSCONDUCTANCE BASED CMOS CIRCUITS

Analogue circuits are commonly designed using simple circuits as building blocks (e.g. differential pairs and current mirrors). Apart from the elegance of simple solutions, there are other good reasons for this design practice: adding components tends to limit the high frequency potential of circuits (additional nodes) and tends to increase the noise level and power consumption. Hence, "squeezing" maximal performance out of a minimal set of components seems to be a very viable design philosophy.

In MOST circuits, transistors are the main components. The primary transistor property that is exploited in many circuits like the differential pair and the current mirror, is the

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transconductance of a MOST. Consequently, the principle of operation of many CMOS circuits can be understood by considering them as transconductance based circuits [5], i.e. circuits with a transfer function that is mainly determined by the transconductance of MOS transistors. Important reasons for this design practice are:

- The good matching of the transconductance values of equally biased MOSTs (better than 0.5% current matching is possible).
- The electronic variability of the transconductance of MOSTs. This allows for on-chip self-correction for spread in IC-processing (e.g. in Gm-C filters [6]) or for adaptive signal processing (e.g. AGC [7]).
- The previously mentioned simplicity of the circuits and related good HF-performance [8].
- The large range of transconductance values that the transconductance of a MOST can take (e.g. 1nS..1S [5]), which is much larger than the achievable conductance range for integrated resistors.

Another reason for choosing a VCCS is that it can also model a resistor (see Figure 1d), that is sometimes also used in MOS circuit design. Figure 1a and Figure 1b show the VCCS model for an NMOST and PMOST[1]. Unfortunately, in both cases there is a connection between one of the voltage and one of the current terminals, which limits the flexibility of use. However, by using two MOSTs a more flexible VCCS with a floating input and output port can be implemented as shown in Figure 1c (biasing sources have been omitted). This *VCCS* will now be used as a *generation element for circuit topology generation.* The use of this abstraction introduces hierarchy in the design procedure, which largely reduces the number of topologies to cope with (many different MOST circuits can be considered as different implementations of a single VCCS-circuit).

A VCCS model fits well to the function of a MOST, and in many cases also to a bipolar transistor. Furthermore, of course more sophisticated transconductor circuits (for an overview see [7, 5]) can be used to implement the VCCS if required, e.g. if tight requirements on the linearity are posed.

3. GENERATING VARIABLE GAIN AMPLIFIER TOPOLOGIES

It can easily be verified that two VCCSs are at least needed to implement non-unity V-V and I-I transfer functions (determined by a ratio of two transconductance values) apart from V-I and I-V relations. With *2 VCCSs* as *generating elements* a *graph based exhaustive circuit topology generation is performed* in [5]. The transfer function of the resulting circuit topologies have been analysed by symbolic analysis. After eliminating cases with no solution or a zero solution, 145 graphs of linear two-ports with 2 VCCSs remain. A detailed analysis shows that two-ports with infinite or finite valued port impedances can be implemented directly, while two-ports with zero port impedances can be approximated for large transconductance values [5]. The set of topologies thus includes most commonly required linear two-ports [9].

As a design example, the first stage of a variable gain amplifier will be considered. It is designed for application in an AGC amplifier that amplifies the TV-IF signal of a SAW-filter at 40MHz. As the SAW-filter characteristic is specified for a resistive load of 2Kohm, the amplifier should have a resistive input impedance. The amplification of the amplifier should be larger than 1 and electronically variable. Alternative topologies for this amplifier have been generated and selected in [5], with either an resistive input impedance or a high input impedance (if high, a resistor of 2Kohm is added). The output impedance is chosen either finite or high (if high, an additional resistor is added that fixes the gain). These choices result in 14 basic topologies with 2 VCCSs. Each of these topologies can be implemented in many different ways, depending on the connections between the voltage- and current-terminals of the VCCS (the simplest realisation of VCCS is a resistor, NMOST/PMOST or MOST-pair, see Figure 1). As a differential pair has four free terminals, it can always be used to implement a VCCS. In Figure 3 the resulting circuits are shown.

Some of the topologies are well-known from literature, e.g. the Gm-R amplifier stage a (with passive resistors [11] and triode resistors [12]), the cross-coupled stage b [13], and stage h [14]. However, many other alternatives are found that would not easily have been found with an intuitive approach.

4. AMPLIFIER SIMULATION RESULTS

In order to analyse and compare the performance of the amplifiers, simulations have been done for the amplifier stages of Figure 3, implemented in a standard 1μCMOS process. To examine the effect of topology on performance, all VCCSs have been implemented and biased in the same way as shown in Figure 2. Two MOS transistors in series are used to reduce the effect of finite output resistance on gain without significant degradation of HF properties [15]. The gain is controlled by the tail current of the differential pairs. The transconductance is tuned over a 1:4 range. The differential pairs have been scaled such that the minimum gain of all the amplifiers is 1.

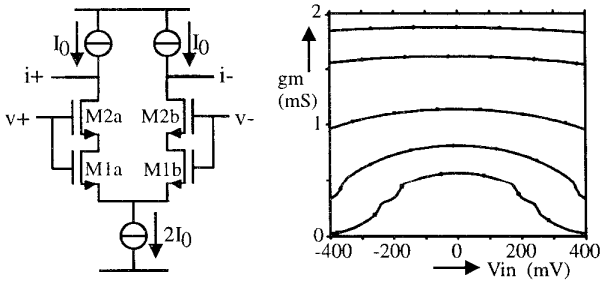

Figure 2: VCCS implementation used in simulations ($(W/L)_1$=150/1.5; $(W/L)_2$=300/1.5); I_0=0.13...2.7mA) and its (small signal) transconductance as a function of the (large signal) differential input voltage.

[1] The body effect of a MOS transistor is considered as a second order effect and is not taken into account in the (first order) model that is used for circuit topology synthesis.

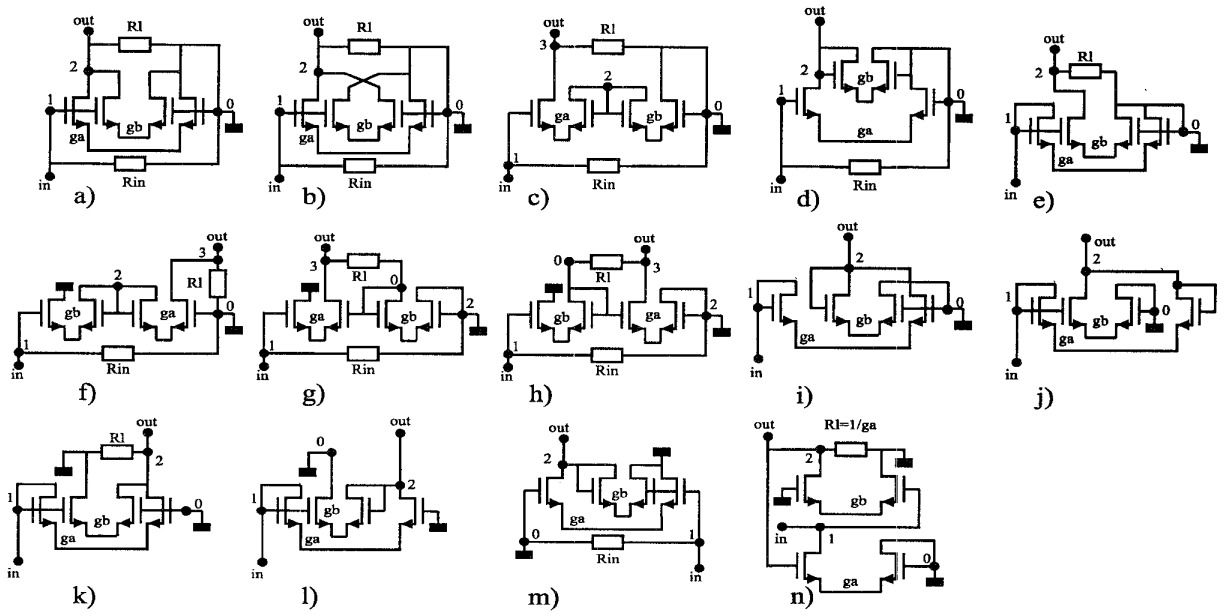

Figure 3: The Variable Gain Amplifier topologies generated in [5] implemented using differential pairs.

The performance of the resulting circuits as a function of a gain control variable pwr (pwr=-1 corresponds to a minimum gain of 1 and pwr=1 to the maximum gain) has been verified by simulations. The resulting simulated gain, input noise, distortion, bandwidth and power supply current are shown in Figure 4 to Figure 8. It appears that large differences in performance occur: the maximum gain ranges from 1.8 to 10; the equivalent input noise voltage from 4.7 to 36 nV/sqrtHz, the bandwidth from 18 to 275 MHz, the distortion from 0.01 to 1 %, and current consumption from 1.4 to 11 mA).

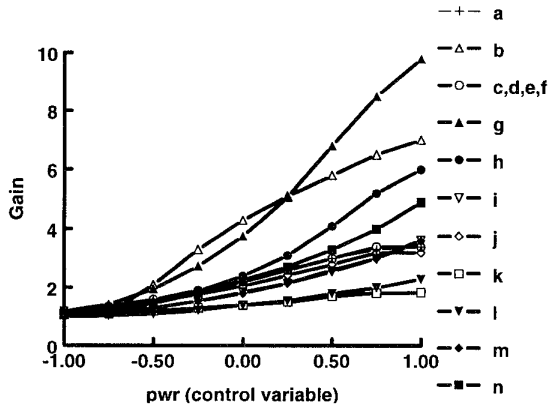

Figure 4: Gain of the circuits of Figure 3.

There is no clear "winning" circuit. Specific strong and weak points occur in different topologies, in various mixes. It is concluded that the set of requirements determines the most suitable topology, and that the availability of alternative circuits is very useful.

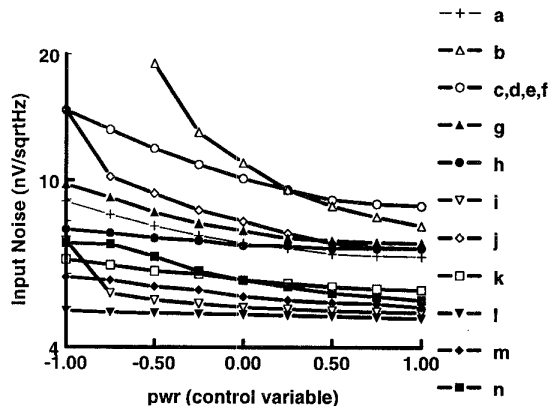

Figure 5: Input Noise of the circuits of Figure 3.

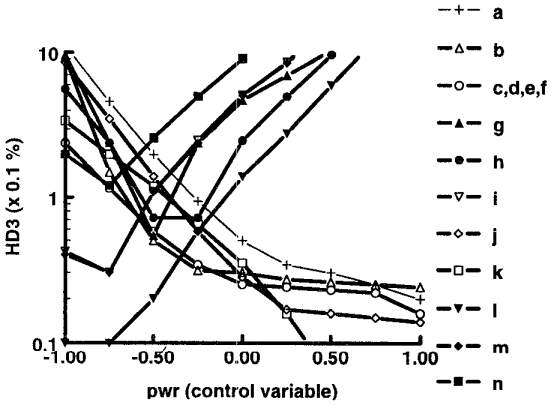

Figure 6: Distortion HD3 of the circuits of Figure 3.

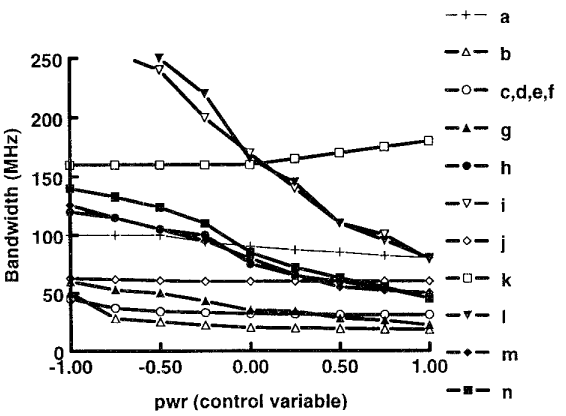

Figure 7: Bandwidth of the circuits of Figure 3.

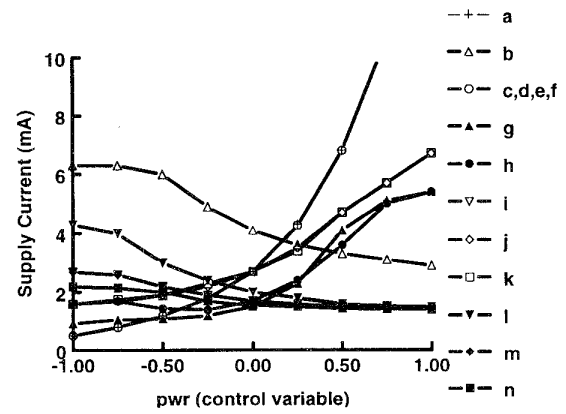

Figure 8: Supply Current of the circuits of Figure 3.

5. CONCLUSIONS

The use of a VCCS as an abstraction of the function of saturated MOS transistors or resistors has been motivated. A method for systematic circuit topology generation and analysis, based on VCCSs has been proposed. It results in much more alternative circuit topologies than a human designer would typically conceive: for an variable gain amplifier design 14 basic topologies with 2 VCCSs are found, which can each be implemented in many different ways using transistors and resistors. Using differential pairs as VCCS implementation, the amplifiers have been compared. The simulation results show that alternative circuits show significant differences in gain-range, distorsion, noise, bandwidth and current consumption, in various mixes of specific strong and weak points. This makes the availability of alternative circuits very useful to be able to choose the one that fits best to a specific set of requirements.

The set of alternative topologies can be very useful as a circuit topology database for future analogue CAD systems. Such systems might eventually beat human designers as they can explore much more design alternatives in a given time than a designer can.

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