RF Transconductor Linearization Technique Robust to Process, Voltage, and Temperature Variations

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***Abstract*— A new reconfigurable linearized low noise transconductance amplifier (LNTA) design for a software-defined radio receiver is presented. The transconductor design aims at realizing high linearity at RF in a way that is robust for Process, Voltage and Temperature variations. It exploits resistive degeneration in combination with a floating battery by-pass circuit and replica biasing to improve IIP3 in a robust way. The LNTA with current domain mixer is implemented in a 45nm CMOS process. Compared to an inverter based LNTA with the same transconductance, it improves P_{IIP3} from 2 dBm to a robust P_{IIP3} of 8 dBm at the cost of 67% increase in power consumption.**

***Keywords*— CMOS, Software-defined Radio, Receiver, Linearity, Transconductor, Transconductor Figure-of-Merit, PVT, robust circuit design.**

I. INTRODUCTION

Software-Defined-Radio (SDR) provides an economically viable solution to cope with the exploding number of wireless standards such as GSM, UMTS, LTE, LTE-A etc. and the various bands allocated across various countries and continents. Due to lack of linear and tunable RF filtering alternatives, a SDR receiver front-end has to contend with strong interferers that can degrade its performance. To combine receiver operation in a broad band of frequencies with impedance matching and low noise, receivers exploiting noise cancellation have proven useful [1,2,3]. Fig.1 shows a schematic diagram of a SDR receiver from [3] that exploits frequency translated noise cancellation (FTNC) [2,3]. As the main path can be very linear due to the use of a resistor and its distortion can also be reduced by the noise/distortion cancellation technique [1,2,3], the LNTA in the auxiliary path now becomes the bottle-neck for the out-of-band linearity of the receiver. A wide-band Low Noise Transconductance Amplifier (LNTA) is used in many recent CMOS receiver front-ends [3-5]. In this work, we introduce a technique to improve the linearity of this LNTA in a robust way, insensitive to process, temperature and voltage (PVT) variations.

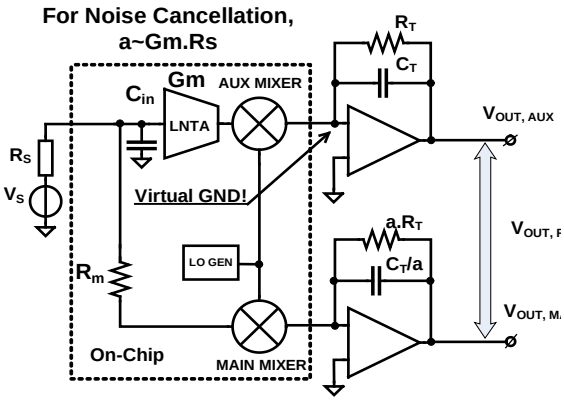


Fig. 1. Schematic diagram of a receiver requiring a high linearity Low Noise Transconductance Amplifier (LNTA).

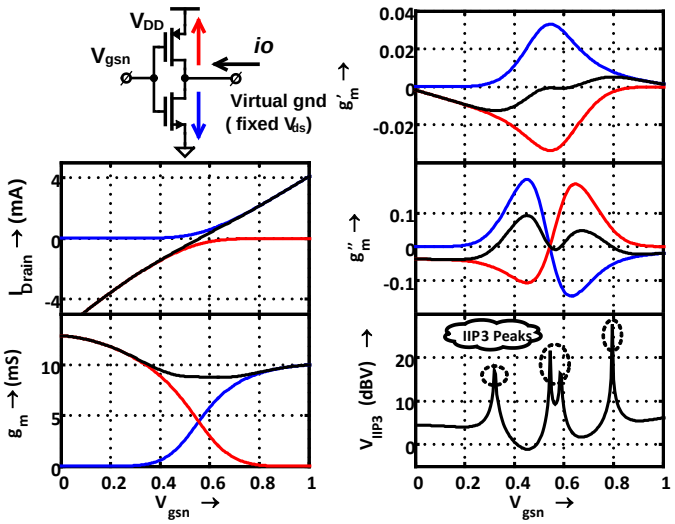


Fig. 2. Output (Drain) currents and their derivatives of NMOS (blue), PMOS (red) and CMOS (black) devices in a CMOS inverter.

High

I. THE CMOS TRANSCONDCUTOR

A. *Good Power efficiency, noise and bandwidth*

For a CMOS inverter (Fig2), the total transconductance g_m is given by the sum of the transconductances g_{mn} of NMOS and g_{mp} of the PMOS transistors respectively while reusing the bias current. Hence both transistor contribute signal, which is good

for low noise figure at high power efficiency (high gm/Id ratio). To linearize receivers ([4]), no RF voltage gain but only V-I conversion is done, while I-V conversion is moved to baseband and combined with filtering of out-of-band blockers, by trans-impedance amplifiers with RC feedback (R_TC_T).

linearity passive current mixing can be applied (Fig.1) and the low virtual ground node impedance is up-converted to the LNTA output. Hence the drain nodes of the inverter experience only a low voltage swing, which is good for their linearity. Moreover, avoiding voltage gain at RF can extend the bandwidth [2]. In Fig.1, this also happens as the low virtual ground node impedance pushes the pole at the output of the LNTA to a higher frequency.

B. High Linearity and Unreliable Nonlinearity Cancellation

For low drain voltage swings, the output i_o current is mainly defined by the input (gate) voltage perturbation v_i from a bias point, which can be written as a Taylor series expansion:

$$i_o \approx g_m v_i + g_m' \frac{v_i^2}{2} + g_m'' \frac{v_i^3}{6} \qquad (1)$$

$$g_m' = g_{mn}' + g_{mp}', \;\; g_m'' = g_{mn}'' + g_{mp}'', \; V_{IIP3} = \sqrt{\frac{8g_m}{g_m''}}$$

Here, g_m', g_{mn}', g_{mp}' and $g_m'', g_{mn}'', g_{mp}''$ are the first and second order derivatives of the transconductances of the CMOS, NMOS, PMOS devices respectively and V_{IIP3}[1] is the corresponding input referred third order intercept point ([9]). These are illustrated in Fig. 2. By properly sizing the transistors, and adjusting the biasing, it is possible to achieve cancellation of the second and third order derivatives. Notice the peaks in the V_{IIP3} (Fig.2) corresponding to the zero crossings in g_m''. This linearization technique is known as complementary derivative super-position ([9]). However, in practice these V_{IIP3} peaks (sweet spots) have somewhat limited benefit as they rely on cancellation between the P- and N-device, which varies with PVT. Moreover, sharp peaks only give good linearity for low swing, while higher order distortion products strongly come up with increasing voltage swing. These sweet spots which are easy to locate during measurements are not reliable.

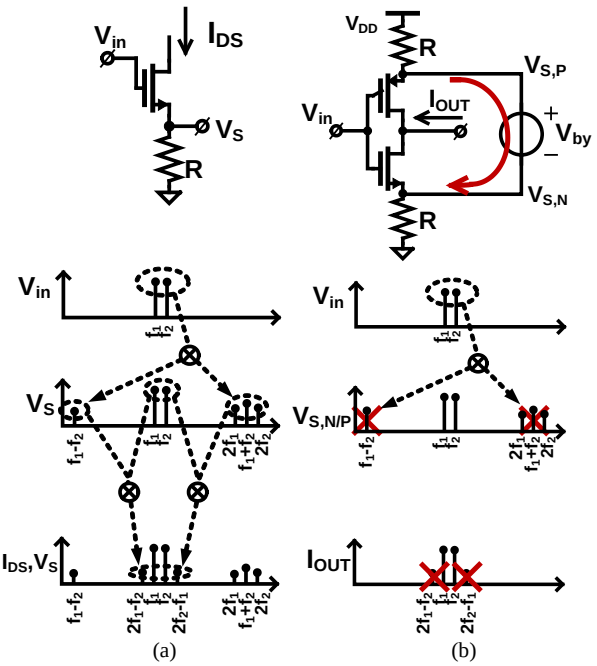


Fig. 3(a) Generation of third order distortion from second order distortion when a degenerated NMOS transistor is excited by two test tones. (b) Linearization concept using a floating battery V_{by} that provides a low impedance by-pass path for second order distortion currents to cancel without degrading the corresponding source voltages.

II. IMPROVING CMOS TRANSCONDUCTOR LINEARITY

A. Linearity with resistive source degeneration

Resistive degeneration is a well-known linearization technique exploiting negative feedback. A resistive degenerated MOST transistor as in Fig.3a, can potentially achieve high Normalized SNR when compared to other alternatives [8]. However, for low loop gain, the square-law term of a MOSFET can be problematic as it indirectly generates third-order distortion [9]. To understand this, it is useful realize that a MOS transistor is ideally a square law device with only the second order distortion. Its third and higher order non-linearity are a second order effect and are dependent on PVT variations. (hence an inverter shows PVT dependent IIP3 peaks). Now, if a source degeneration resistor is added in Fig 3a, due to the quadratic drain current the source voltage V_S will contain a quadratic term. The MOSFET will mix this quadratic term with a linear term on the gate (V_{in}) to *generate third order distortion which would not exist without resistive degeneration.*

To analyze 2-tone intermodulation distortion in Fig. 3a, the gate is excited by two test-tones at frequencies f_1 and f_2 that are closely spaced. Due to the MOSFET's second order distortion, the source voltage V_S has second order distortion components at frequencies f_2-f_1 and $2f_1$, $2f_2$ and f_1+f_2. The square law MOSFET term now results in *third* order distortion components in I_{DS} at frequencies $2f_1$-f_2 and $2f_2$-f_1. A similar effect happens in a degenerated PMOS transistor and when the two outputs are combined, a degenerated CMOS inverter can have more third order distortion than a CMOS inverter with the same biasing conditions.

III. CHIP IMPLEMENTATION DETAILS

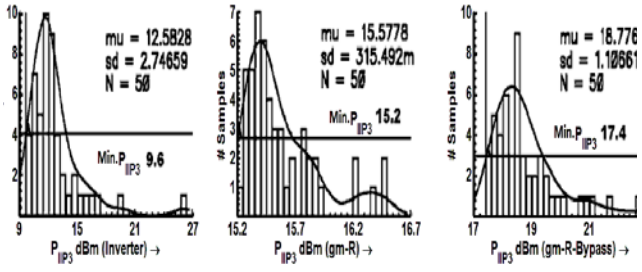
A. Improved LNTA Using a Floating Battery Circuit

Once we understand that it is the quadratic MOSFET current term through the degeneration resistors that largely causes the third order distortion problem, we can try to provide another current path for this term. This is the idea behind the new circuit topology

[1] V_{IIP3} in Volts is used here for convenience as we talk about a transconductor. For the receiver, we use P_{IIP3} in dBm with either 50Ω for single-ended or 100 Ω for (differential).

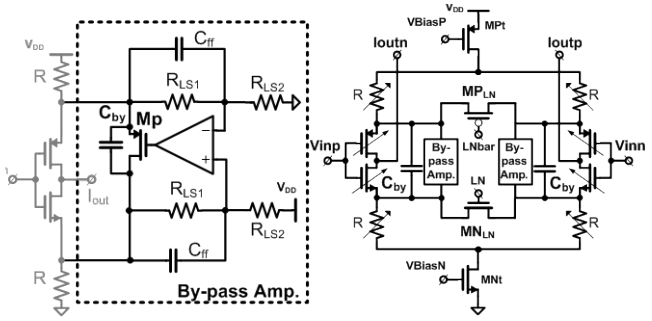
shown in in Fig 3b, which targets to provide a by-pass for the quadratic current (red arrow), so that it flows in a circle and not to the output. This is possible if we use a complementary circuit, and the quadratic terms of the NMOS and PMOS are designed to be equal. The floating battery in Fig 3b represents this low impedance path. In this new LNTA topology, the individual transistors do have second order distortion currents but their source voltages will ideally have no second order distortion and hence the third order distortion generation mechanism mentioned earlier is eliminated. In practice complementary P/N mismatches will introduce residual quadratic terms again, but significantly smaller.

Fig 4 shows simulation results in terms of histograms of P_{IIP3} obtained from 50 Monte-Carlo trial runs (around nominal conditions) of the input referred P_{IIP3} of a plain CMOS inverter, the same inverter resistively degenerated (gm-R), and the inverter with a floating battery bypass (gm-R-Bypass) as in Fig.3b. It can be inferred that resistive degeneration reduces the spread in the P_{IIP3}. The gm-R-Bypass has a bit higher spread in P_{IIP3} than degeneration without by-pass, but higher minimum $P_{IIP3,}$ thus providing a better guaranteed performance across PVT variations.



(a) (b) (c)

Fig. 4 Monte-carlo simulation of P_{IIP3} of (a) a CMOS inverter, (b) Degenerated CMOS inverter, and (c) Degenerated CMOS inverter with ideal floating battery bypass.



(a) (b)

Fig. 5 Schematic of (a) The improved LNTA's By-pass Amplifer, and (b) the LNTA's differential implementation with possibility to digitally tune the transconductance components and set the bias current using MNt/MPt,

Implementing an broadband high quality floating battery (V_{by}) is challenging. However, requirements can be relaxed as a low impedance path is mainly important at low frequencies (f_2-f_1) and at twice the LO frequencies ($2f_1$, f_1+f_2,$2f_2$). The impedance need not necessarily be low at the LO frequency itself. For low frequencies, we can achieve a low impedance path by using a floating voltage regulator, i.e. a "By-pass Amp." in Fig.5a. At high frequencies the capacitive path C_{by} provides a low impedance by-pass path for the double frequency terms. The regulator is implemented by a PMOS transistor (Mp) that is driven by an error amplifier. The error amplifier is an NMOS input single stage cascode differential amplifier with a cascaded PMOS current mirror load. The capacitors C_{ff} are used to stabilize the negative feedback loops. The resistors $R_{LS1,2}$ are used to derive a scaled version of the supply voltage to be used as the floating battery voltage. R_{LS2} are made variable with a feedback bias loop to automatically compensate PVT variations. MPt and MNt are triode MOSTs which are used to regulate the bias current of the LNTA and the bias voltages VBiasP and VBiasN are derived by using replica biasing.

An advantage of this circuit is that any noise currents generated by the bypass regulator that flows through Mp will circulate through the NMOS and PMOS transistors provided that they have the same transconductance and will not reach the output. Thus this transconductor is suitable for linear and low noise applications. Furthermore, in an advanced CMOS process, flicker noise corner frequencies are large. A degenerated MOS transistor has lower flicker noise corner than a MOS transistor. This advantage is also inherited by this improved LNTA.

The LNTA is made width-programmable for gain, linearity and input capacitance. MP_{LN} and MN_{LN} are used to set the LNTA in a low noise mode (without degeneration) in the absence of blockers. It is possible to switch on sections of the inverter to increase g_m to compensate for the reduction in gain due to resistive degeneration.

IV. MEASUREMENTS

To verify the improvement of IIP3 due to the by-pass circuit, an experimental chip was designed with only the crucial RF components that define RF-linearity. The parts indicated in the box of Fig.1 are implemented on chip. We implemented a fully differential version of the LNTA in a 45nm CMOS process. The mixers in Fig.1 are driven by 4-phase non-overlapping LO signals which are generated from an on-chip divide-by-2 circuit with 1.1V supply. The divider inputs are differential and are driven by an off-chip generated 2-times LO signal (2xLO). Four current-mode logic buffer stages improve the differential nature of 2xLO. The LNTA itself uses a 1.5V supply. Thick oxide devices were used in appropriate locations to avoid reliability problems. The active chip area (Fig.6a.) is approx. 0.3x0.3 mm^2. External OPAMPs were used in this research work to purely study the LNTA's linearity. All measurements were done with a fully differential setup. The LNTA of Fig.5a can be programmed in the following two modes:

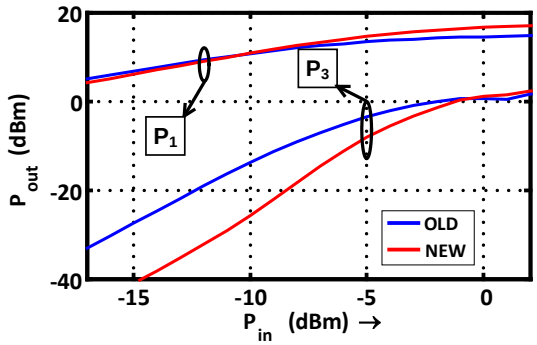
1) *Degeneration OFF ("OLD"), and*
2) *Degeneration ON ("NEW" Linear Mode).*

The bypass capacitor C_{by} is connected in both modes as using a series switch would degrade its high frequency Q factor. The by-pass amplifier is also kept on in "OLD" mode but at low bias. To test the beneficial effect of the by-pass in the new LNTA topology of Fig.5, we measured IIP3 and compression of the LNTA. For the IIP3 test, we used two test tones at offsets of 0.5 and

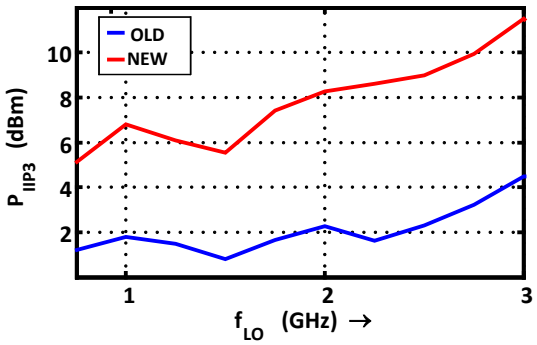
0.7MHz from the LO frequency (f_{LO}) with swept input powers of the two test tones. For fair comparison, the transconductance the two modes was programmed to be nearly equal. Fig.6a shows the results with for f_{LO} of 2GHz. We see that the P_{IIP3} improves from 2 dBm to 8 dBm. Although the absolute achieved IIP3 is less than expected from simulations, we clearly see a significant benefit in linearity of about 5 to 6dB. To see how the linearity improvement depends on frequency, we measured P_{IIP3} versus f_{LO} from 0.75 to 3GHz as shown in Fig.6b. For higher frequencies linearity improves somewhat, possibly because the bypass capacitor is more effective there.

In order to verify the LNTA topology's robustness to large signal non-linearity, a one-tone compression test was done by sweeping the power of a test tone at 500kHz from f_{LO} = 2GHz for both the modes. Compression points of -7 and -2dBm for both modes were found respectively. This demonstrates that the linearity improvement is robust for large input signals.

We also tested the combination of the AUX path at f_{LO} = 2GHz (Fig.1) with the highly linear (P_{IIP3}~20dBm) main path containing only the matching resistor and the main mixer to verify the 3dB improvement assuming a very linear main path. Indeed 8+3=11dBm was found. This shows that under noise cancellation conditions ([1-3]), the LNTA dominates the distortion performance.

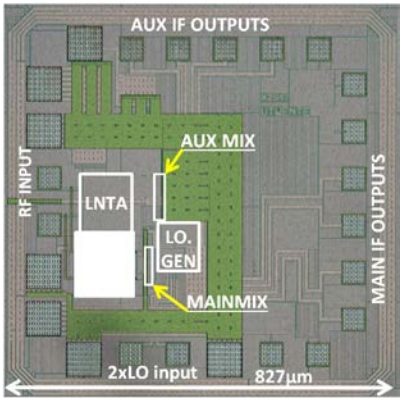


(a)

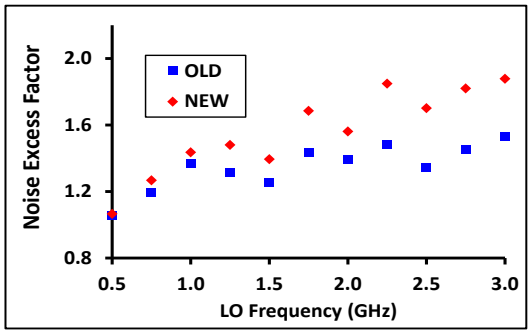


(b)

Fig.6 a) Measured 2-tone P_1 and P_3 at 2GHz, and b) P_{IIP3} vs f_{LO}



(a)



(b)

Fig.7 a) Chip Micrograph b) Measured Noise Excess factor

To analyze the noise performance of the LNTA, we obtained the input referred noise voltage of the LNTA by referring the output noise of the LNTA path to its input via its gain. The noise excess factor (NEF) ([8]) of the LNTA with mixer was calculated for various LO frequencies. The results in Fig.7b show that the noise performance is slightly degraded when using the new technique. This is because the noise of the battery circuit in Fig.5 does not affect the output current of the LNTA, provided that the transconductance of the NMOS and PMOS is almost the same.

To get an impression of the robustness of the linearity improvement, the chip was heated with a hot-air blower at 150°C in the "NEW" mode. The P_{IIP3} degrades only slightly by 0.55dB. The LNTA consumes 8.7 and 14.5mA in the Low Noise and Linear modes respectively.

V. CONCLUSIONS

A new circuit technique was proposed to linearize an LNTA in a robust way, insensitive to PVT. The circuit exploits resistive degeneration combined with a floating battery to address the problem of second-to-third order distortion conversion due to negative feedback with insufficient loop-gain. Experimental results confirm a robust improvement of both P_{IIP3} and the large signal compression, although the performance is less than predicted by simulations.

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