Analytical Design Equations for Class-E Power Amplifiers with Finite DC-Feed Inductance and Switch On-Resistance

Mustafa Acar, Anne Johan Annema and Bram Nauta
IC Design Chair, University of Twente, The Netherlands

***Abstract*— Many critical design trade-offs of the Class-E power amplifier (e.g power efficiency) are influenced by the switch on-resistance and the value of dc-feed drain inductance. In literature, the time-domain mathematical analyses of the Class-E power amplifier with finite dc-feed inductance assume zero switch on-resistance in order to alleviate the mathematical difficulties; resulting in non-optimum designs.**

We present analytical design equations in this paper for Class-E power amplifier taking into account both finite drain inductance and switch on-resistance. The analysis indicates the existence of infinitely many design equations; conclusions include:

1) Class-E conditions (e.g. zero voltage and zero slope) can be satisfied in the presence of switch-on resistance.

2) The drain-efficiency (η) of the Class-E power amplifier is upper limited for a certain operation frequency and transistor technology.

3) Using a finite dc-feed inductance instead of an RF-choke in a Class-E power amplifier can increase η by $\approx 30\%$.

I. INTRODUCTION

The Class-E power amplifier (PA) has been very popular due to it's high efficiency and the simple circuit structure [1]. However, the "finite dc-feed inductance" and the "non-zero switch on-resistance" significantly influence the performance of the Class-E PAs [2]. To alleviate the analytical complexity, theoretical analyses of the Class-E PA in the literature assumed either non-zero switch-on resistance and infinite dc-feed inductance (RF-choke) [3]- [7] or zero switch-on resistance and finite dc-feed inductance [8]- [11].

It is well-known that using a finite dc feed inductance instead of an RF-choke in Class-E has benefits [8], [9] including:

- a reduction in overall size and cost
- a higher load resistance for the same supply voltage and output power; yielding more efficient output matching networks
- larger switch parallel capacitor C (Fig.1a) for the same supply voltage, output power and load; enabling higher drain efficiency or higher frequency of operation.

In order to design Class-E PAs with optimum performance an improved analytical model that takes into account both the finite drain inductance and non-zero switch on-resistance is therefore needed [2].

In [12]- [21] the switch on-resistance is taken into account in the design of Class-E PAs. In [12], the shunt capacitor (C see Fig.1b) is assumed to be disconnected at the switch turn-on moment; which makes the analysis only an approximation. In [13], the shunt capacitor voltage ($V_C(t)$) is assumed to be zero at the switch turn-off moment; which is not analytically exact and can be accepted only for very small switch on-resistance ($R_{on} << R$).

The analysis and the design approach given in [14] offers no initial design guidelines, which tends to make it tedious because of the inherently large number of iterations that are required [5].

Moreover, the design methodologies presented in [15]- [20] either relies on iteration [15]- [19] or assigning initial values to some design variables [20]. In [21], an analytical solution for a sub-class of Class-E PA [1] is presented.

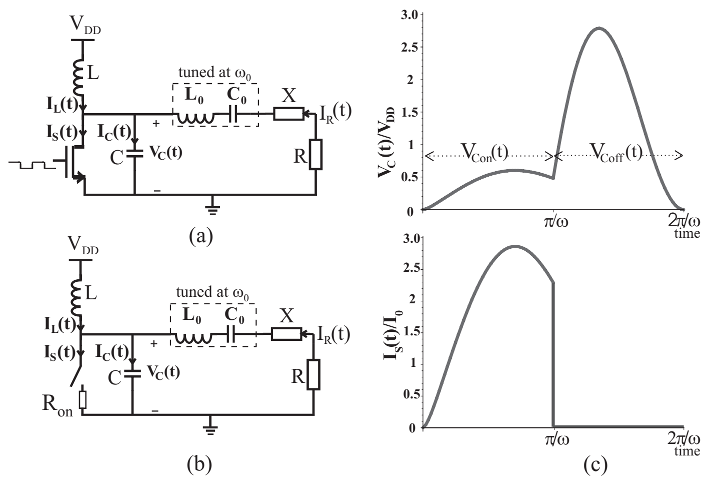

Fig. 1. (a) Single-ended Class-E PA (b) Model of Class-E PA with finite dc-feed inductance and switch on-resistance (c) Normalized switch (transistor) voltage and current for the model of Class-E PA

This paper presents an analysis (time domain) and design equations for Class-E PAs with *finite dc-feed inductance* and *non-zero switch on-resistance*. The analysis in this paper is based on closed form expressions like those presented in [9] and [10][2]. The analysis yields analytical design equations that show the relation between the various design parameters.

[1]The Class-E topology given in [21] assumes zero switch parallel capacitor; which is only applicable for very dedicated technologies with very small $R_{on}C_{out}$ product, where C_{out} is the switch (transistor) output capacitance.

[2]In [9] and [10], the switch on-resistance is assumed to be zero.

II. Analysis of Class-E Power Amplifier

A single ended switching PA topology is given in Fig.1a. For correct input parameters and the circuit element values, the circuit properly operates as a Class-E PA by satisfying the following conditions (1) [9]:

$$V_C(2\pi/\omega) = 0 \quad \text{and} \quad \left.\frac{dV_C(t)}{dt}\right|_{t=2\pi/\omega} = 0 \qquad (1)$$

A design set $K = \{K_L, K_C, K_P, K_X\}$(see Table-1) that relates circuit element values to operating conditions such as supply voltage, operating frequency and output power for the switching PA in Fig.1b can be derived. In [9], an analytical solution for K is given that enables infinitely many ideal Class-E realizations, to be selected by one parameter $q = \frac{1}{\omega\sqrt{LC}}$. In this paper, one more step is taken and the switch on-resistance R_{on} is included in the analysis. As it is shown (later) in this section the design set K can be expressed as a function of only two parameters q and $m = \omega R_{on} C$ both of which are free design variables and can take any positive real value.

$K_L = \frac{\omega L}{R}$, $K_C = \omega C R$, $K_P = \frac{P_{OUT} R}{V_{DD}^2}$, $K_X = \frac{X}{R}$

Table 1: Design Set K for Class-E PA[3]

As mentioned, the analytical solution in [9] is extended to cover Class-E PAs including R_{ON} in this paper.

A. Circuit Description and Assumptions

The circuit model of the Class-E PA is given in Fig.1b. For the analysis and the derivations in this paper a number of assumptions are made:

- the only real power loss occurs on R and R_{on}
- the switch (transistor) operates instantly with on-resistance (R_{on}) and infinite off-resistance
- the loaded quality factor (Q_L) of the series resonant circuit (L_0 and C_0) is high enough in order for the output current to be sinusoidal at the switching frequency
- the duty cycle is 50%

Fig.1c shows the switching behavior and the switch definition used: in the time interval $0 \le t < \pi/\omega$ the switch is closed and in $\pi/\omega \le t < 2\pi/\omega$ it is opened. This switching repeats itself with a period of $2\pi/\omega$.

B. Circuit Analysis

In the analysis, the current into the load, $I_R(t)$, is assumed to be sinusoidal. Note that theoretically this occurs only for infinite Q_L of the series resonant network consisting of L_0 and C_0. It is however a widely used assumption [8], [9], [12] that simplifies analysis considerably:

$$I_R(t) = I_R \sin(\omega t + \varphi) \qquad (2)$$

In the time interval $0 < t < \pi/\omega$, the switch is closed. The KCL at the drain node can be written as:

$$I_L(t) - I_S(t) - I_C(t) + I_R(t) = 0 \qquad (3)$$

[3] L_0 and C_0 seen in Fig.1 can be determined from the chosen loaded quality factor ($Q_L = \omega_0 L_0/R$) where $\omega_0 = 1/\sqrt{L_0 C_0}$.

Relation (3) can be arranged in the form of a linear, non-homogenous, second order differential equation

$$C\frac{d^2V_{C_{on}}(t)}{dt^2} + \frac{1}{R_{on}}\frac{dV_{C_{on}}}{dt} - \frac{V_{DD} - V_{C_{on}}}{L} - \omega I_R \cos(\omega t + \varphi) = 0 \qquad (4)$$

which has as solution

$$V_{C_{on}} = \frac{\left(q^4 \sin(\omega t + \varphi)\, m + \left(-q^2 + q^4\right)\cos(\omega t + \varphi)\right) p V_{DD}}{1 + (m^2+1)\, q^4 - 2\, q^2} + V_{DD} + e^{a\omega t} C_{on_2} + e^{b\omega t} C_{on_1} \qquad (5)$$

where, $a = \frac{-1+\sqrt{1-4\,q^2m^2}}{2m}$, $b = \frac{-1-\sqrt{1-4\,q^2m^2}}{2m}$ and $p = \frac{\omega L I_R}{V_{DD}}$. C_{on_1} and C_{on_2} follow from the continuity of the capacitor voltage (C) and the inductor (L) current at the switch-on moment.

In the time interval $\pi/\omega < t < 2\pi/\omega$, the switch is opened. Then, in the Class-E PA the current through capacitance C is

$$I_C(t) = \frac{1}{L}\int_{\pi/\omega}^{t} (V_{DD} - V_{C_{off}}(t))\, dt + I_L\left(\frac{\pi}{\omega}\right) + I_R(t) \qquad (6)$$

Relation (6) can be re-arranged in the form of a linear, nonhomogeneous, second-order differential equation

$$LC\frac{d^2V_{C_{off}}(t)}{dt^2} + V_{C_{off}}(t) - V_{DD} - \omega L I_R \cos(\omega t + \varphi) = 0 \qquad (7)$$

which has as solution

$$V_{C_{off}}(t) = C_{off_1}\cos(q\omega t) + C_{off_2}\sin(q\omega t) + V_{DD} - \frac{q^2}{1-q^2} p V_{DD} \cos(\omega t + \varphi) \qquad (8)$$

C_{off_1} and C_{off_2} follow from the Class-E conditions (1).

It follows from (5) and (8) that $V_{C_{on}}(t)$ and $V_{C_{off}}(t)$ can be expressed in terms of V_{DD} and ω hence be solved analytically only if φ, q, p and m are known. The derivation of the four parameters φ, p, q and m is the next step in the solution.

By using the continuity of the inductor current and the capacitor voltage at the switch turn-off moment we can derive two independent equations which can be shown to have the same format:

$f_i(p, q, \varphi, m) = p\Big(a_i(q,m)\cos(\varphi) + b_i(q,m) sin(\varphi)\Big) + c_i(q,m) = 0$, where $i = 1, 2$.

The variables p and φ can be solved by using $f_1(p, q, \varphi, m)$ and $f_2(p, q, \varphi, m)$ in terms of q and m as given in the appendix. Here, q and m are free variables that can mathematically take any positive real value.

C. Design sets for Class-E operation

The results of the mathematical derivation of the solutions leading to Class-E operation can be used to derive an an easy-to-use design procedure for Class-E PAs. Using the result of the derivation for $p(q,m)$ and $\varphi(q,m)$, analytical expressions for the design set $K = \{K_L, K_C, K_P, K_X\}$ can readily be derived.

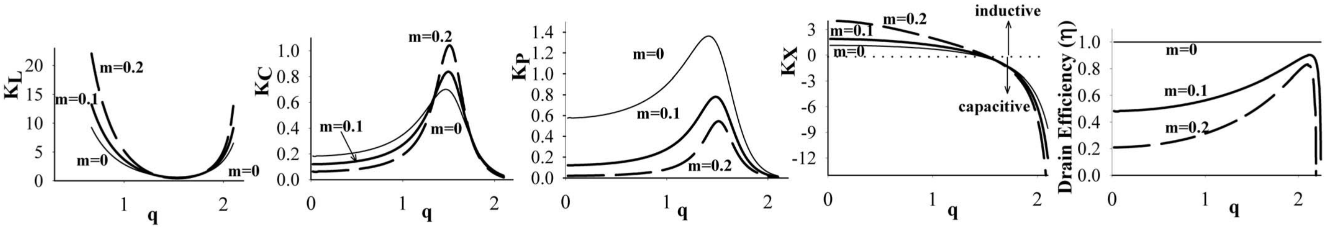

Fig. 2. (a) Design set K and drain efficiency (η) as a function of q for $m = 0, 0.1, 0.2$.

K_L : follows from the principle of power conservation:

$$I_R^2 R/2 + P_{switch} = I_0 V_{DD} \tag{9}$$

In this relation, I_0 is the average supply current:

$$I_0 = \frac{\omega}{2\pi R_{on}} \int_0^{\pi/\omega} V_{C_{on}}(t)dt \tag{10}$$

and,

$$P_{switch} = \frac{\omega}{2\pi R_{on}} \int_0^{\frac{\pi}{w}} \left(V_{C_{on}}(t)\right)^2 dt$$

Substitution of (10) and p in (9) yields

$$K_L(q,m) = \frac{-(pV_{DD}q)^2 m\pi}{\omega \int_0^{\frac{\pi}{w}} (V_{C_{on}}(t)^2 - V_{DD}V_{C_{on}}(t))dt}$$

Since p and φ are all functions of q and m, $K_L(q)$ is a function of e.g. only q and m.

K_C **:** follows directly from the definition of q and K_L:

$$K_C(q,m) = \frac{1}{q^2 K_L(q,m)}$$

K_P **:** can easily be found as a function of q and m by using $I_R = \sqrt{2P_{OUT}/R}$ and the definition of p:

$$K_P(q,m) = p(q,m)^2/(2K_L(q,m)^2)$$

K_X **:** can be derived using two fundamental quadrature Fourier components of $V_C(t)$.

$$V_R = \int_0^{\frac{\pi}{\omega}} \frac{V_{C_{on}}(t)}{\pi} \sin(\omega t+\varphi)\, dt + \int_{\frac{\pi}{\omega}}^{\frac{2\pi}{\omega}} \frac{V_{C_{off}}(t)}{\pi} \sin(\omega t+\varphi)\, dt$$

$$V_X = \int_0^{\frac{\pi}{\omega}} \frac{V_{C_{on}}(t)}{\pi} \cos(\omega t+\varphi)\, dt + \int_{\frac{\pi}{\omega}}^{\frac{2\pi}{\omega}} \frac{V_{C_{off}}(t)}{\pi} \cos(\omega t+\varphi)\, dt$$

$$K_X(q,m) = V_X/V_R$$

Drain efficiency(η): can be derived as a function of q and m.

$$\eta(q,m) = 1 - \frac{P_{switch}}{V_{DD}I_0} = 1 - \frac{\int_0^{\frac{\pi}{w}} (V_{C_{on}}(t)^2)dt}{V_{DD}\int_0^{\frac{\pi}{\omega}} V_{C_{on}}(t)dt}$$

We verified the given design equations in this paper by simulating the model given in Fig.1b by transient and pss (periodic steady state) simulations in spectre (cadence). Very good agreement in the waveforms and the drain efficiency are observed between the simulations and the theory with a discrepancy of $\approx 2\%$; attributed to the finite value of $Q_L = 10$.

In theory, q can take any positive real number however, as it is seen in Fig.2 K_C, K_P and η approach to zero for $q > 2$. Therefore, the useful range of the analytical solution can be assumed to be restricted to $0 < q < 2$ in Class-E PA designs. Similarly, as m increases K_P and η drops as observed in Fig.2; indicating the degradation in Class-E PA performance.

Design Details	RF-choke (q=0)	finite (q=1.47)	finite (q=1.78)
f (GHz), V_{DD}(V), Q_L	2.4, 0.5, 10	2.4, 0.5, 10	2.4, 0.5, 10
P_{OUT}/P_{DC} (mW)	10.6/22.2	11.8/17.0	12.1/15.2
m, **Drain Efficiency**(η)	**0.1**, **47.7%**	**0.1**, **69.4%**	**0.1**, **79.6%**
L, L_X(nH), C(pF)	**20.29**, 0.38, 2.59	**0.72**, 0, 2.82	**0.4**, - ,3.48
R(Ω), C_X(nF)	**3.06**, -	**19.47**, -	**5.06**, 6.88
(W(u)/L(u)), K_L	(297/0.1), 100	(323/0.1), 0.56	(398/0.1), 1.19
K_C, K_P, K_X	0.12, 0.12, 1.89	0.83, 0.78, 0	0.27, 0.20, -1.90
Technology	90nm CMOS	90nm CMOS	90nm CMOS

Table 2: Comparison and design summary of the three Class-E PA designs for $m = 0.1$ and $q = 0, 1.47, 1.78$ in CMOS 90nm transistor technology

III. Design Examples and Discussion

The analytical design equations reveal very important properties of the Class-E PAs. For example, we can express $m \approx \beta\omega$ where $\beta = R_{on}C_{out}$. β is a characteristic property of the transistor technology used as a switch in Class-E PA design[4]. For a certain operation frequency and transistor technology m has a certain value. As it is seen in Fig.2, there is a maximum efficiency level that could be achieved for a given m; showing that the transistor technology and the frequency of operation sets an upper limit for η of a Class-E PA.

The chosen value of q considerably influence η as observed from Fig.2 and the simulation results given in Table-2. We designed three Class-E PAs for an output power of 10 mW[5]. Finite dc-feed Class-E PA(q=1.78) has η that is $\approx 30\%$ higher than RF-coke Class-E PA($q = 0$); indicating how much η can be influenced by the chosen design equations.

[4] In order to minimize R_{on}, maximum possible transistor size can be chosen for which transistor output capacitance $C_{out} = C$.

[5] Slightly higher output power than 10 mW is attributed mostly to deviation of transistor characteristic from an ideal switch behavior at high frequency.

Although the Class-E PA($q = 1.47$) has lower η than the Class-E PA($q = 1.78$) it's load resistance(R) is ≈ 4 times higher than that of the Class-E PA($q = 1.78$); which is very advantageous for low supply voltage - high output power Class-E amplifiers[6]

The Class-E PA($q = 1.78$) can be used for low power applications (e.g. wireless sensors) where the transmit power levels are low $\approx (1-3)mW$ [22] and high efficiency is crucial. If the Class-E PA($q = 1.78$) is designed for an output power of $1\ mW$, it needs $R \approx 50\ \Omega$; meaning that a matching network between the PA and the antenna is not needed.

IV. Conclusion

In this paper, we present a time domain analysis and closed form analytical design equations for Class-E power amplifiers with *finite dc-feed inductance* and *non-zero switch on-resistance*. Important outcomes of the analysis include:

1) Class-E conditions (e.g zero voltage and zero slope) can be satisfied in the presence of the switch on-resistance.

2) Drain efficiency (η) for Class-E PAs is upper limited by the transistor technology and the operation frequency.

3) Using a finite dc-feed inductance instead of an RF-choke in Class-E PAs increases η. Depending on the transistor technology and the operation frequency the increase in η can be as high as $\approx 30\%$.

References

[1] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers" *IEEE JSSC*, vol. SC-10, pp. 168-176, June 1975.

[2] Lie, D.Y.C. et al. "The limitations in applying analytic design equations for optimal class E RF power amplifiers design" *VLSI Design, Automation and Test, IEEE* 2005, pp:161 - 164

[3] D. K. Choi and S. I. Long, "A Physically Based Analytic Model of FET Class E Power Amplifiers Designing for Maximum PAE," IEEE Trans. on Microwave Theory and Techniques, vol. 47,pp. 1712-1720 1999

[4] Kessler, D.J.; Kazimierczuk, M.K. "Power losses and efficiency of class-E power amplifier at any duty ratio" /emphCircuits and Systems I: Regular Papers, IEEE Transactions on [Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on] vol: 51, pp: 1675-1689, Sept. 2004

[5] D. K. Choi "High Eficiency Switched-Mode Power Amplifiers For Wireless Communications" PhD thesis, page 121.

[6] Alinikula, P.; "Optimum component values for a lossy Class E power amplifier" *International Microwave Symposium Digest, IEEE* vol.3, June 2003 pp:2145 - 2148

[7] Raab, F.H.; Sokal, N.O.; "Transistor power losses in the class E tuned power amplifier" *IEEE JSSC* vol. 13, Dec 1978 pp:912 - 914

[8] R. Zulinski, J. Steadman, "Class E Power Amplifiers and Frequency Multipliers with finite DC-Feed Inductance," *IEEE Trans. on CAS*, vol. 34, Sep 1987, pp. 1074-1087

[9] M. Acar, A.J. Annema, B. Nauta "Generalized Design Equations for Class-E Power Amplifiers with Finite DC Feed Inductance" *36th European Microwave Conference*, September 2006, pp. 13081311.

[10] M. Acar, A.J. Annema, B. Nauta "Generalized Analytical Design Equations for Variable Slope Class-E Power Amplifiers" *13th IEEE International Conference on Electronics, Circuits and Systems*, December 2006, accepted for publication.

[11] Choi, D.K.; Long, S.I.; "Finite DC feed inductor in class E power amplifiers-a simplified approach" *International Microwave Symposium Digest, IEEE* vol. 3, June 2002 pp:1643-1646

[12] Wang, C.; Larson, L.E.; Asbeck, P.M.; "Improved design technique of a microwave class-E power amplifier with finite switching-on resistance" *Radio and Wireless Conference, IEEE*, Aug. 2002, pp:241-244

[13] Ho, C.K.; Wong, H.; Ma, S.W.; "Approximation of non-zero transistor ON resistance in class-E amplifiers" *Proceedings of the Fifth IEEE International Caracas Conference on*,vol. 1, Nov. 2004, pp:90-93

[14] Avratoglou, C.P.; Voulgaris, N.C.; Ioannidou, F.I.; "Analysis and design of a generalized class E tuned power amplifier" *Circuits and Systems, IEEE Transactions on* vol. 36, Aug. 1989, pp:1068-1079

[15] Sekiya, H.; Sasase, I.; Mori, S.; "Computation of design values for Class E amplifiers without using waveform equations" *Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on* vol. 49, July, 2002, pp:966-978

[16] Reynaert, P.; Mertens, K.L.R.; Steyaert, M.S.J.; "A state-space behavioral model for CMOS class E power amplifiers" *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 22, Feb. 2003, pp:132-138

[17] Mandojana, J.C.; Herman, K.J.; Zulinski, R.E.; "A discrete/continuous time-domain analysis of a generalized class E amplifier" *Circuits and Systems, IEEE Transactions on* vol. 37, Aug. 1990, pp:1057 - 1060

[18] Choi, Y.-B.; Cheng, K.-K.M.; "Generalised frequency-domain analysis of microwave Class-E power amplifiers" *Microwaves, Antennas and Propagation, IEE Proceedings*, vol. 148, Dec. 2001, pp:403-409

[19] Tabrizi, M.M.; Masoumi, N.; "High efficiency class-E switched mode power amplifier design and optimization with random search algorithm" *Microelectronics ICM Proceedings*, 2004, pp:283 - 286

[20] J.-K. Jau, Y.-A. Chen, T.-S. Horng, and T.-L. Wu "Optimum Analytical Design Solution to Integrated Class-E Amplifiers" *Proceeding of Wireless Networks and Emerging Technologies* - 2005

[21] Mury, T.; Fusco, V.F.; "Analysis and synthesis of pHEMT class-E amplifiers with shunt inductor including ON-state active-device resistance effects" *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 53, July 2006, pp:1556-1564

[22] Chee, Y.H.; Rabaey, J.; Niknejad, A.M.; "A class A/B low power amplifier for wireless sensor networks" *Proceedings of International Symposium on Circuits and Systems*, vol. 4, May 2004 pp: 409-412

Appendix I

In this section the solution for p and φ in terms of q and m are given[7].

$$
\begin{aligned}
p = &\ \frac{\sqrt{\left(g_1 h_3 - g_3 h_1\right)^2 + \left(h_2 g_3 - h_3 g_2\right)^2}}{-g_1 h_2 + g_2 h_1}, \varphi = \arctan\left(h_2 g_3 - h_3 g_2, g_1 h_3 - g_3 h_1\right) \\
g_1 = &\ \frac{-e^{a\pi}\left(A + bmq^2\right) + e^{b\pi}\left(A + amq^2\right)}{B\left(-b+a\right)} - \frac{q\sin\left(q\pi\right)}{q^2-1} + \frac{mq^2}{B} \\
g_2 = &\ -\frac{\left(\cos\left(q\pi\right)+1\right)q^2}{q^2-1} + \frac{m^2q^2\left(q-1\right)\left(q+1\right)}{B} + \\
&\ \frac{-e^{a\pi}\left(Ab - mq^2\right) + e^{b\pi}\left(Aa - mq^2\right)}{B\left(-b+a\right)} \\
g_3 = &\ \frac{e^{b\pi}a - e^{a\pi}b}{-b+a} - \cos\left(q\pi\right) \\
h_1 = &\ \frac{m^3q^2\left(q-1\right)\left(q+1\right)}{B} - \frac{q\left(m\cos\left(q\pi\right)q + \sin\left(q\pi\right) + mq\right)}{q^2-1} \\
&\ +m\Big(\frac{ae^{a\pi}\left(A + bmq^2\right)}{B\left(-b+a\right)} - \frac{be^{b\pi}\left(A + mq^2a\right)}{B\left(-b+a\right)}\Big) \\
h_2 = &\ -\frac{m^2q^2}{B} + \frac{q^2\left(m\sin\left(q\pi\right)q - \cos\left(q\pi\right) - 1\right)}{q^2-1} \\
&\ +m\Big(\frac{ae^{a\pi}\left(Ab - mq^2\right)}{B\left(-b+a\right)} - \frac{be^{b\pi}\left(Aa - mq^2\right)}{B\left(-b+a\right)}\Big) \\
h_3 = &\ -\cos\left(q\pi\right) + m\sin\left(q\pi\right)q + m\left(\frac{ae^{a\pi}b}{-b+a} - \frac{be^{b\pi}a}{-b+a}\right) + 1 \\
A = &\ \left(q^4 - q^2\right)m^2 \text{ and } B = 1 + m^2q^4 - 2m^2q^2 + m^2
\end{aligned}
$$

[6]In order to obtain high output power from low supply voltage Class-E PAs a matching network that steps down 50 Ω antenna impedance to low impedance values is used. In the absence of high Q inductors the matching network can be very lossy for high transformation ratios.

[7]Two roots exist for p and φ. The second root is p'=-p and $\varphi' = \arctan\left(-h_2 g_3 + h_3 g_2, -g_1 h_3 + g_3 h_1\right)$. Both roots result in the same K.