

Frequency Compensation of an Audio Power Amplifier

R.A.R. van der Zee and R. van Heeswijk

Abstract— A car audio power amplifier is presented that uses a frequency compensation scheme which avoids large compensation capacitors around the MOS power transistors, while retaining the bandwidth and stable load range of nested miller compensation. THD is 0.005%@(1kHz, 10W), SNR is 108dB, and the amplifier is stable for any passive load up to 50nF.

Index Terms—Power amplifiers, Audio amplifiers, Frequency compensation

I. INTRODUCTION

The growth of in-car entertainment systems demands smart power devices, including audio power amplifiers. Despite the trend towards class-D systems, integrated class AB amplifiers are still superior in terms of frequency response, integration level and ease of application. The market drive for lower distortion and higher stability demands good frequency compensation schemes.

Audio amplifier design has similarities to general purpose OPAMP design. A large bandwidth is desired for low distortion and the load is unpredictable, with especially capacitive loads causing problems. Several publications [1-5] address this issue with frequency compensation schemes that - in their current form- are less fit for our purpose. All these techniques require compensation capacitors (C_m) that are much larger than the circuit parasitics, including the gate-source capacitance (C_{gs}) of the power transistor. In power amplifiers, however, the power transistors occupy most of the chip area, so $C_m \gg C_{gs}$ is not feasible. Although $C_m < C_{gs}$ could still work, pole-splitting would be limited and the achievable Unity-Gain Frequency (UGF) would be reduced. Furthermore, parallel gm paths to the output [2-5] are difficult to combine with proper class AB control, which is indispensable for audio power amplifiers which can have a quiescent-to-maximum current ratio of 1:500.

We propose a modification to Nested Miller Compensation (NMC) [1] such that with limited C_m we can get the same UGF as if with large C_m . That way, we can use the parasitic

Ronan van der Zee is with the IC-Design group of the University of Twente, P.O. Box 217, 7500AE, Enschede, the Netherlands. E-mail: r.a.r.vanderzee@utwente.nl. Remko van Heeswijk is with NXP in Nijmegen, the Netherlands.

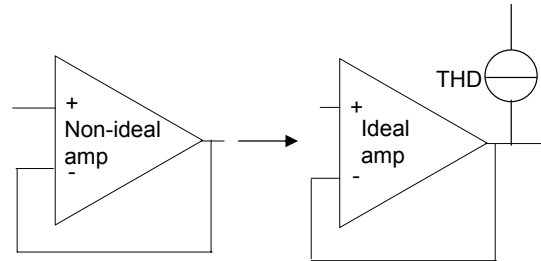


Fig. 1: Power amplifier distortion modelling

gate-drain capacitance of the power transistors as C_m and need only a small extra compensation capacitance. Inspired by [6], this is possible when we degenerate the gain of the penultimate stage, although we use more stages and small instead of very large C_m .

II. OUTPUT IMPEDANCE

In most publications about the stability of amplifiers, focus is on the open loop frequency transfer function. Usually, this transfer function is analysed mathematically, with the load assumed to be purely capacitive, or capacitive and resistive. The disadvantage of this approach is that it is very difficult to assess the behavior of the system for varying loads. Several simplifications in the mathematical analysis are only allowed for e.g. large load capacitances or high load resistances.

A much easier method in this respect is to look at the output impedance of an amplifier circuit. It offers several advantages. a) The mathematical analysis has one order less because a voltage source is connected to the output. b) The effect of complex loads can easily be identified. When e.g. the output impedance is inductive at a certain frequency, and one would connect a capacitor at the output with the same impedance at that frequency, a resonant circuit is formed that would certainly lead to peaking in the frequency transfer or oscillation. c) In power amplifiers, the output impedance gives an indication of the distortion. In our case the output stage is a common-source stage for maximum output swing, giving the output a current-source character. Since the dominating source of distortion is the power transistor, this means the amplifier can be modelled as an ideal amplifier with a parallel distortion current source. See Fig. 1. Therefore, lower closed loop output impedance at the same closed loop gain means lower distortion. d) The output impedance can be measured on a fabricated chip, easing the verification of calculations and simulations.

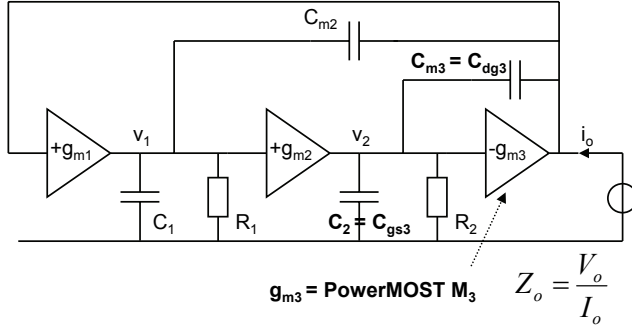


Fig. 2: Nested Miller Compensation (NMC)

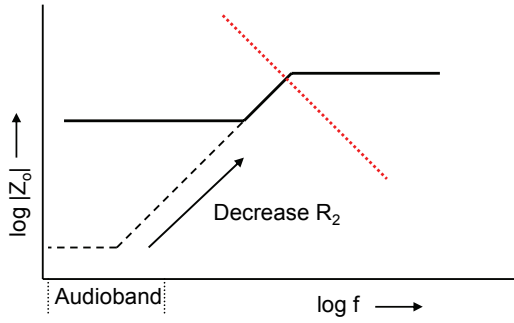


Fig. 3: Gain degeneration

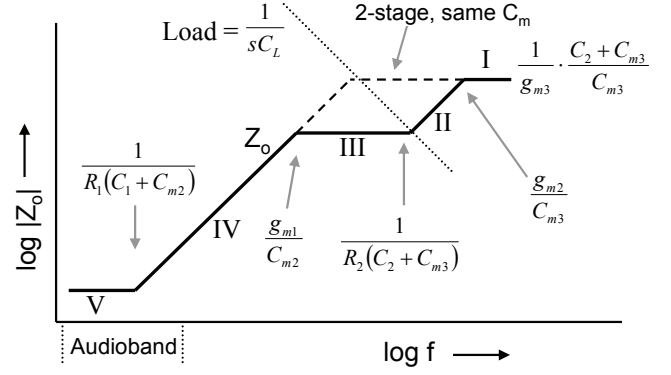


Fig. 4: Output impedance of Fig. 2 and of two-stage NMC (dashed)

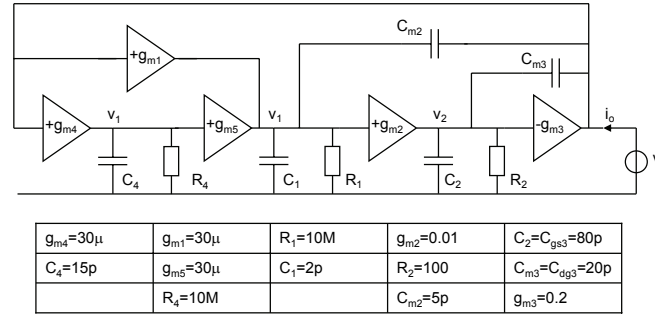


Fig. 5: Frequency compensation setup of one bridge-half

III. FREQUENCY COMPENSATION SETUP

A. Degeneration of second stage gain

Starting point is a miller compensated two-stage opamp formed around g_{m2} , g_{m3} and C_{m3} in Fig. 2. The output impedance is sketched in Fig. 3, where the direct contribution of C_{m3} to the output impedance is neglected because it manifests itself only at very high frequencies. Also sketched in Fig. 3 is what happens to the output impedance when R_2 is decreased. The pole and the zero move much closer together. Consequently, the phase of the output impedance does not get very close to 90 degrees, so a capacitive load, indicated with the red line in Fig.3, will not cause much ringing in the frequency response. The opamp with decreased R_2 , however, hardly has any gain, so an extra path with g_{m1} must be used, as indicated in Fig. 2. This leads to the output impedance drawn in Fig. 4.

To get a simple expression for Z_o , we again neglect the direct contribution of C_{m3} and C_{m2} . Furthermore, we will assure that $g_{m1}R_1 \gg 1$ and $C_{m2} \gg C_1$. If $g_{m2}/C_{m3} \gg g_{m1}/C_{m2}$, in other words: the UGF of the inner loop is much larger than the UGF of the outer loop, the expression for Z_o can be approximated with a Taylor expansion. The resulting values for the poles and zero's are indicated in the bode plot of Z_o in Fig. 4. As a reference, the output impedance of two-stage NMC with the same limited C_m is plotted as a dashed line.

For high frequencies (region I), the output impedance is real, so for a small load capacitance (C_L) the OTA is stable. When C_L is increased, it will cross the output impedance in an inductive part (II). This constitutes a resonant circuit at that frequency, leading to peaking in the frequency response. The ratio between the zero and pole that form the borders of region II determines how bad the worst case peaking is. In our case, where $C_{m3}=C_{dg3}=20pF$, $C_2=C_{gs3}=80pF$ and $g_{m2}R_2=1$, the ratio is 5, leading to approximately 45° phase margin. Increasing C_L further, the system is more stable again (III), and only for larger C_L (IV) stability is compromised. Note that the stability of two-stage NMC would already be compromised for C_L larger than indicated in Fig. 4, a significant factor $g_{m2}R_2(C_2+C_{m3})/C_{m3}$ ($= 5$ in our case) lower. Concluding, we see that the drawbacks of the limited miller capacitance have been overcome.

One might be tempted to look at this structure as a simple way of driving the gates of the power transistors with a low-impedance source, a kind of resistive broadbanding. It is not that simple, however, because a smaller C_{m3} would then be favorable, as it limits the capacitive load seen by g_{m2} . Our analysis, however, shows that a smaller C_{m3} will actually decrease the phase margin for capacitive loads in region II in Fig. 4.

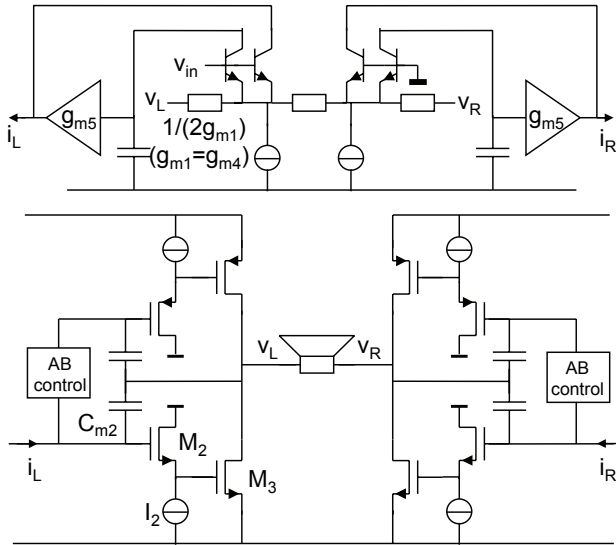


Fig. 6: Basic topology of one channel

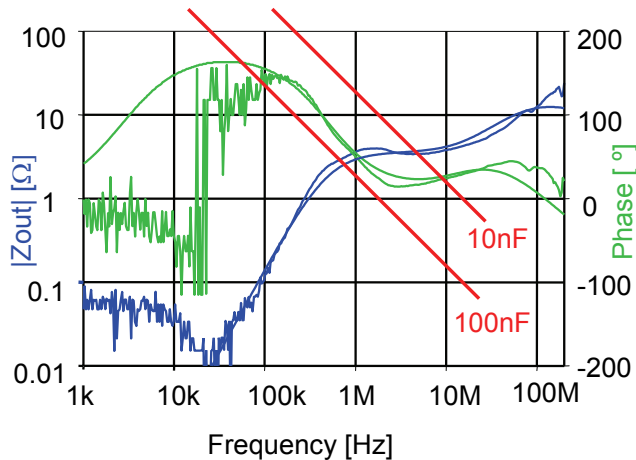


Fig. 7: Output impedance simulated (Fig. 5) and measured (packaged product). Red lines are possible load capacitances.

B. Extra gain path

For our purpose, the amplifier still doesn't have enough gain in the audio band, so another gain path (with $g_{m4,5}$) is added in parallel to g_{m1} , dimensioned such that it adds gain (and phase shift) only below $g_{m1}/C_{m2} = 1\text{MHz}$ (see Fig. 5). This technique also works with normal NMC, but it can be shown that due to the limited C_m , and consequently low UGF, the contribution would be marginal here.

C. Driving the load

The calculations above assumed a constant g_{m3} , whereas in reality g_{m3} varies strongly. The calculations are done for quiescence, where the power transistors are almost in weak inversion, with a very low g_{m3} . When the power transistors carry a larger current, the whole curve in Fig. 4 simply shifts down, only improving the stability of the amplifier.

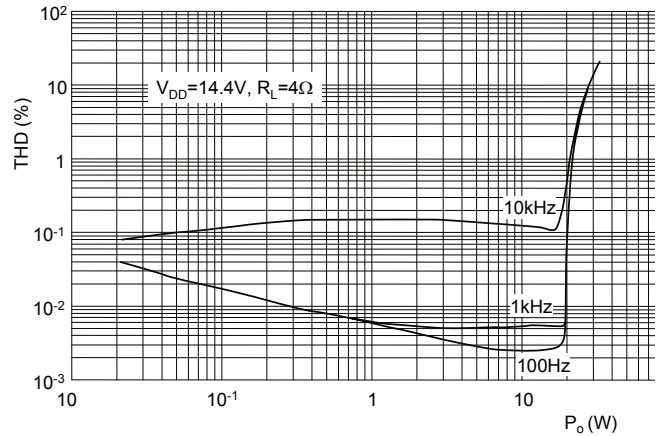


Fig. 8: THD+N as a function of output power and frequency.

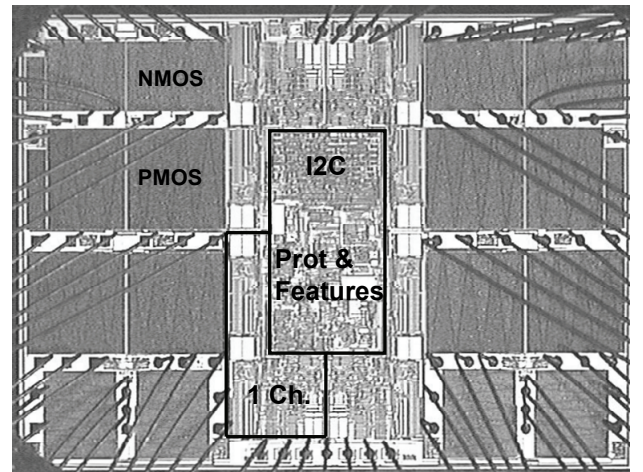


Fig. 9: Chip photo

IV. REALIZATION

The amplifier was realized in the Philips A-BCD2 process, an SOI BCD process with $1\mu\text{m}$ feature size. The chip is targeted as a 4x46W (4Ω, EIAJ) audio amplifier for automotive applications. Fig. 6 shows the topology of one channel. The gain $g_{m2}R_2$ is chosen equal to 1 and realized by a source follower, which behaves like $g_{m2}R_2 \approx 1$ in the frequency range of interest. To achieve a high value of g_{m2} , I_2 must be large, but we need a large I_2 anyway because of the high charge- and discharge currents of the gate of M_3 during crossover and clipping. The load is connected in bridge and a current-mode feedback topology ensures good common-mode stability.

V. MEASUREMENTS

The viability of the calculations and the design is demonstrated by measurements of the output impedance in Fig. 7. Also indicated in this figure are two possible load capacitances. The 10nF line has the same impedance as Z_{out}

when the phase of the output impedance is well below 90° , giving a very damped response. For 100nF, we see it is very close to 90° . Indeed, the measured amplifier is stable for any passive load with a capacitive component less than 50nF, without the use of any external stabilizing network. THD+N is typically 0.005%@1kHz,10W (Fig. 8), SNR is 108dB. Features like line driver mode, no-plop startup, standby, soft mute, load detection, and several protection features are all accessible by I2C interface. A chip photo is shown in Fig. 9.

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