INCORPORATION OF IN-PLANE ELECTRICAL INTERCONNECTS TO THE REFLOW BONDING

B. Moğulkoç[1], H. V. Jansen[1], H. J. M. ter Brake[1] and M. C. Elwenspoek[1, 2]

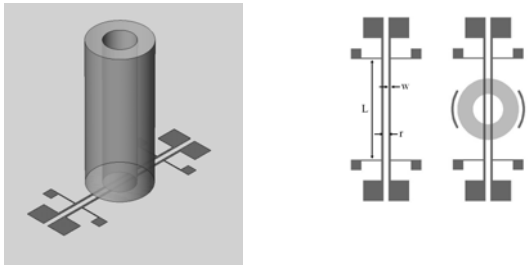
[1] *Institute of Mechanics Processes and Control – Twente (IMPACT) and MESA+ Institute for Nanotechnology, University of Twente, PO Box 217, 7500AE Enschede, The Netherlands*
[2] *Freiburg Institute for Advanced Studies (FRIAS), University of Freiburg, D-79194 Freiburg, Germany*

***Abstract* — This paper elaborates on the incorporation of in-plane electrical interconnects to the reflow bonding. After joining the tubes to silicon substrates, the electrically conductive lines will allow probing into the volume confined by the tube. Therefore methods of fabrication of electrical interconnects, which would survive the bonding and not alter the quality of the bond interface, are investigated.**

***Keywords :* Reflow bonding, electrical interconnects, fluidic interconnects**

I - Introduction

The reflow bonding is the joining technology of glass tubes to silicon substrates [1, 2] to be used as fluidic interconnects to microfluidic devices. The connections can be operated at high pressures and are inherently hermetic. However, integrated microfluidic devices incorporate a lot of functionality with electrical interconnects for sensing and actuation. Typical mechanical applications are microvalves, pumps and flow sensors [3]. Integrated devices for chemical and biological analysis, optical sensing elements, cooling of electronics [4] and manipulation of fluids through electrowetting or electrophoresis [5] are other applications that might require electrical interconnects. Therefore, in this chapter, the incorporation of in-plane electrical interconnects to reflow bonding is investigated.



(a) (b)

Figure 1: *(a) Schematic representation of incorporation of in–plane electrical interconnects. (b) Top view of one of the structures in the mask design.*

The electrical lines start outside the tube and run through the bond interface allowing access to the volume encapsulated by the tube as depicted in Figure 1(a). The connections should be able to survive the bonding process and preserve the bond quality. The fabricated interconnects should stay conductive and should not produce any direct leak paths or cause reduction in the package strength.

II - Fabrication

Two types of in-plane electrical interconnects are fabricated for integration to reflow bonding. The first design is to fabricate boron doped lines in an n-type substrate and the second one is to deposit metal lines. The mask consists of two sets of nine different structures with varying parameters. The structural parameters are labeled in Figure 1(b). The length of the metallic lines, L, is 10 mm and always kept the same. The line widths, w, of 100, 200 and 500 μm are tested with separations, r, of 200, 500 and 1000 μm. The glass tubes are bonded to one set of the lines, while the second set acted as a reference point for comparison.

A. Doped Lines

The selected substrate wafers are lightly n-type doped, <100> oriented, Single Side Polished (SSP) wafers of 380 micron thick. The first step is to grow 2 μm thick silicon oxide by wet thermal oxidation in a tube oven. Secondly, this oxide layer is patterned in buffered hydrofluoric acid (BHF) using a hard baked photoresist mask. After removing the photoresist in 100% nitric acid (HNO_3), the doping can be performed in a tube oven.

Boron nitride wafers are used as solid sources [6]. This process is constant-source diffusion and we name it as solid source dotation (SSD) in this text. After the doping, wells of p^+-type are created in junction with the n-type substrate. We have performed SSD at 1000 °C, 1050 °C and 1100 °C for 60 minutes. After the dotation, the boron containing residue on the doped regions is cleaned by initially dipping the wafers in 50% HF for 2 minutes. The doped regions were still hydrophilic. Therefore the wafers are briefly oxidized at 800 °C for 30 minutes and etched for another 2 minutes in 50% HF. After this procedure, whole silicon surface was clean and hydrophobic. The step height between the protected and the doped regions are measured by Dektak profiler to be approximately 30 nm, 50 nm and 100 nm for the wafers treated respectively at 1000 °C, 1050 °C and 1100 °C for 60 minutes.

B. Metallic Lines

The selected substrate wafers are <100> oriented, Single Side Polished (SSP) wafers of 525 micron thick. The first step is to grow 310 nm thick silicon oxide by dry thermal oxidation in a tube oven. The oxide layer will act as a diffusion barrier between the metals and the silicon substrate to prevent formation of silicide [7]. After standard lithography, the metal lines are sputtered

in Argon plasma. In all of the samples, 10 nm thick Titanium is deposited on SiO_2/Si stack as the adhesion layer or the bond layer as it is known to react directly with silicon oxide [7]. The second metallic layer is the functional layer and is chosen to be either platinum or rhodium due to their high melting temperature and resistance to oxidation. The thickness of the platinum layer was about 310 nm and the thickness of the rhodium layer was about 270 nm. The photoresist mask is lift-off to release the metallic interconnects. For removal of the photoresist, the wafers are put in acetone and isopropanol at 50 °C in ultrasonic bath for 0.5 hours each and let dry in laminar flow bench.

III - Results and Discussion

After the fabrication of both designs, their electrical resistances are measured and the tube bonding is performed by annealing the samples at 700 °C for 30 hours in air environment [1] to test their performance and integrability to the reflow bonding. The electrical resistances of these lines are measured both before and after the tube bonding. The hermeticity of every bonded tube is tested by a helium leak detector. The last step of characterization is to measure the burst pressures of the bonded tubes to check if the in-plane electrical interconnects caused any reduction in the strength of the package and change in the fracture behavior of the silicon membranes.

A. Electrical Resistivity

The electrical resistances of the fabricated structures are measured with four-point probe method by obtaining current–voltage curves and by multimeter measurements. The electrode configuration is exampled in Figure 1(b), where the connections on the side are used to couple current and the connections on the ends are used to measure the voltage drop. The electrical resistances of the doped lines are measured in dark to minimize photo-currents and the junction depths of the diffused layers are measured by the groove-and-stain method [6]. The resistance of doped lines with respect to the line width is plotted in Figure 2 with the sheet resistances and junction depths. The deviation of the measurements was less than 5%. The accuracy was limited by the uniformity of the process.

The surface dopant concentration remains the same during the high temperature diffusion and is determined by the solid-solubility limit of boron in silicon [6]. For temperatures higher than or equal to 1000 °C, the diffusion coefficient of boron becomes dependent on its local concentration [8, 9, 10]. Therefore, the dopant concentration profile deviates from complementary error function curves and extra measure has to be taken to calculate the junction depth. This effect has been studied and formulated by Fair [11]. If the values of the solid-solubility limit of boron in silicon [8], the intrinsic diffusion coefficient of boron in silicon [11] and the intrinsic-carrier concentration of silicon [12] are substituted in the corrected junction depth [11] formula for diffusion temperatures of 1000 °C, 1050 °C and 1100 °C and time of 60 minutes, the corresponding junction depths can be calculated as 0.84, 1.55 and 2.72 microns. These values are quite close to our experimental measurements displayed in Figure 2, especially considering that the diffusion coefficient of boron will be changing more than a decade during the diffusion process at the mentioned temperatures [13].

After the analysis of the SSD process, the electrical resistances of the doped lines are measured after the reflow bonding is performed at 700°C for 30 hours. The bonding is performed in air environment and therefore the silicon wafers are oxidized about 20 – 30 nm [14]. That oxide layer was thick enough to insulate the test probes from the diffused layer. Therefore, the wafers are dipped in dilute HF solution after the tube bonding in order to remove the surface oxide layer before the resistance measurements. The measurement results after the tube bonding showed that the resistance values increased 3% on the average. This increase is within the uniformity limits of the doping process.

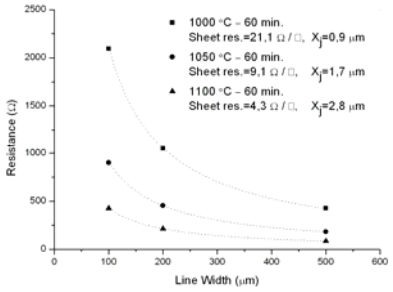


Figure 2*: Electrical resistances of 10 mm long boron doped lines at different temperatures with respect to the line widths.*

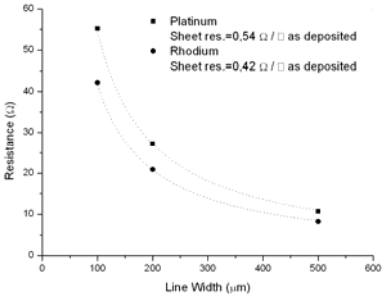
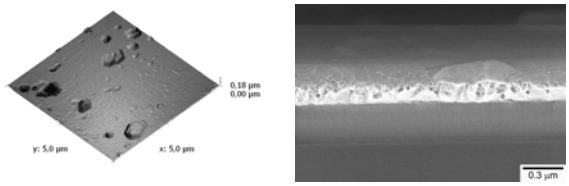


Figure 3*: Electrical resistances of 10 mm long metallic lines with respect to the line widths.*

For the fabrication of metallic line stacks, titanium is used as the adhesion layer to form continuous and smooth coverage [7]. The resistance of metal lines with respect to the line width is plotted in Figure 3 with the sheet resistances. The deviation of the measurements was less than 2%. The accuracy was limited by the uniformity of the process. The sheet resistance of the rhodium stack is slightly less than the platinum stack, while both of them were about one tenth of the lowest sheet resistance of the boron doped lines. After the initial resistivity measurements of the metallic lines,

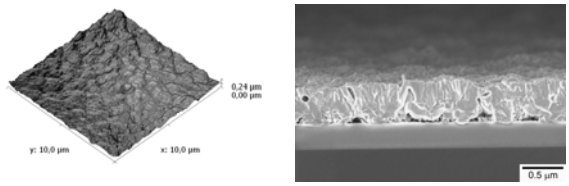
their electrical resistance are measured after the reflow bonding is performed at 700°C for 30 hours. Since the bonding is performed in air environment, oxygen was present in the environment during high temperature annealing.

The platinum lines stayed conductive and their resistance has decreased 13% on the average presumably due to healing of the defects and the grain growth [15]. An Atomic Force Micrograph (AFM) of the surface of platinum layer after the bonding is displayed in Figure 4(a). The grain growth and hillock formation in the platinum layer are clearly visible in the topography. The Scanning Electron Micrograph (SEM) of the cross–sectional view of the stack in Figure 4(b) indicates the porosity of the large grains. Olowolafe et al. [16] and Kreider et al. [17] observed that platinum layer remained unreacted during the Post-Deposition Annealing (PDA) of $Pt/Ti/SiO_2/Si$ stack at high temperature. In conformity with them, our energy dispersive x-ray analysis confirmed that the platinum layer was not oxidized. Relevantly, the base thickness of the platinum layer is observed to remain constant after the reflow bonding.



(a) (b)

Figure 4: *The platinum layer is annealed at 700 °C for 30 hours in air environment for the tube bonding. (a) The surface is examined in an atomic force microscope and (b) the cross–section is examined in a scanning electron microscope.*



(a) (b)

Figure 5: *The rhodium layer is annealed at 700 °C for 30 hours in air environment for the tube bonding. (a) The surface is examined in an atomic force microscope and (b) the cross–section is examined in a scanning electron microscope.*

The rhodium lines lost their conductivity. In presence of oxygen, rhodium starts to oxidize above 600 °C [18]. At and above 700 °C, the oxide layers are explicitly growing on the surface in the form of Rh_2O_3 which is a stable product until around 1000 °C [18]. Although, the lines on which the tubes were bonded showed lower resistivity, their sheet resistances were higher than 1000 Ω/□. An AFM of the surface of rhodium layer after the bonding is displayed in Figure 5(a) with a SEM of the cross–sectional view of the stack in Figure 5(b). Our energy dispersive x-ray analysis confirmed that the rhodium layer was oxidized. The base layer thickness of the rhodium layer was measured to be 580 nm, which is higher than twice its initial thickness. The reason is ascribed to the volume gain during oxidation.

B. Hermeticity

The hermeticity of every bonded tube is tested by a Leybold UL 500 helium leak detector. The tubes are connected to the detector through a flange and pumped down to the background pressure of 0.5 Pa. The bond between the glass tube and the silicon is sprayed with Helium gas. If there is an apparent leak, helium molecules can migrate through direct paths and the detector will read a signal if the leak is above 10^{-9} Pa m^3 sec^{-1}. The maximum signal is obtained by continuously spraying helium to the leaky region and the rates are recorded. As the result of leak tests, all of the tubes bonded to the boron doped lines did not cause any instant leak and were found to be hermetic. However, all of the tubes bonded to the metallic electrical interconnects were found to be leaking. The maximum level of flux was measured to be about 10^{-6} Pa m^3 sec^{-1} for $Pt/Ti/SiO_2/Si$ stack and 3 10^{-6} Pa m^3 sec^{-1} for $Rh/Ti/SiO_2/Si$ stack. No correlation between the structural parameters of the metal lines and the leak values could be found.

C. Bond Strength

The electrical interconnects running through the bond interface might reduce the maximum pressure to which the assembly can be subjected and cause change in the fracture behavior of the silicon membranes. Therefore, the burst pressure of every bonded tube is tested to measure the effect of in-plane electrical interconnects on the strength of the package, as has been done for non-processed wafers [1].

The burst pressures of the silicon–glass assembly containing the boron doped electrical interconnects are measured and the results are shown in Table 1. All of the pressurized samples were found to fracture in the silicon plate. The values are similar to those obtained by testing non-processed 380 micron thick silicon wafers [1]. The step between the protected and the doped regions were completely filled by the softened glass and the fracture mechanism of the silicon substrates with boron doped lines was the same as non–processed substrates. Therefore, the doped lines can be said to cause no reduction in the strength of the bonds and no change in the failure mechanism of the assembly.

The burst pressure of the silicon–glass assembly containing the metal electrical interconnects are measured and the results are shown in Table 2. All of the pressurized samples were found to fracture in the silicon plate. The burst pressures of the samples containing platinum lines were similar to those obtained by testing non-processed 525 micron thick silicon wafers [1]. However, it is good to notice that the burst pressures of the samples containing rhodium lines are more scattered and lower than non-processed wafers.

During the PDA of $Pt/Ti/SiO_2/Si$ stack, the titanium layer at the interface can oxidize [16]. The loss of

titanium bond layer will lead to coalescence problem in platinum layer and the loss of adhesion can be observed in addition to surface roughening in the platinum layer [17]. In conformity with the literature, we have seen that the platinum layer was peeled off the underlying substrate. A SEM of partly stripped platinum layer is shown in Figure 6(a) from an oblique view. This is the edge of the sample presented in Figure 4. Another example is displayed in Figure 6(b), which is the surface of a ruptured silicon piece containing platinum lines. The crack initiated in the glass tube near its inner rim before propagating into the silicon and the lines at the interface are stripped off the silicon piece during the fracture of pressurized assembly. The stiction problem of platinum layer after the annealing is a possible explanation for apparent leaks discussed in the previous section.

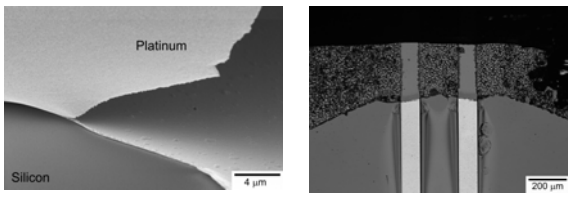
During the PDA of Rh/Ti/SiO_2/Si stack, the rhodium layer is oxidized [18] and thickened from 270 nm to 580 nm. Similar to the platinum lines, the rhodium lines lost their adhesion to underlying silicon substrates. In addition, the rhodium lines at the glass tube–substrate wafer interface were cracked. The oxidation and the cracking behavior of these lines are thought to have altered the electrical resistance measurements.

Table 1: *Burst pressures of <100> single side polished silicon wafers of 380 µm thick, containing boron doped lines at different temperatures, after the tube bonding.*

	1000°C ; 60 min.	1050°C ; 60 min.	1100°C ; 60 min.
Burst press. (MPa)	5.71±0.16	5.71±0.18	5.66±0.1

Table 2: *Burst pressures of <100> single side polished silicon wafers of 525 µm thick, containing different types of metallic lines, after the tube bonding.*

	Platinum	Rhodium
Burst press. (MPa)	7.53±0.53	6.79±0.74



(a) (b)

Figure 6: *(a) Oblique view of the platinum layer, which is peeled off the silicon substrate after annealing at 700 °C for 30 hours in air environment. (b) Top view of the edge of a fractured silicon plate containing platinum lines after the tube bonding and burst pressure test.*

IV - Conclusion

The incorporation of electrical interconnects to reflow bonding is required for probing to the volume encapsulated by the tube and is therefore investigated. Two types of electrical lines were tested for integrability to tube bonding. The first design was to fabricate boron doped lines in an n-type substrate. The sheet resistances between 5–20 Ω/□ were obtained after doping. The conductivity of the lines did not change after the reflow bonding. The doped lines did not cause any leakage or reduction in the strength of the tube–silicon assembly.

The second design was to deposit metal lines. Platinum or rhodium metallic lines were deposited on oxidized silicon using titanium adhesion layer to form Pt/Ti/SiO_2/Si or Rh/Ti/SiO_2/Si stack. The sheet resistances of both types of metal were about 0.5 Ω/□ after deposition. After the reflow bonding, the resistivity of platinum lines slightly reduced while the rhodium lines lost their conductivity. Both types of metallic interconnect caused direct leak paths through the bond interface. Although the presence of these metallic lines did not considerably affect the strength of the glass tube–silicon joint, both types of metals lost adhesion to the underlying silicon substrate after the post-deposition annealing of the reflow bonding.

In light of the presented test results, we conclude that the doping process is easily integrable to the reflow bonding, as they survive the bonding process and preserve the bond quality. However, the platinum and rhodium lines suffered from loss of adhesion after the reflow bonding. Although the platinum lines stayed conducting, the rhodium lines were oxidized during the annealing in air environment.

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