A 1.35 GS/s, 10b, 175 mW Time-Interleaved AD Converter in 0.13 µm CMOS

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Abstract

A time-interleaved ADC is presented with 16 channels, each consisting of two Successive Approximation (SA) ADCs in a pipeline configuration. Three techniques are presented to increase the speed of an SA-ADC. Single channel performance is 6.9 ENOB at an input frequency of 4 GHz. Multi-channel performance is 7.7 ENOB at 1.35 GS/s with an ERBW of 1 GHz and a FoM of 0.6 pJ/conversion-step.
Keywords: ADC, SAR, SA-ADC, time-interleaved, T/H.

Motivation

A trend in receiver design for digital-TV, satellite receivers and set-top boxes is the move towards software defined radios, where the embedded Analog-to-Digital Converter (ADC) is moved closer to the antenna. Such ADCs require 8-10 bits of resolution for GHz range of signals and limited power consumption of a few hundred mWs.

Architecture

The Successive Approximation (SA) ADC architecture has a high power efficiency; it uses only 1 comparator, which makes it suitable for nanometer scale technologies. Its operation speed is however limited at high resolution: for an *n*-bit converter, *n* iterations are required.

By time-interleaving multiple ADCs the operation speed is increased by the interleaving factor [1,2]. A trade-off exists between this factor and the power required for a buffer driving the input load. Here a moderate interleaving factor of 16 is chosen based on the interleaved T/H presented in [3]. In this design an improved version is used which has more bandwidth, includes bootstrapping of the sampling switch for enhanced linearity and includes gain and offset calibration.

An interleaving factor of 16 still requires a high sample-rate of the sub-ADCs. In this design three techniques are used to get a high sample-rate and good power efficiency:
(1) two SA-ADCs are combined in a pipeline configuration (2) the single-sided overrange technique (3) look-ahead logic.

Sub-ADC architecture

An overview of the sub-ADC architecture which is used 16 times in the complete ADC is shown in Fig. 1.

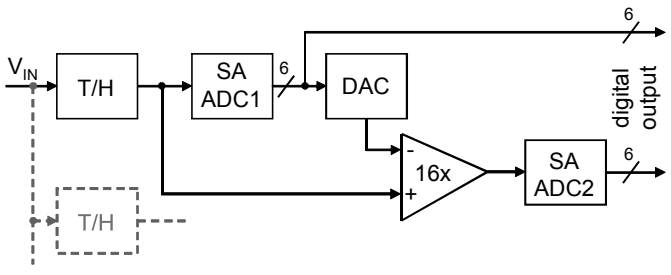

Fig. 1: Overview of the sub-ADC architecture (1/16 of total ADC)

It consists of an interleaved T/H section, a first SA-ADC, a DAC, an inter-stage amplifier and a second SA-ADC. Both SA-ADCs are 6 bit and with the amplifier gain of 16 the resolution becomes 10 bit. Pipelining and inter-stage gain relaxes the requirements of the SA-ADCs: more time is available per conversion and the required accuracy is reduced.

The inter-stage amplifier uses a switched-capacitor opamp configuration with offset cancellation of the two-stage opamp. The DAC is implemented as a resistor-ladder with switches. All signaling is pseudo differential.

An SA-ADC operates in a loop: The comparator makes a decision, the control logic determines the next DAC level and the DAC settles to the next value. For an *n* bit converter *n* iterations are required. All three actions have to be completed within one clock-cycle. Techniques to reduce the delay caused by the DAC and the logic will be discussed next.

Single-sided overrange technique

For a 6 bit converter 4.9 τ of DAC settling is required in each clock cycle, where τ is the settling time constant. The speed can be increased by using the principle of overranging [5]. When an overrange of 1/8 of the range is used as shown in Fig. 2a, the DAC settling can be reduced to only 1.4 τ. The next range has the size of 5/8 of the previous range and $^2\log(1/(5/8)) = 0.68$ bit is resolved each cycle, requiring 9 cycles to reach 6 bits of accuracy.

The overrange technique assumes overrange on both sides of the comparison level. An RC limited DAC however, does not show overshoot during transients and the DAC error is only due to incomplete settling. An overrange is therefore only needed at the side from which the DAC signal is settling. This is schematically shown in Fig. 2b for a rising DAC signal (for a falling DAC signal the diagram is vertically mirrored). The DAC settling requirement is the same as in the case of normal overranging: 1.4 τ. The size of the next range is now 9/16 of the previous range, resulting in 0.83 resolved bits per cycle and only 7 instead of 9 cycles are required for 6 bits of accuracy. The sample-rate can therefore be 30% higher for equal power consumption in the SA-ADC.

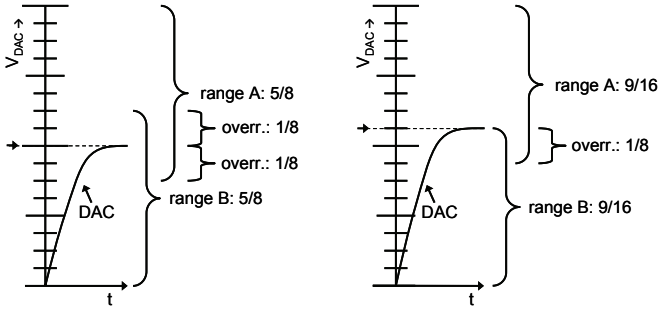

Fig. 2: Overrange techniques a) conventional b) single-sided