A flexible WLAN receiver

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Abstract— **Flexible radio receivers are also called Software Defined Radios (SDRs) [1], [2]. The focus of our SDR project [3] is on designing the front end, from antenna to demodulation in bits, of a flexible, multi-standard WLAN receiver. We try to combine an instance of a (G)FSK receiver (Bluetooth) with an OFDM receiver (HiperLAN/2).**

This paper focusses on the integration of the two receivers. The used modulation techniques (GFSK and OFDM) are very different and result therefore in different receiver structures. As HiperLAN/2 is the most demanding standard, we have used a more advanced receiver algorithm for Bluetooth reception, the MAP (Maximum A posteriori Probability) receiver. Besides the better performance of the MAP receiver, the structure of it is more similar to the HiperLAN/2 receiver.

The resulting partitioning of the Bluetooth receiver functions on the HiperLAN/2 receiver parts is very balanced. As other WLAN standards use the same frequency bands and similar modulation techniques, our Bluetooth-HiperLAN/2 receiver can easily be adapted to these other WLAN standards.

I. Introduction

Dedicated receivers (for one standard) will always consume less power (a factor 10 or more) than a flexible SDR receiver. However SDR has several advantages for both consumers and manufacturers. For manufacturers this could result in shorter development time and cheaper production due to higher volumes. Furthermore, SDR has advantages for consumers because it enables to provide new functionality by software updates without the need for new hardware.

Moreover, in digital communication the trend is, due to Moore's law, that more functionality of the radio transceiver is implemented digital, because the analog part of the transceiver remains the same in every fabrication technology whereas the digital part is scaled down. So the transceiver is more and more digitized which enables software (defined) radio.

A. Outline

The outline of this paper is as follows. First an introduction is given on the SDR project at the University of Twente. Then the two receivers for both standards (HiperLAN/2 and Bluetooth) are discussed and their computational requirements will be presented. Commonly used Bluetooth receivers have a structure that differs considerably from a HiperLAN/2 receiver. So integration of the two receiver is rather difficult. By using a Maximum A posteriori Probability (MAP) receiver for Bluetooth, integration of both standards can be achieved more easily. Finally, a functional architecture of a combined receiver is given and evaluated by looking to other WLAN standards.

B. The Bluetooth-enabled HiperLAN/2 receiver project

In our SDR project [3] we aim to combine an instance of a (G)FSK receiver (Bluetooth) with an OFDM receiver (HiperLAN/2). Our focus is on the physical layer of the receiver: from antenna output to raw bits. The research is carried out by two chairs of the University of Twente: the IC-Design group which focusses on the analog part and the Signals and Systems group focussing on the digital part.

The vehicle of our project is a notebook to which we add the SDR functionality. This has three advantages. First, we can use the processing capabilities of the general purpose processor for digital signal processing purposes. Second, in comparison to SDR for mobile phones, our demonstrator can consume much more power (in the order of 1 W). Third, a notebook is very suited for demonstration purposes.

Table I shows some characteristics of the physical layer of both standards. HiperLAN/2 is a high-speed Wireless LAN (WLAN) standard using Orthogonal Frequency Division Multiplexing (OFDM). Its physical layer is very similar to the 802.11a standard. Bluetooth on the other hand is a low cost, low speed standard, designed for replacing fixed cables. Bluetooth

uses Gaussian Frequency Shift Keying (GFSK) which is also used by other standards such as HomeRF and DECT.

For our project we interpret SDR as an implementation technology: the HiperLAN/2 hardware is that complex to the Bluetooth hardware that the Bluetooth receiver may be added to the HiperLAN/2 at limited costs. This point of view on software radio differs from the views in [1] and [2]; flexible, universal, radio systems at each layer of the OSI model where manufacturers, network operators and consumer can benefit from this flexibility. Our interpretation on SDR is more focussed on the physical layer; an implementation technology, invisible for consumers, which enables shorter development time, patchability and cheaper production due to higher volumes for manufacturers.

In order to gain knowledge about Bluetooth and HiperLAN/2 receivers we first built a test-bed with two separate receivers [4]. The functional architecture is depicted in Fig. 1.

B.1 Analog front-end

A block schematic of the current implementation of the analog front end is given in Fig. 2 [5]. For HiperLAN/2 this is a zero-IF structure with an output of 1 channel at baseband. A HiperLAN/2 channel has a (complex) bandwidth of 20 MHz[1]. Analog-to-digital conversion has to be performed in quadrature and with a minimal sample rate of 20 MSPS (Million Samples Per Second). For our demonstrator we choose to use 80 MSPS, because power-efficient analog filters do not have small transition bands. The analog front end uses a 3^{th} order Butterworth filters with a cut-off frequency of about 11 MHz. So part of the channel selection is performed digitally. In Bluetooth mode, the output of the analog front-end is also a 20 MHz wide signal containing 20 Bluetooth channels (a Bluetooth channel has a bandwidth of 1 MHz). As neighboring Bluetooth channels can be 40 dB stronger than the wanted channel [6], the ADC resolution should be at least 10 bit. (HiperLAN/2 has less stringent requirements.) In our project we use 12-bit ADCs.

B.2 Digital front-end

This test-bed has enabled us to estimate the processing power for both receivers (roughly 2 billion operations per second for each receiver). As our project focusses on a daughter card for a computer/notebook, we can use the processing power of the notebooks' CPU. Current processors, such as the Pentium IV, posses special signal-processing instructions (MMX/SSE/SSE2) [7] and have therefore huge processing capabilities. A Pentium IV can, for example, do four floating point multiplications during one clock cycle. So a large part of the receiver can run real-time on a Pentium IV. Drawbacks of this solution are however, its resource claim and power consumption. As Moore's law will continue for a few years, these drawbacks become less important in the future.

[1]So the bandwidth per quadrature channel is 10 MHz.

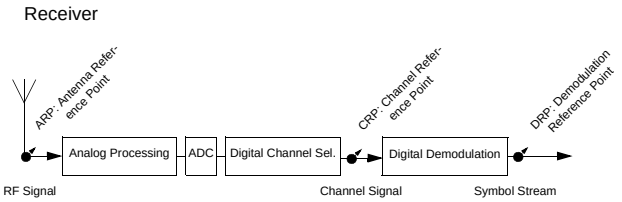

Fig. 1. Functional architecture of the SDR test bed

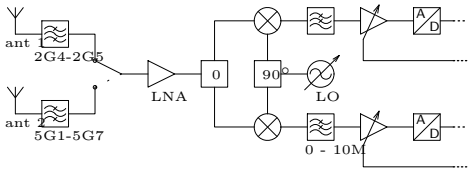

Fig. 2. Block schematic of the SDR receiver (analog part)

II. Functional architecture of a HiperLAN/2 receiver

HiperLAN/2 uses OFDM, a multi-carrier modulation technique. Both the transmitter and receiver operate at 20 Million Samples Per Second (MSPS). An OFDM symbol has a duration of 4 μs (80 complex samples) with 48 data and 4 pilot carriers. A MAC frame has a maximal duration of 2 ms [8]. This frame consists of 5 parts. For estimating computational requirements, we assume that all parts have equal duration and that we have to demodulate 2 parts (one common and one user part). These part have a duration of $\frac{2000}{5} * 2 = 800\ \mu s$ (200 OFDM symbols). Moreover we assume continuous transmission. (Of course, in realistic situations this is not the case.) The number of transmitted OFDM symbols per second is in our case $N_s = \frac{1}{T}M = \frac{1}{0.002} * 200 = 100000$ symbols. (M is the number of OFDM symbols in a burst that have to be demodulated and T the duration of a burst.) For all parts except the FFT, we assume that 16-bit fixed point calculations are sufficient [9].

The digital part of the HiperLAN/2 receiver consists of two parts; channel selection and demodulation

(See Fig. 1).

A. Channel selection

For HiperLAN/2 receiver we use a zero-IF structure with an output of 1 channel at baseband. The output of the ADCs is a complex (2x12-bit) digital signal. As the analog low pass filter removes only non-adjacent channels, the digital channel selection has to remove the adjacent channels and reduce the sample rate to 20 MSPS. Initial simulations showed that 25-tap FIR filters is sufficient.

A.1 Computational requirements

The used ADCs are 12-bit, therefore 16-bit registers in the FIR filter should be enough. Assuming symmetric FIR filters operating at 80 MSPS (at the input rate), 25 taps and decimation factor 4, the computational load is: $2 * \frac{25}{2} * \frac{80}{4} = 500$ million 16-bit multiplications and $2 * (25 - 1) * 20 = 960$ million 16-bit additions per second.

B. Demodulation

A general receiver structure for OFDM is depicted in Fig. 3. To eliminate Inter Symbol Interference (ISI), each OFDM symbol contains a so called *prefix* (of 16 samples) that is a copy of the last part of the symbol. A MAC frame starts with special, known, symbols, so called *preambles*. The synchronization part can use these preambles to detect the start of a burst, estimate the channel characteristics and frequency offset. We assume that these parameters are constant during the burst, because of the HiperLAN/2 standard requirements, the channels' coherence time (of about 10 ms). However current research [10] focusses on the effects of phase noise introduced by the oscillator. We expect that the introduced phase noise also requires (only) burst synchronization.

Demodulation of data-OFDM symbols consists of five parts:

- frequency-offset correction
- 64-point FFT
- channel equalization
- phase-offset correction
- QAM demapping

B.1 Computational requirements

synchronization/parameter estimation: For the time and frequency-offset estimation we used the Schmidl and Cox algorithm [11]. For time offset detection, this algorithm uses a normalized 32-sample correlation to detect the start of the preamble. If the optimal time is found, the angle of a 16-sample correlation is used to estimate the frequency offset and the channel is estimated by using the zero-forcing algorithm.

The HiperLAN/2 standard specifies very stable local oscillators and therefore time-offset detection is only needed during a short time to detect the optimal timing. (If a burst has been detected, the start of the next burst can be predicted very precise.) In our case only 5 correlations are calculated and the frequency-offset detection needs only 1 correlation per burst. Preamble C is transmitted twice [8] and used for channel estimation. So the channel is estimated twice for improved estimation. The computational load can be found in Table II.

frequency-offset correction: The frequency offset is estimated by the synchronization/parameter estimation part and *corrected* by the frequency-offset-correction part of the receiver. It requires one complex multiplication per sample. An OFDM symbol has a duration of 80 complex samples. Only 64 samples of them are needed for the FFT. So 64 samples have to corrected. The computation load is $N_s * 64 = 6.4$ million complex multiplications (25.6 million multiplications and 12.8 million additions) per second.

64-point FFT: The receiver has to perform a 64-point FFT every OFDM symbol. As a 16-bit receiver degrades the performance [9] we assume that the FFT has to be more accurate, namely 24 bit. According to [12], a P-point FFT requires $Plog_2(P)$ complex multiplications. So in our case the requirements are: 384 24-bit complex multiplications.

channel equalization: The equalizer has to "undo" the channel for the 52 carriers. This requires 52 complex multiplications per OFDM symbol.

phase-offset correction: Frequency-offset correction is implemented by calculating only the values of the frequency offset for the first symbol and these values are re-used for other symbols. This saves (computational-intensive) instructions (cos and sin) but also introduces a phase offset. This phase offset can be corrected by using the pilot carriers in the OFDM symbol. This requires 48 complex multiplications and estimation of the phase offset.

QAM demapping: The largest constellation used is 64-QAM. A 64-QAM symbol has $2^3 = 8$ possible values for both the real and imaginary part. De-mapping can be implemented by generating an index for a table that is shown in the pseudo code below:

```
//values of the re and im part of the 64-QAM
```

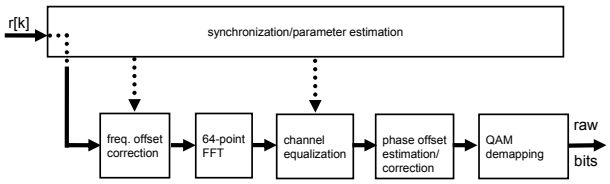

Fig. 3. OFDM receiver

```
//const are:  -7, -5, -3, -1, 1, 3, 5, 7
index = round((input+7)/2);
if (index > 7) index = 7;
if (index < 0) index = 0;
Bits = Table[index];
```

So de-mapping requires 2 comparisons (border checking), 1 addition, 1 multiplication and 1 table lookup. An OFDM symbol has 48 data carriers and each QAM symbol requires two de-mapping operations.

Table II shows an overview of the estimated computational load for each part of the receiver. Computational intensive parts are, besides the SRC, the FFT and QAM demapping. Moreover, the synchronization/parameter estimation requires relatively few computations. The main differences between this table and the computation requirements shown in a previous publication [13] are the introduction of the phase offset correction and the estimation of the computational requirements for the synchronization/parameter estimation part of the HiperLAN/2 receiver.

III. Functional architecture of a Bluetooth receiver

Bluetooth uses GFSK as modulation technique. The symbol duration is 1 μs and data is transmitted in time slots with a duration of 625 μs. For estimating computational requirements, we assume maximal transfer rate. In this mode, Bluetooth uses a packet which spans 5 time slots and 1 time slot is used for uplink communication. Moreover we assume continuous transmission. (Of course, in realistic situations this is not the case.) For all parts we assume that 16-bit fixed-point calculations are sufficient.

A. Channel selection

In Bluetooth mode the output of the analog front-end is also a 20 MHz complex signal containing 20 Bluetooth channels. Channel selection can be divided in three parts:

- Sample rate reduction (from 80 to 20 MSPS)
- Mixing of the wanted channel to baseband
- Removing adjacent channels

The first part, Sample rate reduction, is equal to the channel selection in HiperLAN/2 mode. The next step consists of mixing the wanted channel to baseband by multiplying the signal with a complex frequency. The final step is a low pass filter which eliminates all other channels.

A.1 Computational requirements

Sample rate reduction: This part is equal to the channel selection in HiperLAN/2 mode, so symmetric FIR filters are assumed operating at 80 MSPS (at the input rate) with 25 taps and a decimation factor 4. The computational load is: $2 * \frac{25}{2} * \frac{80}{4} = 500$ million 16-bit multiplications and $2*(25-1)*\frac{80}{4} = 960$ million 16-bit additions per second.

Mixing: Mixing requires one complex multiplication per sample. Mixing is only required during the reception of a packet (which is $\frac{5}{6}$ of the input sample rate of 20 MSPS). Moreover the mixing frequency samples can be generated by using a lookup table. This requires 2 table lookups.

Removing adjacent channels: This part is a low-pass filter. The used MAP receiver requires a symmetric 50-tap FIR for both the real and imaginary part. Furthermore the sample rate is reduced to 1 MSPS (1 sample per bit) after the start of a packet has been detected. The computational load is: $2 * \frac{50}{2} * \frac{20}{20} * \frac{5}{6} =$ 41.7 million 16-bit multiplications per second and $2 * (50 - 1) * \frac{20}{20} * \frac{5}{6} = 81.7$ million 16-bit additions per second.

B. Demodulation

GFSK receivers often use a a so-called *FM discriminator* for demodulation [14]. The output of this FM discriminator are soft bits and a comparator is often used for hard bit decisions. The performance is not optimal but implementation is easy and low-power (AD conversion is performed by the comparator). The demodulator requires a real input signal at low-IF that does not map easily on the (complex) HiperLAN/2 demodulator. Furthermore the channel selection filter is not defined by this demodulator. Therefore we have researched more advanced demodulators and decided upon to use a MAP receiver. This receiver requires an orthogonal vector space which is given by the Laurent decomposition [15]. This Laurent decomposition describes the GFSK signal by a sum of linear, orthogonal, Pulse Amplitude-Modulated (PAM) waveforms.

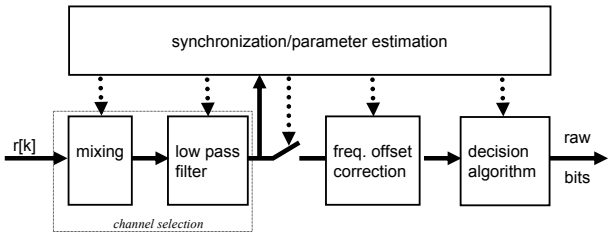

Fig. 4. MAP receiver

C. Laurent decomposition

In [15] it has been shown that GFSK and in general Continous Phase Modulation (CPM) signals can be written as a sum of PAM waveforms. In many cases the signal power is concentrated in the first pulse, $c_0(t)$. In the Bluetooth case [16], the first pulse contains about 99 % of the signal power. So, the GFSK signal can be approximated by using only this pulse (which simplifies the construction of the MAP receiver):

$$\tilde{r}(t, \boldsymbol{\alpha}) \approx \sum_n b_{0,n} c_0(t - nT) \quad (1)$$

where $b_{0,n}$ is the so-called *pseudo symbol* that is given by:

$$b_{0,n} = exp\{jh\pi(\sum_{m=-\infty}^{n} \alpha_m)\} \quad (2)$$

with $\alpha_m = \{-1, 1\}$ the m^{th} data bit and h the modulation index (for Bluetooth: $0.28 \leq h \leq 0.35$).

Moreover this first pulse, $c_0(t)$, defines also the channel selection filter (the low pass filter in Fig. 4). Further research is needed to verify if the adjacent-channel interferer requirements are met with this filter.

D. MAP receiver

The MAP receiver is shown in Fig. 4.

The channel selection filter is a matched filter for the first Laurent waveform $c_0(t)$. The output of the filter is a (SNR maximized) estimation of $b_{0,n}$. This estimation has a maximized $\frac{E_b}{N_0}$ but suffer from Inter-Symbol Interference (ISI). An efficient search algorithm will be needed which determines the *best* path through the trellis diagram. For our MAP receiver we used the *Viterbi* algorithm with 2 states. This receiver requires (for the smallest modulation index) an $\frac{E_b}{N_0}$ of about 11 dB [16] for a BER of 10^{-3} (as is the BER required by the Bluetooth standard).

synchronization/parameter estimation: Data is transmitted in bursts of maximal 3.125 ms (5 time slots), that starts with special a special code, the so-called *access code* [6]. The synchronization part can use this access code to detect the start of a burst, estimate the frequency offset and modulation index. Exact knowledge of the modulation index is needed for the MAP receiver because this value determines the states in the Viterbi algorithm. Estimation of the channel is not needed because the channel bandwidth is smaller than the *coherence bandwidth* [17] (of about 1 MHz). The synchronization part also determines the optimal sample moment and decimates the incoming 20 MSPS to the symbol rate (of 1 MSPS).

D.1 Computational requirements

synchronization/parameter estimation: Current research focusses on synchronization (and the combination with HiperLAN/2 synchronization/parameter estimation algorithms) and therefore the algorithms that will be used are at this moment not entirely clear. We assume that the modulation index is constant and terminal-instance dependent, so it has to be estimated once. However, the frequency offset needs also tracking because the offset can be +/- 75 kHz at the start of the packet and may vary 40 kHz during the transmission [6].

Frequency offset correction: The frequency offset is estimated by the synchronization/parameter estimation part and corrected in the frequency-offset-correction part of the receiver. It requires one complex multiplication per sample. The sample rate is $\frac{5}{6} = 0.83$ MSPS. Moreover the influence of the frequency offset on each symbol/sample has to be calculated, which requires 2 multiplications and 2 table lookups.

MAP receiver: The MAP receiver consists of a 2-state-Viterbi algorithm. This algorithm has to calculate for each state 2 branches and select the best branch. The state with the highest values determines the detected bit. Each branch requires 2 or 3 complex multiplications and in total the Viterbi algorithm requires 9 complex multiplications, 4 complex additions and 3 comparisons (36 multiplications, 26 additions and 3 comparisons). The Viterbi algorithm also operates at 0.83 MSPS.

Table III shows an overview of the estimated computational load for each part of the receiver. Besides the SRC, computational intensive parts are mixing, the low pass filter and the MAP receiver. The main difference between this table and the computation requirements shown in a previous publication [13] is the decimation factor in the low pass filter. In [13] we

used a decimation factor of 5 instead of 20.

IV. A Bluetooth-enabled HiperLAN/2 receiver

The Bluetooth-enabled HiperLAN/2 receiver is depicted in Fig. 5. For both receivers, the first step, sample rate reduction, is the same. In this step, the sample rate is reduced from a 80-MSPS to a 20-MSPS complex signal. The frequency-offset correction of the the HiperLAN/2 receiver can be integrated with the mixing step of the Bluetooth receiver. Frequency-offset correction is the same as mixing; both steps multiply the input signal with a complex carrier.

In the HiperLAN/2 receiver, the FFT has the highest computation requirements (see Table II), whereas, in Bluetooth mode the low-pass filter in the channel selection function requires most processing power (Table III). As filtering and FFT both incorporate multiplications and additions, it is possible to combine them. Low-pass filtering in the frequency domain is not an option because the *overlap-add* method [12] requires far more computations[2] than filtering in the time domain. Other combinations for integration are now very straightforward. The HiperLAN/2 equalizer which incorporates complex multiplications can be combined with the Bluetooth frequency offset correction. Finally the MAP receiver can be combined with the QAM demapper. In our current design of the HiperLAN/2 receiver we use a very simple demapper (because our focus is from antenna output to raw bits). More complex QAM-demappers have a soft-output and are integrated with the Forward-Error Correction (FEC) decoder which also contain a Viterbi decoder.

The resulting partitioning of the Bluetooth receiver functions on the HiperLAN/2 receiver parts is very balanced both from a functional-partitioning perspective and from a computational-load perspective. (See Table II and Table III.)

A. Other standards

Table IV shows a list of WLAN standards in the 2.4 and 5 GHz band. From this table it can be seen that other OFDM standards e.g. IEEE 802.11a and 802.11g use the same physical layer as HiperLAN/2. Thus our SDR receiver is "prepared" for these standards.

[2]This method requires for this applications at least a 128-point FFT and a small 8 point IFFT (decimation and mixing can be performed after the FFT). So far more computations are required than "normal" filtering in the time domain.

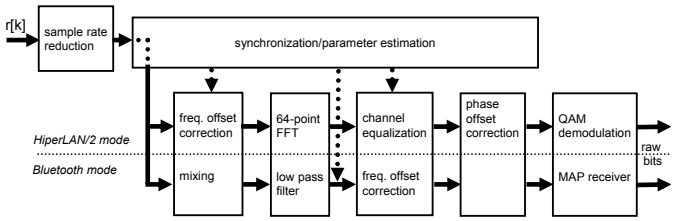

Fig. 5. A Bluetooth-enabled HiperLAN/2 receiver

All other standards use some kind of phase modulation, just like the Bluetooth standard. The structure of a MAP receiver for these standards will be similar to the Bluetooth MAP receiver. So it is believed that, our SDR receiver can easily be adapted to these standards.

V. Conclusions and recommendations

This paper presents a functional architecture of a Bluetooth-enabled HiperLAN/2 receiver. The Bluetooth standard is designed for low power and low cost receivers. Therefore a large part of the receiver is implemented in the analog domain which does not map on a digital OFDM receiver. In our project we used a MAP receiver for Bluetooth. This receiver has better and even optimal performance compared with commonly used Bluetooth receivers. Moreover this receiver can be mapped on the HiperLAN/2 receiver. In the proposed SDR receiver, channel selection of the Bluetooth receiver has been integrated with the frequency offset correction and FFT of the HiperLAN/2 receiver. Moreover the HiperLAN/2 QAM demapper (and FEC decoder) can be combined with the Bluetooth MAP receiver.

The proposed SDR receiver can easily be adapted to other WLAN standards because other WLAN standards use the same frequency bands and similar modulation techniques.

Further research focusses on synchronization/parameter estimation for the Bluetooth mode and the realization of a real-time testbed.

Acknowledgment

We thank our colleagues from the IC-Design group for their work on the analog part of the front-end and for interesting discussions. This research is supported by the PROGram for Research on Embedded Systems & Software (PROGRESS) of the Dutch organization for Scientific Research NWO, the Dutch Ministry of Economic Affairs and the technology foundation STW.

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parameter	Bluetooth	HiperLAN/2
band	2.4 – 2.48 GHz	5.15 – 5.725 GHz
ch. spacing	1 MHz	20 MHz
modulation	GFSK	OFDM + BPSK/QPSK/16-QAM/64-QAM
nom. bitrate (no FEC)	172.8 – 723.2 kbit/s	12 – 72 Mbit/s

TABLE I
SOME PHYSICAL LAYER CHARACTERISTICS OF BLUETOOTH AND HIPERLAN/2

stage	# million ×	# million +	# million special op. cos, sqrt, shift, etc.	# bits
SRC	500	960	0	16 bit
synchronization	2.8	1.6	0.2	16 bit
freq. offset corr.	25.6	12.8	0	16 bit
FFT	153.6	76.8	0	24 bit
channel equalization	20.8	10.4	0	16 bit
phase offset corr.	19.2	10.4	0.3	16 bit
64-QAM demapping	9.6	9.6	57.6	16-bit

TABLE II
COMPUTATIONAL REQUIREMENTS FOR HIPERLAN/2 RECEPTION

stage	# million ×	# million +	# million special op. cos, sqrt, shift, etc.	# bits
SRC	500	960	0	16 bit
mixing	66.7	33.3	33.3	16 bit
low pass filter	41.7	81.7	0	16 bit
synchronization	t.b.d	t.b.d.	t.b.d.	16 bit
freq. offset corr.	5.0	1.7	1.7	16 bit
MAP receiver	29.9	21.6	5.0	16-bit

TABLE III
COMPUTATIONAL REQUIREMENTS FOR BLUETOOTH RECEPTION

name	frequency band	modulation technique
Bluetooth	2.4 GHz	GFSK (BT = 0.5 and $0.28 \leq h \leq 0.3$)
HiperLAN/2	5 GHz	OFDM with BPSK/QPSK/16-QAM/64-QAM modulation
IEEE 802.11a	5 GHz	OFDM (equal to HiperLAN/2)
IEEE 802.11b	2.4 GHz	DPSK/DQPSK
IEEE 802.11g	2.4 GHz	OFDM (equal to HiperLAN/2)
HiperLAN/1	5 GHz	GMSK
homeRF	2.4 GHz	2-FSK/4-FSK ($0.17 \leq h \leq 0.38$)
DECT	1.9 GHz	GFSK (BT = 0.5 and $0.4 \leq h \leq 0.5$)

TABLE IV
PHYSICAL LAYER CHARACTERISTICS OF WLAN STANDARDS